U.S. DEPARTMENT OF ENERGY | Energy Efficiency & Renewable Energy

ADVANCED MANUFACTURING OFFICE

# Wide Bandgap Semiconductors for Clean Energy Workshop:
## Summary Report

July 25, 2012
Rosemont, IL

## THE DEPARTMENT OF ENERGY (DOE)’S ADVANCED MANUFACTURING OFFICE PROVIDED FUNDING FOR THIS MEETING AND SUMMARY.

The DOE Office of Energy Efficiency and Renewable Energy (EERE)’s Advanced Manufacturing Office partners with industry, small business, universities, and other stakeholders to identify and invest in emerging technologies with the potential to create high-quality domestic manufacturing jobs and enhance the global competitiveness of the United States.

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# INTRODUCTION

In the same way that the invention of the silicon chip 50 years ago led to the development of the modern computer and today's electronics industry, wide bandgap (WBG) semiconductors—such as silicon carbide (SiC), gallium nitride (GaN), zinc oxide (ZnO), and diamond (C)—offer an opportunity to revolutionize the next generation of microelectronics and clean energy innovations. Compared to today's silicon-based solid-state technologies, WBG semiconductors can operate at temperatures above $150^{o}$C without external cooling, have the potential for longer lifetimes at higher operating voltages, and can switch at higher frequencies with lower power losses.

WBG materials are increasingly important in many industrial energy-saving technologies and have broad applications in power electronics and solid-state lighting (SSL). Many challenges remain, however, before WBG technologies can gain widespread market adoption in clean energy applications and achieve their potential for reducing overall U.S. energy intensity. In addition, it is anticipated that improving the quality and reliability of WBG semiconductors while reducing manufacturing costs offers significant potential to accelerate deployment of electric vehicles, fuel cells, and grid-integrated renewables.

The U.S. Department of Energy (DOE)'s Advanced Manufacturing Office (AMO) partners with industry, small business, universities, and other stakeholders to identify and invest in emerging technologies with the potential to create high-quality domestic manufacturing jobs and enhance the global competitiveness of the United States. In support of its mission, AMO held a workshop in Rosemont, IL, on July 25, 2012, to identify core manufacturing challenges and key foundational technology breakthroughs needed to support the U.S. WBG semiconductor industry and the market acceptance required to reduce the energy intensity of U.S. manufacturing.

This document summarizes the input gathered during the WBG Workshop from subject matter experts in industry, academia, and government on the current state-of-the-art; industry trends and emerging applications; barriers to research, development, and implementation of WBG semiconductor technologies at commercial scale; and potential actions needed to advance the use of WBG semiconductors in clean energy applications.

Welcoming remarks were provided by Robert Gemmer, AMO Technology Manager. David Danielson, Assistant Secretary for Energy Efficiency and Renewable Energy (EERE), set the stage for the day by describing EERE's mission to create U.S. leadership in the transition to the global clean energy economy.

In addition to the applicability and potential of WBG semiconductors in a wide range of applications, the Assistant Secretary noted that they offer:

- An opportunity for U.S. competitive advantage
- Substantial U.S. Department of Defense (DOD) investment leveraging
- A platform technology for multiple clean energy applications
- An opportunity to expand U.S. manufacturing and retain global export markets.

Mark Johnson, Program Director at Advanced Research Projects Agency-Energy (ARPA-E), concluded the opening session with an overview of DOE's existing WBG efforts, their opportunity as a cross-cutting technology for clean energy, and the current platform research challenges and opportunities.

Workshop participants were then split into one of the three breakout focus areas:

(1) Power Electronics for Electric Vehicles and Motor Drives
(2) Power Electronics for Renewable Grid Integration
(3) Solid-State Lighting.

Participants from all three breakout groups reconvened as a group for the closing session. The DOE facilitators from each session presented summary slides and key takeaway messages from the discussions.

This report presents a summary of the high-level results and workshop discussion.

AMO would like to thank all the participants for their insights and valuable contributions at the workshop. Appreciation is extended to SRA for conference planning as well as to Marina Sofos, American Association for the Advancement of Science (AAAS), for organizing the meeting and preparing this report. In addition, AMO appreciates the participation of all the DOE staff and contractors who played a crucial role in the formulation and execution of the workshop's technical content: Steve Boyd, Kerry Cheung (AAAS), Bob Gemmer, Pawel Gradzki (Booz Allen Hamilton), Mark Johnson, Colin McCormick, Mark Philbrick (AAAS), Rajeev Ram, Susan Rogers, and Kelly Visconti (AAAS). Finally, special thanks to EERE Assistant Secretary David Danielson for both his vision and leadership throughout.

# SUMMARY OF RESULTS

The results of the high-level summary presentations given by the DOE facilitators in the closing session are provided below for each of the three focus areas:

(1) Power Electronics for Electric Vehicles and Motor Drives
(2) Power Electronics for Renewable Grid Integration
(3) Solid-State Lighting.

## *(1) Power Electronics–Electric Vehicles and Motor Drives*

| ***Major Pathways/Approaches for Impact*** |
|---|
| • **Long-Term Device Reliability Coupled with Degradation Physics and Device Failure.** *(User Facility Approach).*<br>o Develop standards and benchmarks for device measurements not applicable to Si-based device operations.<br>o Link simulation and modeling for both device performance and reliability to material defect density and device design for understanding failure mechanisms.<br>o Develop and standardize performance measurements and qualification procedures for incorporating degradation and failure mechanisms not applicable to Si to devices and application-specific systems.<br>o Develop and correlate device reliability parameters to end-system for effective design of future application utilizing WBG device specifications. |
| • **Performance Improvement for Power Electronics Devices.** *(Consortium/Center of Excellence Approach).*<br>o Communicate on pre-competitive terms of device performance specifications and requirements.<br>o Develop solutions to WBG-specific device design knowledge gaps, such as gate drive design, to facilitate knowledge sharing for proper utilization. |
| • **Value Proposition and Cost Reduction for End-System Applications.** *(Vertically Integrated Team Approach)*<br>o Focus on specific applications to define the value proposition for WBG as compared to Si and to develop the corresponding supply chain.<br>o Focus on incorporating solutions across the supply chain, including cost reduction, performance specifications, new processing step reductions, device architectures, and implantation into end-systems.<br>o Develop partnerships across the supply chain, including team members and partners from manufacturing through production with no gaps.<br>o Develop well-defined intellectual property (IP) terms for vertically integrated teams across the supply chain. |

### (2) Power Electronics–Grid Integration and High Voltage (HV)

| Major Pathways/Approaches for Impact |
| --- |
| • **WBG Material Focus.**<br>o Utilize a portfolio approach for both GaN and SiC to solve applicable manufacturing gaps.<br>o Focus SiC-specific approach to reduce its cost and solve its existing manufacturing gaps. |
| • **Hardware-in-the-Loop Simulation Consortia.**<br>o Assist with slow penetration and pull in utility markets. |
| • **Out-of-the-Box.**<br>o Explore HV converter switch devices using optical triggering. |
| • **Wafer and Device Processing.**<br>o Standardize processing methods for wafer size to increase yield.<br>o Investigate processing dependence for grid applications (in contrast, in automotive applications, the interest lies in packaging and testing).<br>o Integrate importance of voltage range, current density, and cost per unit area.<br>o Improve SiC over Si and explore wafer size technology and assets.<br>o Integrate importance of epitaxial thickness and growth rate.<br>o Integrate adiabatic limits, not just Baliga limit. |
| • **Early/Near-Term Market Opportunities.**<br>o Example: Base inverter module for wind currently stacking 5 kV devices. |
| • **Economic Modeling of Value and Cost Proposition.**<br>o Translate technological opportunities.<br>o Identify general metrics for cost and reliability to enable comparison to existing Si-based technologies. |
| • **New Value-Added Applications.**<br>o Develop new value-added applications rather than replace existing technologies that currently work, such as transformers.<br>o New value-added applications include 13.8 kV direct converters without transformers, DOE Solar Energy Grid Integration Systems (SEGIS), microgrids using a disconnect/reconnect switch and asynchronous connection, residential and campus products, and continuously variable converters. |

### (3) Solid-State Lighting

| Impact Areas |
|---|
| • **Substrates.**<br>o Bulk GaN (4- to 8-inch, defect density < $10^4/cm^2$).<br>o Bulk indium gallium nitride (InGaN), engineered substrates, GaN/Si.<br>o Disruptive technologies with downstream implications.<br>o Wafer bowing, particularly at large diameter (6- to 8-inch), affecting doping control and breakdown voltage. |
| • **Epitaxy Process Yield/Throughput/Consistency.**<br>o In-situ monitoring and management.<br>o Improved reactor design, product and composition uniformity.<br>o 1°C, 5nm wavelength difference. |
| • **Thermal Management.**<br>o Packaging (i.e., encapsulants, solder, thermal conductors, interface materials, and active cooling) improvements and cost reduction.<br>o Increased temperature can reduce performance of phosphors and longer wavelength devices and decrease lifetime of other elements.<br>o Manage heat by improving efficiency. |
| • **Visible Spectrum Efficiency Improvements.**<br>o Phosphor elimination.<br>o High-efficiency emitters through red wavelengths (i.e., nitrides, phosphides, etc.).<br>o Other material systems (i.e., gallium arsenide [GaAs], ZnO). |
| • **Synergy with Other Applications.**<br>o Radio frequency (RF) power devices.<br>o Electric Vehicle (EV).<br>o Power electronics. |

| High-Risk, Highest-Impact Critical Technology Breakthroughs to Address Gaps |
|---|
| • **Nano- and Mesoscale Structures.**<br>o Photonic crystals (log piles, nanowire arrays) to change optical density of states and increase relative radiative recombination rate.<br>o Electronic bandgap engineering via 1, 2, and 3-dimension materials. |
| • **Stress/Strain Management Techniques, such as Nanorods as Intermediate Layer, 10–20nm high-k dielectric aluminum oxides ($Al_xO_y$) Layers via atomic layer deposition (ALD).**<br>o Thin nano-columnar aluminum nitride (AlN) on Si, patterned sapphire substrate (PSS) as buffer layer.<br>o Core-shell GaN nanowires (InGaN coating). |
| • **Lasers for SSL devices ([red yellow green blue] RYGB or Phosphor for Good Color Rendering Index [CRI]).** |
| • **Epitaxy Alternatives to metal organic chemical vapor deposition (MOCVD).**<br>o Hydride Vapor Phase Epitaxy (HVPE), high pressure, and other growth techniques.<br>o Oxides, i.e., ZnO. |

| *High-Risk, Highest-Impact Critical Technology Breakthroughs to Address Gaps* |
| --- |
| • **Additional Functions in light-emitting diodes (LEDs).**<br>o Materials and methods for active cooling.<br>o Communications.<br>o Microelectromechanical systems (MEMS) integration, driver functions, directional control, and color tuning. |
| • **Integrate Efficient Frequency Conversion Concepts into LED Chip.** |
| • **Quantum Dot Phosphors (cadmium-free), Rare Earth Mitigation—Longevity Questions.** |

# MEETING NOTES

In the following meeting notes, each bullet captures a statement from a participant. No attribution is given to specific participants except for the DOE facilitators. Minor editing of participant comments has been done to improve readability, but no substantive changes were made. As a result, the transcription of conversations remains rough. Participants shared their opinions but did not come to consensus.

## I. FIRST BREAKOUT SESSION

The discussion in each breakout group kicked off with one-slide presentations by participants who volunteered to share their perspective on the current state-of-the-art and existing challenges and gaps in the industry.

The following questions were used to frame further discussion:

- What would impact in this focus area look like?
- What are the necessary performance and cost targets?
- What are the major barriers and current gaps?

### *(1) Power Electronics–Electric Vehicles and Motor Drives*

***Presentations***

- **Presentation #1**
    - The application dictates thermal/ambient constraints. For the end-application, is the ambient going to be that high in terms of temperature?
    - If WBG operates at 150°C, need to change the packaging (i.e., encapsulation and package housing materials) for >150°C.
    - Bus capacitors, gate drives, and controls also need to operate above 150°C. Si technology is limited above 150°C and SiC or silicon on insulator (SOI) is required.
    - With higher switching frequencies using WBG, also need flux work to connect to module.
    - **Question:** Peak under hood temperature at 140°C, is that what ambient conditions are at?
    - 105°C for under hood compliance. Can qualify at 85°C for no internal combustion engine. Reliability wise, don't actually run at 150°C.

- **Presentation #2**
    - Still room for improvement in basic WBG materials. WBG crystal quality remains well below Si material quality. WBG >1,000 dislocation defects/cm$^2$ versus Si < 1 dislocation defect/cm$^2$.
    - Doing well with status quo, but still a lot to be gained from fundamental materials research. Sufficient quality material is the foundation of beneficial WBG power electronics technology.
    - Need fundamental understanding brought out (i.e., at times in the past, commercialization has come ahead). Historically, WBG power device industry was not viable until first-generation material quality and cost metrics were attained via investment in fundamental WBG materials improvement. We are nowhere near getting all the benefits from commercialization alone. Today's mass-commercialized SiC power devices are functioning well below (about half) theoretical WBG performance limits and Si commercial devices are not nearly as de-rated.
    - We need to keep pushing ahead in cleaning the material further in existing WBGs and alternatives. Further substantial improvements in WBG material quality will enable further

important "next generation" WBG energy-efficient capabilities and enhance beneficial technology infusion and payoff to entire power production chain.
- **Question:** Are we going to talk about air-cooled devices?
  Some packaging technologies have moved along that allowed Si junctions to get to 200°C. Si can get there. SiC diodes have a good foothold in the market. There could be a theme for a Si switch optimized to use a SiC diode. This would allow for 105°C loop (Si switch with SiC diode). *(Note: 1,200 V, 100 A Si insulated-gate bipolar transistor (IGBT) with SiC diode in the same package currently available commercially).*
- For capacitor technology, if the cool plate is done properly, we can get the temperature standards.

- **Presentation #3**
  - GaN: For brainstorming in presenting challenges.
  - Performance and reliability risks. For cost competitiveness, need 6-inch minimum; 8-inch is more realistic. Scaling to high diameter is not trivial because of cracking due to mismatch in epitaxy. No problem with Si substrate itself, but addressing epitaxial material is key.
  - Scaling with high yield (85%) is also needed for cost competitiveness. The issue is not just macroscopic defects, but microscopic defects that create weak spots for high-voltage applications. Moves from the substrate to the epitaxy to fabrication.
  - For performance issues: eliminate performance killers (dynamic on resistance ($R_{ON}$), bulk, surface, interface traps create delayed response), which are dependent on manufacturer. Threshold voltage changes with temperature due to a change of interface and bulk charges. This should not change. Need to understand why it is, i.e., creates shift in density of states and carriers in channel. Catastrophic versus avalanche breakdown.
  - Reliability is dependent on application. There needs to be a good correlation between data generated and various types of defects and degradation, i.e., fundamental understanding of failure mechanisms. High-voltage switching devices.
  - Success metrics: scalable (large chip area), manufacturable (6- to 8-inch wafers), reliable (similar to Si), cost (similar to Si).

- **Presentation #4**
  - User point of view challenges. Even though it's okay to run at 200°C, can reduce system size by eliminating cooling loops with non-Si WBG.
  - Packaging technology and reliability are hindrances right now for temperature.
  - Desaturation protection.
  - High-temperature capacitor. But if want to switch at high frequencies and control bandwidth, need a different control platform.
  - For inverter design (maximum 10 kV), need more access and degrees of freedom. Depending on optimization objective, should choose different solution frequency.
  - State-of-art SiC: 50 A die, 100 A power module, 250°C high-temperature packaging module.

- **Presentation #5**
  - GaN works well and is a reality today with performance advantages.
  - Current status: efficiency with reduced size demonstrated with high frequency (100 kHz) motor drive with system level (drive and motor) energy savings from 5% to 8%.
  - For motor drives, there is a 5% point system efficiency gain using pure sine wave drive compared to square wave drive.
  - Important to note that it is at lower power levels that most improvement is obtained and is often the regime in which motors are often run.
  - Same is true for solar inverter with 1.5% California Energy Commission (CEC) efficiency and >3% low load efficiency gain.

- Problem exists in qualifying for a specific application; since Joint Electron Device Engineering Council (JEDEC)-like standards exist for power GaN devices, users increase the qualification space to ensure reliability in all operating conditions met.
- Real challenge in large-volume manufacturing process is to realize high yielding and reliable kV class devices.
- Higher quality and defect-free GaN/Si heteroepitaxy on 6- to 8-inch wafers are needed for kV class 50 A devices.
- Still running below performance matrix for GaN, currently 3–5x better than Si, but can be pushed further.
- Effort is to get depletion-mode devices performing to GaN theoretical limits and better performing, more reliable enhancement-mode devices.
- **Question**: Was a filter used for the data presented?
- Yes, the losses include losses in the filter.
- **Question:** What about dead time measurement?
- The dead time measurements should be made with a low capacitance probe and we have used 60–120 ns. But this space needs to be further explored with new generation drivers.

- **Presentation #6**
  - Metrics for 6-inch SiC include: < 0.1 $cm^2$ micropipes, <1,000 $cm^2$ screw dislocations, < 800 $cm^2$ basal plane defects (BPDs), and <1.5 $cm^2$ epitaxial topographic defects with <10 µm thickness.
  - For 6-inch GaN/Si, <1 $cm^2$ epitaxial topographic defects with 5 µm thickness.
  - The real battle is epitaxial area. Topographic defects are much more related to killer defects.
  - To make reliable 50 A devices, need half the defects than to date for GaN/Si.
  - Need feedstock to use devices. Technology gaps include transistor commercialization and plurality of transistor suppliers.
  - Need a roadmap by device type, V/A, $R_{ON}$, cost, and applications.
  - Need standards for materials, metrology, and device tests.
  - Reliability performance/science in power system applications also needed.
  - Packaging requirements.

***Further discussion on current state-of-the-art***

- **Facilitator:** GaN devices are on the cusp of commercialization. One of the challenges to think about is the dearth of product portfolio. Don't have available die sizes, for example. Let's say investment is made in devices and reliability, will that be sufficient to apply to transportation applications?
- No. Automotive won't be the first high-volume application. It's about proving technology in the field and getting enough lifetime performance on the road.
- We should develop other markets as well.
- Consider consumer electronics first. Things will go naturally down this path. Automotive has its own development cycle that is longer. Industrial goods will come after consumer electronics because of a shorter lifetime and fatality risks are not as high. When it gets to a 5–8 year lifetime, then we can consider automotive. Need is in place at the same time with field applications in other areas.
- **Facilitator:** Consider impact on non-core powertrain: converters and chargers?
- There is more than just the inverter—DC/DC converter, for example. Not every application in automotive will lead to death. Maybe we don't do traction converter right away. LED lighting might resolve these issues too.
- Two companies are already using solar inverters in Europe. Europe spent 4-years in the design cycle, and is in production right now. Great incentive exists for a 3-phase inverter because cost pressures to increase voltage (1,200 V SiC power transistors). Ramping up pretty quickly in Europe ($15 million

market next year projected) and eyeing 6-inch wafers coming out soon. Europe is very carefully monitoring because 20-year reliability is needed.

- What is the value proposition for the end consumer?
- For automotive, it's safety without question. Also have to determine whether there is a value-added for the consumer. Baseline is Si. It doesn't have to be the identical price, although that would make it easier.
- Government funding is needed because quality of standards increases costs. If you can translate to better yields, you won't need to overdesign and push cost.
- More than device cost. It's the value. Not well understood yet and how it would apply. Improvement in material quality helps drive cost down.
- Automotive value: cost reduction; size reduction (i.e., packaging); efficiency and reliability.
- When we look at overall requirements, we need to look at packaging. Question is, will it fit into vehicle architecture? Car does not have infinite space. If you have an application, and you cannot package, that would be a motive. The problem with the devices with WBG is the packaging. It's the other things (non-WBG) that need to be brought up to the same level. The WBG is not the weakest link. For packaging, need to do it in a harsh environment.
- Consider applications where magnetics and galvanic isolation are required (i.e., DC/DC converters and chargers). Drivers and inverters are an application, but the switching frequency is also an area (i.e., chargers, converters).
- WBG is not going to be wholesale, that is, won't replace all Si components. Play to strength.
- **Facilitator:** Considering cost, is the cost of epitaxy not that significant? Should we focus on substrate?
- Unit cost, cost of substrate. When analysis is done, the epitaxy cost is not trivial. In the lighting business, it's 10% of cost, but once high volume is reached, it is not an issue. At the end of the day, for the epitaxy unit cost, how much does it contribute to final cost? Driving down cost of epitaxy for government funding is not most important. What is important is the substrate, as well as yield. Investment could be made for higher power devices.
- **Facilitator:** What current voltage level and amps would be transformational? ARPA-E is making the investment in 200 A devices right now. Do we continue investment? What about reliability? The ARPA-E program set defect density targets, but could not fund reliability because it needed to have a stable device design (i.e., once you change parameters, you can't do). Two years ago it was too early. Are we at the point that devices are stable enough that we can look at reliability? What people think a gate should look like has changed in 2 years. Where do we need to be in terms of defect density?
- 50 A is a good compromise. Needs epitaxial improvement, but get a balanced stable device in terms of power. The real cost killer in SiC is not the epitaxy process, it's the yield (i.e., it can drop from 85% to 40%).
- **Facilitator:** Si switch requires protection that is eliminated with SiC and leads to cost improvement in the grid.
- Focus on defects to understand reliability. Yields are lower at larger die sizes. These defects are a problem because one can't tell what defects are the killer ones. Not failing anything inside the SiC, but in the process (i.e., circuits, etc.). For solar, 50 kHz is the value proposition to hit cost targets.
- Fear of unknown. Current overdesign is used to overcome reliability and cover device inconsistency.
- **Facilitator:** SiC diodes (first in power supply, high-end supply). Took a leap of faith because of customer demand in data centers. Why has automotive space moved less slowly into SiC diodes?
- Cost. It is always being looked at, but is 5x the cost with WBG according to module suppliers. Have to get close to parity in cost for original equipment manufacturer (OEMs). Used 10 years ago and saw improvement, but didn't use due to cost. Need to look at best Si IGBTs and diodes, and need to always compare to latest Si technology and performance. Always benchmark against current Si. This is the measuring stick.

- Data centers run all the time. Maybe chargers are a good application because they run a long time.
- People also questioning Si. Need data.
- Matching the SiC diode with Si IGBT doesn't always work well. Not just drop-in replacement.
- **Facilitator:** Can there be a program for long-term reliability? Packaging and reliability program to evaluate different devices? For example, central location for evaluation of hundreds of devices to test and communicate back to device manufacturers. Consider existing Si test? If there is an interest in reliability, how do we establish when we need lifetime results? Can we have a federal government program that takes 3 years to collect data? Sometimes there is no way to accelerate testing. Even most aggressive requires 3 years.
- Understanding rather than just testing needed in conjunction.
- Having the existing building block of device evaluation and building off of it. Have folks submit their devices and provide feedback to suppliers and how they stack up and their performance without revealing information to competitors.
- We can learn about how to best use devices.
- **Facilitator:** Is there an opportunity with gate drives where everybody's figuring these out on their own so far?
- Wind program has a database for grid box reliability.
- Group approach versus cost-shared user facility. Maybe high-end characterization agreement and industry agreement on how to share data.
- Benefit is for final manufacturer, not device folks. A feedback mechanism that will drive adoption and save money on applications.
- Typically, each company would do its own qualification, so the U.S. would not gain knowledge. A common pool could potentially address this and accelerate development.
- Need an honest broker, such as the government, and communication has to be between partners. Some companies have already made this investment.
- Consider high-temperature power electronic facility at U.S. Army Tank Automotive Research, Development and Engineering Center (TARDEC) as a model.
- Need to incorporate the understanding of the physics of failure.
- Another mode of sharing—developing a gate drive circuit and demonstration activity. Competitive standard to develop test bed?
- There are resident technical experts to help users at the facility; these experts have the appropriate equipment to help teams and then spread teachings.
- IP sharing is through centers of excellence at universities or national labs.
- **Facilitator:** Foundry service is from Defense Advanced Research Projects Agency (DARPA), Metal Oxide Semiconductor Implementation Service (MOSIS). There is an evaluation of design with a cost-share approach. SiC wafer runs or unit-processing in same model? A way used by DOD to make sure fabs are always full. Where is the opportunity in the supply chain?
- Difficult because there are unique processes with SiC. These unique processes are also proprietary, so not at the wafer level, but rather, should be done at circuit and device level.
- **Facilitator:** Packaging shuttles. Temperature, so people know how to package, and manage that risk by government. Circuit design is constantly changing.
- What's the final outcome? Still need understanding of physics. Have a central location. Evaluating benchmarking performance with not just 10 devices for fundamental quality assurance, i.e., not for application, but for feedback. Can learn what drives reliability data.
- Need a balance in $20 billion industry. Case-by-case, when you want to engage to balance proprietary. Access to failure analysis and deep-dive. Understanding what the mortality and killers are (i.e., defects), to then be able to adopt end-user goals.
- People present data to OEMs all the time, but it is hard to compare one from another. If done in the same manner, that's how they end up convincing the OEM to adopt.

- Can be a real enabler for formulation of GaN. Can speed up development.
- Large number of samples, not just 10, and want to see consistency since that's the big deal for OEMs.
- Si processing. Wouldn't you use the same for reliability study? Yes. But it can be more than that. Before this uniformity, smaller sample testing needs to be done to get understanding of defects and failures.
- Sampling must have to be different because of crystal size difference between Si and SiC, and GaN. Need to address variability across with more testing.
- How did batteries, with many of the same issues, get there?
- A lot of money. You have no choice in batteries. Don't want to replicate battery fiascos.
- Currently de-rate SiC because they don't understand the failure mechanism.
- Still learning about packaging failure mechanisms.
- Understanding value proposition. There has never been a full demonstration in traction in WBGs. Mitsubishi has a SiC roadmap, for example, Toyota has done packaging.
- Learning from the value proposition. Still need to learn how best to use devices and how to manage with application.
- Proper system design is a gap. The gap will always exist, will claim you overdesign.
- **Facilitator:** Question for drives. If individual teams are funded right now, and every team has to learn how to do gate drives on their own, for the teams with industrial performers, it becomes a competitive advantage. Is there a government role in a user facility?
  Two different modes possible: (1) Semiconductor Manufacturing Technology (SEMATECH)-like with information available to all, or (2) more proprietary with one-on-one interaction.

## (2) Power Electronics–Grid Integration and High Voltage

- Grid requires high reliability, so it is challenging for innovation.
- Trillion dollar industry, few technologies, but still very important.
- Want something out of it, i.e., HVDC and solid-state transformer (SST), so let's try to get it done.
- Manufacturing challenges and new opportunities to move technology to get into the power grid.

*Participants in this breakout session were asked by the facilitator to list the challenges, opportunities, and other general issues in the field on index cards. Listed below is a compilation of the index cards submitted.*

***Index Card Summary***

- **Challenges**
  - Costs
    - Gate dielectric for both SiC and GaN.
    - SiC is expensive.
    - Substrate cost for WBG is too high. SiC is good, but wafer cost is too high.
    - SiC devices are expensive. This is because SiC material is the dominant cost of devices.
    - Reduce cost to <$20/A.
  - Yield
    - High yield. 10 kV SiC metal-oxide-semiconductor field-effect transistors (MOSFETs) and 10 kV SiC junction barrier Schottky (JBS) diodes.
    - Improved Si IGBT yield.
    - High yield, more manufacturable tools, 6-inch (150 mm) 4H-SiC wafers. Larger devices.
    - SiC power device manufacturing on 6-inch (150 mm) 4H-SiC wafers.

  - Wafer is a big component. Size of the wafer is key to improve yield and match with Si infrastructure.
  - Size of wafer and number of people making wafers (i.e., competition) is key to drive cost down.
- Voltage/Current
  - High voltage devices—how high can they be?
  - What is the highest voltage GaN device rating?
  - SiC devices, 600 V to 1,700 V SiC MOSFET and JBS diode.
  - >15 kV 100 A SiC IGBT.
- Reliability
  - Reduce defect density in bulk SiC and GaN by two orders of magnitude, i.e., <100/cm$^2$.
  - Cheap defect-free, large substrates for high yield manufacturing, SiC, GaN, AlN, ZnO, etc.
  - BPD reduction & lifetime enhancement, uniformity.
- Packaging
  - Common (packaging, costs, current), unique (high voltage device current).

- **Opportunities**
  - New Materials
    - GaN substrate at a low price is being developed by the LED industry.
    - Future manufacturing process and material.
    - More than one candidate for WBG (i.e., SiC, GaN, etc.).
    - Choice can be made based on semiconductor material properties and/or more likely metal-oxide-semiconductor (MOS) (gate/dielectric) quality.
  - System Designs
    - Design and manufacturing for system reliability.
    - Balance of system components.
    - Overdesign to accommodate defects.
    - New junction termination technology to solve a critical reliability issue.
    - System-level benefit—lower weight, better efficiencies: this needs larger devices.
  - User Facilities
    - Open user facilities (national labs) to manufacturers for testing processes to see if common manufacturing facilities can be available in the future.
    - Test bed/toll facility.
    - Set up multiple (each complimentary) user facilities at national labs.
    - DOE Fab?
  - Defects
    - Reduce bulk and epitaxial defects in SiC and GaN to below <100/cm$^2$.
    - Better metrology of SiC defects: effect on yield, reliability, and costs.
    - Defect density, reliability, and yield connection. Science of nucleation of SiC epitaxy to eliminate BPDs.
    - GaN/GaN has a defect density of $10^6$/cm$^2$.
    - GaN/sapphire has defect density of $10^9$-$10^{10}$/cm$^2$.
    - GaN on others have similar defect density.
    - It is not clear that GaN on an alternate substrate can have reliable high-voltage termination because of the defect density.
    - More university research on reliability all the way from materials to systems.
  - Epitaxy and Growth
    - New epitaxy for SiC.
    - Epitaxy for new materials.
    - More broad-based efforts on epitaxial growth in SiC.

- High growth rate SiC epitaxy while simultaneously achieving high lifetime epitaxy.
- Science of SiC growth on 2$^o$ offcut SiC substrate is a challenge.
  - High lifetime epitaxy for thyristor, need uniformity.
  - Large die—1.4 cm x 1.4 cm.
- Demonstrations
  - Demonstration of possibilities.
  - Liability issues, possible DOE role.
  - SiC/Energy Star-type subsidies.
  - Field demonstrations targeting wind, photovoltaic (PV) solar, marine, etc.
- Standards
  - Manufacturing standards.
  - Standardize manufacturing equipment.
- Doping
  - GaN is typically a lateral device, which may not be the preferred design for high voltage because of lack of avalanche capability.
  - Vertical GaN requires p-type doping in the termination. This is very difficult. High voltage vertical GaN requires epitaxial doping $<10^{16}cm^{-3}$. Doping of GaN epitaxy with n-type doping $<10^{16}cm^{-3}$ has not generally been demonstrated. Epitaxial growth rate can be an issue.
  - Many vertical GaN devices require p-type doping—key issue is how to implement the p-type doping.

- **General**
  - Applicability
    - Is this a SiC dominated platform technology?
    - Is there room for market-driven new materials?
    - What if there are alternative approaches to economically thick GaN other than GaN/GaN?
    - GaN is not likely to provide significant technical advantage over SiC in the ultra HV area.
    - Cost with GaN is promising, but is GaN really feasible for 1,200–1,700 V devices?
    - <1,000 V GaN is promising, for >1,000 V, SiC looks better. 1,200 V is very feasible with lateral GaN device and >2,500 V would be the domain for SiC vertical devices. >1,200 V and <2,500 V is a no-man's land with the most suitable device depending on the operating current level and frequency of operation.
  - Institutional
  - Funding Challenges—end user/customer not there.
    - Zero sum game.
  - Utilities are a regulated industry—risk adverse.
    - This is because there is limited competition, both for epitaxy and substrates.
    - Investments should be made to have diversity in SiC players at device, epitaxy, and substrate levels. Need think tank to educate and guide customers.

*Presentations*

- **Presentation #1**
  - For MW applications, SiC diode hybrid with Si switches is a promising entry point for SiC.
  - SiC diode technology brings a definite benefit in reducing the turn-on switching losses of the semiconductor switch.
  - Full SiC modules show an additional reduction in losses compared to hybrid technology, but are limited mainly by their low-current rating and over voltages due to the fast unipolar SiC switch.
  - Hybrids are limited by Si operating temperature. Si may not be optimized. Need faster Si switches.

- High-power Si semiconductor devices, packages, and system topologies are continuously improving for achieving higher power, improved efficiency and reliability, and better controllability.
- In order to fully benefit from the advantages of SiC in MW applications, further developments are required, i.e., optimized fast Si switches and packages with reduced parasitics, gate drives, and topology concepts.
- Current capabilities for SiC are not there for MW applications. Demands include:
  - Power, i.e., higher current and temperature, with single device/chip area, 200°C and packaging.
  - Loss, i.e., lower static and dynamic losses, on state losses, system and packaging for higher frequency.
  - Cost, i.e., lower device and system costs, system topologies including modularity, lower cost and higher power. Need to look at packages and magnetics—systems analysis needed—specific cost targets?
- Market Size—$1.5 billion for HVDC offshore system. Devices are a few hundred million.
- GaN voltages and current levels are too low. No thorough investigation and analysis.
- Other WBGs, would like to know more about a good area for fundamental research and development.
- Current (A) is the main concern. What is the decision criteria? Is management required to forward specifications to AMO? Manufacturers would like to know what to aim for.
- For currently explored HV applications, costs are the current problem.
- 1,200 V SiC is currently going into inverters at 2–3x Si prices.
- There are manufacturing challenges and opportunities. Goals are desired.
- The major challenge is yield, specifically identifying challenges that impact yield (i.e., micro piping).
- Use of manufacturing tools for 4- to 6-inch (100–150 mm) and scaling since 6-inch (150 mm) is more common.
- 6- to 8-inch wafers for Si. Leverage state-of-the-art in the Si processing industry. Wafer handling, reworking, cleanliness, etc.
- They over-design a device for a specific rating. Die size selection, optimizing design for manufacturing.
- For 10 kV diodes, need enough people buying the devices and need to interface with end users to know specifications.
- Grid integration resistant to new innovation. New technologies are not market driven because there is no demand for it. Need to think about consumer, product specifications, cost points, and risks.
- Grid was designed around early invention of transformer. Easy way to convert voltages. Need to think about the paradigm shift, not just replacing for the sake of replacing. Hard to displace technologies that have been optimized (maybe DC, microgrids, inverters, etc., versus SST). Need to build a market instead of replacing at a higher price point. People are not solving the problems that the grid has. Currently still don't know what the market size is.
- Address the spectrum, i.e., 600 V to 10 kV. Want the platform that can address all applications, not just HV.
- Need to make the argument for increased reliability, etc.
- Need to think about business cases and find out how to address challenges. Need to think about the market case and core challenges, i.e., for transistors it's lithography and for WBG it's defects.
- Is it the right area to invest in? No rational company will put all their eggs in this basket, i.e., the grid.

- Need fundamental growth of wafer scale-up capabilities. HV needs another platform that might build on low voltage (LV). Find commonalities in a base platform with HV as another revenue source.
- Framework for common challenges with other electronics and unique challenges for HVDC.

- **Presentation #2**
  - A big technical challenge is the gate dielectric for reliable, normally off applications at high temperatures.
  - Have observed negative shift of threshold voltage with increasing temperature for Si and SiC. Expect that there are traps that change the threshold voltage.
  - GaN field-effect transistor (FET) retains threshold voltage better as a function of temperature than SiC MOSFET and Si super junction metal-oxide semiconductor field-effect transistor (SJ-MOSFET).
  - Interfaces depend on normally-on, normally-off.
  - Understanding of dielectric trapping (i.e., temperature and time dependencies). Gate dielectric trapping is less of a problem for negative gate bias.
  - Hafnium oxides and other work. Is it synthesis or characterization? New materials or better understanding? Everything is needed.
  - National labs have the capabilities to help address these challenges.
  - Gate oxide reliability work—want much less transconductance for HV.
  - There is a unique challenge for LV to HV; gate oxide should be okay. 15 kV won't use as much current density.
  - For LV (i.e., 600 V and 1,200 V), need to consider gate oxide. Limitations want U-shape metal-oxide-semiconductor field-effect transistor (UMOSFETs).
  - Trenching, oxide growth on different crystal faces.
  - High-k dielectrics will help. Electric field at the bottom of the trench. Electric field jumps up by 3 if using silicon dioxide ($SiO_2$). Need some way to shield or block fields.
  - GaN is more of a lateral device. Cascade structure will have charge trapping between devices.
  - **Question:** What are the challenges with scaling?
  - HV needs thick layers of GaN/GaN. New device structures need to have high blocking voltage without current collapse. Limitation is from drain to substrate.
  - Baliga on-resistance, trade-offs, but will hit adiabatic issue, i.e., it can't absorb heat in a fault condition. Need area and thickness.
  - Applications are not just blocking. IGBT eliminates need for fuses. Vertical device is not necessary, just volume for absorbing heat. Long way from GaN/GaN.
  - Want low doped layer under device layer. Lateral scaling for HV may encounter many surface issues, then also adiabatic issues.
  - Are there alternatives other than GaN/GaN? Lots of novel thick layers of GaN but not manufacturable for a while.
  - Not just a lateral device. Still needs thick epitaxial layer (low doped, low defect). Not just surface engineering. There are fundamental understanding gaps still for impact ionization, etc.
  - Not just a zero sum game. GaN has advantages for surface devices.
  - Volume devices might not make sense for HV devices. GaN thick will have a comparable option no better than SiC.
  - Caution with putting all the eggs in one basket.
  - Integration is different from connection. 600 V plus should be the focus. People are looking at grid connection and on the load side. We want to look at everything in between. There are lots of options for 600 V and below.

- **Presentation #3**
  SiC technology path.
  - Commercial now is Schottky, MOSFET, vertical junction field-effect transistor (VJFET). Moving to Schottky, then PIN diode, and long term is gate turn off (GTO), IGBT, and FET.
  - Near-term application is integrating Si switch with SiC diodes.
  - PIN diode has 10x higher current than Schottky and Schottky has thermal runaway issues. PIN diodes are slower devices due to charge storage.
  - What is missing is the consideration for $R_{ON}$. 6.5 kV plus PIN diode needs to be mature to think about the $R_{ON}$ issue.
  - **Question:** What is the current density where SiC becomes competitive?
  - **Answer:** Two diodes for every 4 switches. 50 A/die for switches at 4.5 kV. Majority carrier device—10 kV is 30A/cm$^2$ and 1 kV is 100A/cm$^2$.
  - Reliability is important for device, which translates to defects.
  - Current and blocking voltage is a cost issue. Increasing voltage without increasing cost is a good value proposition.
  - HV Si switches are not made in the U.S.; technologies for packaging could be domestic.
  - **Question:** Where is DOE's role in helping SiC GTO in 3–5 years?
  - MOSFET uses the same manufacturing capabilities.
  - Addressing fundamental issues. There is a technology role and a cost role for module manufacturers. There are not enough big dies so there are more issues with control and packaging. What is the current density and how big can we make it reliably? A common issue is bigger wafers. Will get to it eventually. Economic drivers, if the government helps make jump.
  - 6.5 kV with 60–80 A SiC MOSFET, and also 10 kV diodes available, but no one is playing with them.
  - SiC is expensive for end users to adopt because materials are expensive.
  - **Question:** Why is it expensive?
  - Not enough competition or players. A lot of MOCVD takes place in Asia.
  - Need to proliferate more users. DOD investments have good specifications and some products have come out of it. Government subsidies are needed to speed up the development cycle.
  - We need to think about the problem differently.
  - Five layers of stakeholders exist so there is no security.
  - Role of test bed. Hardware in the loop since the main challenge is proving the technology.
  - Question is structural, mission in life is different.
  - Technology transfer to help get things out of the national labs. SEMATECH for power electronics.
  - **Question:** Would it be beneficial to develop an industry and technology roadmap?
  - International Technology Roadmap for Semiconductors (ITRS)—industry, national labs, academia, etc., all working together. Alternative technologies that can address challenges.
  - Want level playing field and specifications. Find common denominator, such as Si lithography.
  - **Question:** Will Si be able to meet the challenges? Will we miss the window for applications?
  - Having the community, entire supply chain to come in, is very important with key stakeholders.
  - Need large dies as well as large wafers.
  - Low screw dislocations SiC wafers. Minority devices limited due to quality, lifetime issues, termination issues (i.e., two-dimension [2D] field issues), and dielectrics (not a key issue for SiC).

## (3) Solid-State Lighting

### *Presentations*

- **Presentation #1**
  New things in WBG materials and device development.
  - The big "green" gap and how to get more indium (In) into the film without defects?
  - New epitaxial techniques and greater In incorporation, strain management, GaN substrates, and reduced micropipes in SiC.
  - Materials and device development needs include:
    - Strain management needed for InGaN for higher efficiency at $\lambda$>525 nm.
    - Substrate materials, including large area GaN and SiC micropipe reduction.
    - Alternate ZnO-based material system requires an effective and reproducible p-type dopant, reduction of defects with Mg or Cd alloys, and demonstrated stability and reliability of devices.
    - Droop-low efficiency at high current density. Non-polar/semi-polar orientations of GaN have demonstrated improvements.
  - Packaging of high brightness LEDs:
    - Temperature, i.e,. component lifetime, and thermal management for LEDs approaching 250 lumens per watt (lm/W). Active cooling for improved efficiency, light output, and operating lifetime. Thermal management has relevance for high power RF devices as well.
    - Color quality and binning. Commodity polychromatic phosphors combined with UV emitters.

- **Presentation #2**
  - Native substrates used everywhere except GaN.
  - 20% of electricity used for lighting. For SSL:
    - GaN-based LED efficiency >5x incandescent, >2x fluorescent.
    - Principal barrier of implementation of SSL is cost, $/lm. Efficiency is important, but the cost has to go down. Higher power density is also key.
    - Get lower droop for GaN/GaN, less heat sinking required, simplified and cheaper packaging, and reduced epitaxy costs. A commercial GaN/GaN lamp delivers 50 W equivalent light for 12 W with a lifetime of 3 years and <1 year payback. Announcements about GaN/GaN LEDs have also been made by NG Insulators, Seoul Semiconductor, and Toyoda Gasei.
  - For power electronics:
    - 40% of electricity used by motors. High potential. More efficient with variable-speed controls.
    - Theoretical performance is 10x SiC, 1,000x Si, and native substrate required. GaN/GaN devices with superior performance to best SiC/SiC have already been demonstrated.
    - Vertical devices need low defect substrates to get the improved performance of GaN/GaN. Evidence is available that reducing defect densities to $10^6/cm^2$ can mitigate droop.
    - Potential of 10%–88% higher motor efficiencies with 50% lower inverter losses.
    - GaN-based electronics will be cheaper than SiC because of LED industry.
  - The enabler is low-cost, high-quality, 4- to 8-inch GaN substrates.
    - Have different requirements for LED, electronic substrates.
    - U.S. industry (ammonothermal, HVPE, other?) can meet the challenge given funding.
    - Support "ecosystem" including raw materials, chemical-mechanical polishing (CMP).
    - High-performance green (530 nm) lasers demonstrated on semi-polar substrates may also be important for LEDs. Performance can be limited by uniaxial relaxation due to generation of misfit dislocations from pre-existing threading dislocation. Reducing the concentration of threading dislocations in semi-polar substrates by 2 or more orders of magnitude is possible

and may lead to dramatic improvements in the performance and lifetime of long-wavelength light emitters.
  - Leading manufacturers of bulk GaN are currently overseas. Substrates, with ~$10^6$/cm$^2$ defects, are driven by laser diode market and are too expensive and not big enough for widespread deployment in LEDs.

- **Presentation #3**
  - Philips Lumiled: why only 20% efficiency?
  - Blue LED is only 43% efficient (0.7 A). Efficiency droop due to increase in the power, lose the efficiency.
  - Losses due to the photon conversion in red and green phosphors (i.e., phosphor photon efficiency), stokes conversion losses, remove the phosphor architecture to get more In into the material and epitaxy to get to 56%. Completely electroluminescent devices.
  - Mismatch between white light out of device and sensitivity by human eye. Red phosphor, europium (Eu) material issue, is creating a red wavelength out of the range of human eye response, lose efficiency.
  - Four grand challenges:
    - Efficiency droop: near-100% efficiency at all currents.
    - Green-yellow gap: near-100% efficiency at all wavelengths.
    - Lack of narrow line width wavelength down conversion, especially red, output. Need to match human visual response. 615 nm, orange gap.
  - Functional light, control of light in intensity, chromaticity, time, and space to get to 85%. Smart lighting: directionality, presence-sensing. What is the current mass ratio of the phosphors? (90:10 green to red).
    - Red phosphors—Eu-doped. Quantum dot phosphors.
    - Mass ratio: yellow >> red, very little Eu.

- **Presentation #4**
  A holistic alternative view with four main focal areas:
  - Materials for SSL: low defect GaN, or other WBG materials, over the visible range, as well as high-pressure MOCVD growth. Epitaxy tends to replicate inherent structure of substrate, including dislocations and defect densities.
  - Devices for SSL: large area, low current density, high lumen, and low-cost devices. Move away from the point source, high current density devices. For broad-area light sources:
    - High current density may not be necessary.
    - Get around efficiency droop problem.
    - Emphasis on maximum efficiency may be a dead end.
  - Components for SSL: universal SSL "bulb." Need some type of standard "bulb," like fluorescents? IP advantages will play out over time.
  - Infrastructure for SSL: back to the future (i.e., Edison versus Westinghouse). The DC building envelope. One inverter for a house and have a DC system in the house, making a building envelope solution.

***Other comments on state-of-the-art***

- Need to look at epitaxial processes, different substrates for different applications/devices, but underneath is the MOCVD process for all of them. A lot of tools just sold to China. The difference between Tier 1 suppliers for LEDs is knowing how to use the tools.
- Yield is the issue. Better yield and uniformity without having to test every wafer. Headroom in yield and uniformity will eliminate binning and reduce testing.

- U.S. core competency is manufacturing equipment.
- Need to understand and maintain the MOCVD process knowledge.
- MOCVD equipment is ~$12.5 million. Cost of the machines and processes. Takes 8–10 hours for temperature and buffering of the cycle. Spend tremendous amounts of cycle time changing temperature and depositing buffer layers.
- Yield and throughput are issues in the manufacturing process. Push to larger diameter substrate. Manufacturability is the key challenge.
- Don't let *better* be the enemy of good enough.
- Can use ammono process and take growth seed to make a substrate in an hour.
- 500 µm/hour. Combining growth techniques and blending the processes.
- Avoid the need for bulk GaN and buy time.
- Sapphire cost is going down.
- Thermal conductivity of low defect-density bulk GaN 2x better than alternatives.
- CMP: reduced polishing time for SiC by 50x and similar expectations for GaN with trials in progress.
- 1–2 Å diamond layer on 4-inch wafer. Diamond substrates to grow on using a capping process for defects, as well as polishing, etc. Polishing to cap substrate defects. Buffer layer and substrate interface key. Buffer and substrate layers have to improve in order to make advances downstream.
- ALD is an emerging nanocoating process with precise control over film thickness with atomic-scale precision. The process is cheaper than MOCVD or HVPE because of the lower temperature and vacuum operation. Usually get an amorphous (ALD) coating, but a crystal structure is possible via a plasma-enhanced ALD technique. There is the possibility of success for employing ALD to: (1) massively prepare core/shell quantum dot-based phosphors for generating pure white light and (2) make the core/shell nanowire/nanorod LEDs with higher quantum efficiency.

***What would impact in this focus area look like?***

- Phosphors: nanophosphors, rare earth-free work is in development. Doping with S, selenium (Se), telleride (Te) is encouraging for broad spectral response. Need some fundamental work still to develop this. ZnO position is dependent on maybe a mixture of two types of phosphors to get the full spectrum.
- Two photon phosphors are still early stage and require deep science. Fundamental work is needed to understand the potential.
- Nanophosphors are transitioning from basic science to products.
- Solving the "green-gap" issue removes the phosphor issue and creates a new device pathway. Not a manufacturing issue. Could create a huge competitive advantage for the U.S.
- Nanostructuring different materials from PV building layers is a powerful approach that might transfer for this technology.
- **Facilitator:** Where do we add value?
- It is possible to not even deal with "green-gap." Look beyond it. How do we push GaN, or others like GaAs and ZnO, across the visible spectrum? How do you get a highly efficient red emitter in nitrides? Could solve green gap too.
- **Facilitator:** How to drive out cost?
- A manufacturing solution to "green-gap" would be a great win. High cost is still a consumer barrier. Get throughput up, and can compete on the global stage and then get the revenue to do more research and development (R&D) and improve materials. Start selling.
- Not necessarily throughput. More consistency would remove binning.
- Packaging is the largest aspect of cost of the LEDs.

- Bandgap engineering: quantum wells, quantum dots, and one-dimension nanostructures of large sheets of nanorods. Combine with existing materials and processes.
- ZnO lattice constant in desirable range.
- Vapor-phase processes.
- Growth rates of 100 µm/hour or faster. $100 today on 2-inch wafers. 2-inch GaN substrate now, value of Ga, N ~ $5.
- Investment of $1 million could yield 100µm thick InGaN layer.
- Variable lattice constants.
- HVPE.
- Insertion of aluminum (Al) moves system towards indirect bandgap.
- Take nitrides and push them down in terms of energy.
- $10^4$ dislocation densities.
- Reactor modeling.
- Improve yield and throughput and get rid of binning.
- In-situ diagnostics. Need to track 1/2°C tolerances at 900°C.
- Dependence on external sensing loops is indicative of inadequate engineering.
- **Facilitator:** Thermal management is a cross-cutting issue, what is the state-of-art?
    - Life-cycle costs, including replacement and installation cost.
    - Eliminating binning.
    - Sell enough material to generate revenues to support R&D.
    - Bulk of cost in packaging.
    - Thermal droop independent of packaging.
    - Some phosphors color shift with temperature.
    - Packaging, phosphors, and encapsulants.
    - Extended service life costs have to be considered in the design and cost.
- **Facilitator:** Other issues in the balance of the package?
- Need thermally resistant materials. The submount is a critical piece, not so much the substrate as it's not in the thermal path.
- Why 85°C operation?
- Phosphors and thermal droop. Luminaire temperature is not an issue, 70°C. Stokes loss in the phosphor due to heating.
- Soldering, encapsulants, and phosphors are limited in temperature. Phosphors may lose performance with higher temperature. Soldering, encapsulants (i.e., packaging) does get damaged by higher temperatures. For example, tradeoffs for encapsulants, use high index to reduce light piping but less thermally stable.
- Light management and extraction:
    - Chip encapsulant and phosphors need more directional light. High-index encapsulant materials tend to be more temperature sensitive.
    - Need electron confinement, room for WBG material improvement to help with light management and extraction. Stokes losses create heat in phosphors.
    - Light extraction is very efficient. Most commercial are 80%, so the 5–10x cost reduction is not going to be the big hitter. Surface roughening does the job. Not a lot of head room here. Photon extraction, glare avoidance, and surface texturing.
    - Application drives design decisions.
    - Industry solutions must match consumer preferences.
    - Non-WBG problems.
- Lower the current density and change the packaging. Spread the light to reduce the cost. The application will drive the intensity needed.

- There is a possibility of using modeling to combine chemistry with computational fluid dynamics (CFD) to improve the processes and manufacturing processes. We have this for Si, so are there possibilities for WBG? Models are cheaper than experiments, and an integrated part of semiconductor industry.
- Also, in-situ monitoring is an important development as well but there are challenges and the route around it is the design of the tools themselves without monitoring.
- **Facilitator:** What is the state-of-the-art for surface temperature monitoring?
- Pyrometry. This is a high-value problem. Very difficult to solve because you need to monitor the whole epitaxial process. There are a number of MOCVD reactor designs with some more amenable to monitoring. The approach now is to really design the tool to give an improved product without sensors. Sensors just don't work despite all of the theory. If the product is not good, the system is not designed properly. Not feedback control for one deposition.
- Substrates still need work.
- The further down to the final product, the less likely for collaboration because of more IP involvment. Going earlier in the process gives the opportunity to do more in the pre-competitive arena and getting the disruptive technology there.
- Platform, i.e., cross-cutting, LED components.
- Chip-encapsulant-phosphor interface: more directionality.
- External Quantum Efficiency (EQE). AlGaAs, electron and photon confinement. Refractive index works in favor.
- Light extraction above 80% efficient. Good enough?
- Embed photonic crystals to improve extraction.
- Surface roughening also effective.
- Patterned sapphire substrates common.
- Cost issues being addressed incrementally.
- CRI problems have been resolved.
- Eliminate droop by operating at EQE peak.
- Efficient low-current LEDs are available today. Viable low-cost path? If so, why is it not happening?
- Epitaxy is still 1.5x the cost of the substrate. How do you deposit materials cheaply and get them to come out of a system almost ready to go? The fundamental design and process hasn't changed in 15 years. Is there another way to go and another way to look at it? Pushing down technological dead end?
- **Facilitator:** Where are the cross-cutting areas for AMO and the SSL program?
- Cost reduction on the applied side. GaN/GaN and substrates could be cross-cutting beyond SSL; look to power electronics for synergies in substrates and beyond.
- Need semi-insulating for RF. GaN/SiC, still have piezoelectric effect issues and degradation and reliability issues, as well as a need to lower defect density. Still not 100% there. Don't know if the problem is in the substrate or the epitaxy, etc.
- Existing efforts do not necessarily span the full gamut of options.
- Get industry back from China.

## II. SECOND BREAKOUT SESSION

In the second session, the following questions were used to frame further discussion:

- What are the major pathways to identified cost reduction and performance targets?
- What are the highest impact critical technology breakthroughs (game changers) to address gaps?
- Are there "out of the box," risky, or other approaches that should be considered?

### *(1) Power Electronics–Electric Vehicles and Motor Drives*

- The real benefit is for the manufacturer. If you have a mature product, you have to do all-term, long-term testing. In the process, you learn things you never thought would happen. For a drive system, it will lead the 15-year life.
- Potential robustness. You'll find out in the third and fourth year something that you didn't think would happen.
- In industry, data on reliability is not shared, so it is difficult to get an understanding of what makes a device fail. In the U.S., we don't get much in terms of knowledge. If we have a common pool where devices are tested for understanding failure, it could potentially advance the entire pool of knowledge and provide feedback on technology to manufacturers. An IP solution could be firewalling between organizations where government plays an honest broker-type role.
- Failure mechanism and having the right tools to debug.
- We have to build up infrastructure. We can't have multiple pieces in multiple locations. Communication has to exist, however, between them.
- Can be tricky because companies don't want to share their cycle of testing.
- Need a solution. What if a company does own the failure analysis? Many companies would be ready to make an investment.
- Companies have to have a benefit and have to like the model.
- There should be a survey of what there is already out there, such as TARDEC at Detroit. TARDEC is also conveniently located near automakers.
- JEDEC is not good enough, so we overdesign so it won't fail. Every customer goes to their own tester that they consider proprietary, which adds a lot of cost to high-volume applications.
- A modified JEDEC test for SiC or GaN would clear up a lot of issues for manufacturing, customer side.
- Part of reliability is real understanding of mechanisms of failure. Has to be more than testing and analysis pool. Have to bring physical insight into situation.
- **Facilitator:** What are your thoughts on gate drives for WBG? A big barrier is that there are a fewer number of vendors that know how to build these devices. We have individual companies that build proprietary technologies. Would it be beneficial to have a platform for sharing information?
- What's lacking is sharing of information in the U.S. Publication cannot be only motivation.
- DARPA, for example, provides funds to universities and others to buy early-stage components. The resources then become a shared resource. You pay for devices at a low cost. This creates a small market for early devices. Don't have to be fully qualified for reliability and performance. This creates a knowledge base to use when building more practical devices/systems.
- **Facilitator:** Once suppliers are involved, IP is wrapped up. How do we protect IP from abroad? What is a suitable sharing mechanism? Could there be a competitive program for building a test bed? Create a standard set of measurements (accepted test bed) for transistors and diodes?
- Create a competition that pulls from entire chain/system and forces to choose partners throughout and share within team to avoid IP issues.

- Previous examples exist of three teams where each team would do its own system equated to a softball tournament with friendly competition. Each company did a whole hybrid system.
- **Facilitator:** How does that help to bring together the industry as a whole?
- If you are a vendor, you want to have more than one customer.
- Combine this with a user facility and a resident tech to educate each team. To exercise the whole thing. Don't share information into the true public domain.
- **Facilitator:** What is a pre-competitive model?
- The user facility will see everyone's problems so they can translate to all teams and educate others who haven't participated.
- Multiple excellence centers.
- Metals Supportability Initiative could be a potential model.
- Can't be short term. This type of a center would need long-term support.
- Are there enough commercial devices at this point to populate a center?
- **Facilitator:** Can slightly tweak with earlier devices too. Small number of people that can succeed in designing high switching frequency devices. Most people can't take full advantage of these systems.
- **Facilitator:** Passive components. We are 5–6 years behind investment compared to state-of-the-art switches. For example, if you want to buy a 5 MW inductive transformer, no vendor exists with a few percent loss. You could have a university build it. What do you do? No one even has a prototype to demonstrate.
- Getting high-frequency magnetics is trial and error.
- Integrated magnetics is further along. When you get to kW scale, need materials to get better. We need to make a collective investment, but it's at another scale. Will be a bottleneck for all these systems. It's on a different timeline at this point. Could make the case that you need to accelerate the timeline and coordinate efforts further.
- For performance targets, we need to figure out how to use these systems. Systems work needs to be done first to figure out the combination.
- Need at-scale power device.
- We are going to do certain functions with WBG and certain with Si. That is what we have to figure out. What is the best combination?
- Where's the gap to make that determination?
- The gap is doing the work on the systems side. There is a lot of analysis on what the devices are. OEMs need device data, which they get now through the labs. It would be better if there were a wider base to characterize the topology for the best way to use them, i.e., balance of systems. Efficiency, cost, reliability, packaging. If it helps me package, it might go all WBG in that component. We need a lot of learning on how and when to use devices and how to match up to a vehicle (i.e., drive cycle).
- There are still barriers on application needs. What is best?
- A better base for device characteristics.
- Toyota is already making devices to go through the process with SiC, including figuring out parasitics, gate drives, and how they ripple through the system.
- **Facilitator:** Can DOE help to refine knowledge around value proposition and learning?
- To determine the value proposition, you need to build up the base. The Japanese government has put some money into what Nissan is doing. They (Japan) divide up what they are interested in.
- What laboratories do needs more of a tie to automotive to prove to automakers. We can do drive cycle simulations for example. You may have to drive differently (i.e., actively slow down). What's the operating strategy?
- **Facilitator:** Is that easier for a DC/DC converter than for an inverter?
- Yes.
- Novel device architecture process through manufacture or design for cost reduction.

- **Facilitator:** Sunshot has a cost target. Can we do that here? We know what it needs to be for an inverter (i.e., match Si).
- We can possibly leave it to the team to learn how to match targets.
- Two possible ways are: (1) maintain freedom to meet targets or (2) let the cost target be related to device architecture.
- **Facilitator:** Temperature requires 140$^{o}$C underhood ambient. What are other standards/benchmarks?
- Power level for DC/DC converter is 1.8-2.2 kW and can do cooling with GaN.
- Through ARPA-E funding, there are two projects on bidirectional switches at 4 kW where one is air-cooled. It is definitely possible to do air-cooled and simultaneously make them smaller by eliminating magnetics and making them more efficient.
- Cost targets are dependent on volume and manufacturability.
- **Facilitator:** Sunshot and battery programs have tight cost targets. The goal is to measure the cost target against those references. You could embed that mechanism. The National Renewable Energy Laboratory (NREL) models were part of the Sunshot kick-off.
- Development of cost models could start with DC/DC converters and/or chargers to drive and target development.
- Specifications: 600 V typical for automotive rating. The Japanese automakers are at 1,200 V. What is the reason? They're pushing to higher voltage because of boost converter.
- Safety design built in on voltage. This can be done through circuit-related innovation. No reason to choose 600 V or 1,200 V; instead, ask what is the system requirement and choose depending on the application.
- Push voltage, frequency, and temperature. Every auto customer has a different answer. What is the best direction?
- This also applies to current. It can be a mysterious number. Is it device rating or operating?
- The reason you see all these voltage and current ratings is that it always comes down to the application. The battery is the 800 pound gorilla in cost and is a big driver. The space allocated for the motor is the other thing. These two have to fit the architecture. The power electronics is the last piece. Must provide yourself as much flexibility as possible, because it will be a bumpy road until there is enough volume to design dedicated systems.
- If the power train is the big payoff, is this something that DOE could focus on?
- You need data to drive decisions on devices selected and to convince executives.
- Uncertainty of topology.
- Do we go back to improvements in materials and devices? From a manufacturing effort, is there work to be done to improve materials for predictive output? Is it too wide to understand? Do we need to go back to basics? Is there inherent variability that we should focus on rather than device redesigning? Is there annealing/processing to bring down to Si?
- The goal should be to challenge processes to get narrow distributions like Si. Otherwise, you over design on a sketchy model. We need to build better fundamental knowledge.
- **Facilitator:** Summarizing, three main discussion threads have emerged:
  (1) Investigating fundamental reliability where federal government underwrites long-term study coupled with physics of failure analysis. Connecting physics of failure.
  (2) Developing a consortium model with IP sharing where groups come together to build the knowledge base, e.g., learning how to build a gate driver. Being able to improve the knowledge base and facilitate knowledge sharing with users.
  (3) Using vertically integrated systems teams (materials, devices, circuits) to drive down costs, such as charger and traction drive with a goal of demonstration or production.
- DOD investment in demonstration has worked, but there is an insufficient supply base, which can make the demonstration fall short. Well-defined cost targets would assist.
- Teams would want to partner with someone who will take it to production.

- Maybe the user facility is where it is fabricated.
- Partnering with longer term vision is necessary.
- **Facilitator:** Which of these three is more near term?
- A consortium model will help people learn about devices, whereas a physics-of-failure analysis will take more time.
- **Facilitator:** What is the biggest problem?
- From the customer side, understanding the value and how it can be optimized. The reliability issue can change with changes in device design and architecture. You need to understand value proposition first before you can get to reliability data.
- One suggestion is to build from the WBG DOD roadmap for high power and RF with a converter and inverter track. The first task is to get material to a manufacturable point. The second task should be more integration, hemps, and amplifiers.
- **Facilitator:** The DOD case is different because the customer knew what they wanted.
- Two possible modes: (1) drive development of a technology roadmap to accomplish Si cost parity, regardless of vehicle (defects, materials, etc.) and (2) convince yourself that there is enough value even though it's not at cost parity. The disadvantage right now is that competitors are already putting in WBG components and understanding this as they go, so they will be ahead of U.S. automakers.
- We can't just do a demonstration. Need to be committed to production at full scale.
- The consortium model needs to be in place before implementing the vertically integrated team approach.
- Value proposition should be defined upfront.
- Each OEM will need to do its own value proposition.
- **Facilitator:** Can we make a superset of metrics?
- Overall traction system costs are needed to determine whether we can meet or beat them.

## (2) Power Electronics–Grid Integration and High Voltage

*During the second session, this breakout group shared the remaining presentations prepared for the first session.*

***Presentations (continued)***

- **Presentation #4**
  - Need to think about market drivers.
  - Market volume is not sufficient to command continued investments. Power market is extremely segmented.
  - We need to look at the whole range of voltages and applications. You can build it and it might sit on the shelf if there is no real market for it.
  - SiC is a robust material, but look at new market entrants. Opportunities for new materials such as GaN, diamond, etc.
  - Lateral high electron mobility transistor (HEMT) devices are well known and there are opportunities for GaN. The debate is what it should be on: Si, GaN, SiC, diamond, or sapphire?
  - GaN on Si has Japanese companies funding more than DOE.
  - Adiabatic thermal limits and reliability issues. There are opportunities for surface engineering. When and at what cost is it sufficient? Need to think about scalability. Need to ask market-relevant questions.
  - Alternate crystal growth methods, 3C-polytypes, etc.

  - Think about majority versus minority type devices. There are many options such as different materials or growth methods. Advocate an even playing field for technologies. I believe that if GaN is done right, it will have many advantages and opportunities.
  - **Question:** Is it a new advantage or a substitute? 20µm is one aspect, but what are the implications? What is the market size for the HV applications?
  - **Question:** What are the manufacturing challenges?
  - Wafer transfer.
  - **Question:** Are there other ideas?
  - Large surface area is a fundamental need across the spectrum. High growth rate is a good technology across.
  - Capital equipment utilization.
  - GaN is grown at a lower temperature than SiC, which provides advantages.
  - If possible to leverage 2D gas with 10 kV blocking.
  - Superjunctions are an opportunity to think outside the box.
  - Performance is always desired.
  - Mobility can be traded off with yield. Is performance good enough?
  - Need to think about the short circuit constraints.
  - SiC market growth rate is 70% for diode, not switch.
  - Federal investment prompts the market growth.
  - There are opportunities for DC offshore wind and power electronic devices.
  - **Question:** How do you make sure the timing is correct?
  - The future grid will have more power electronics. Window can favor Si IGBT or SiC can make the wave. There are green-field markets in China, but there are brown-field applications domestically.
  - Need to think about new market opportunities and not just replace existing technology.
  - Building blocks are needed that can be applied to wind, ships, etc.; we always need to address reliability and cost.
  - Focus on new processes or on helping to adopt into products. There are different manufacturing challenges across the supply chain. Fundamental limitations of failure.

- **Presentation #5**
  - Bulk conduction semi-insulating devices. Very high-power electronics MV, MA. How do you switch such devices?
  - The field in a junction device drops across the depletion region. A WBG bulk device behaves more like a transconductance device. Can optically pump to generate carriers. Turn on with optical energy.
  - Can think about power gain, optical power in and controlled power out.
  - New lasers with higher efficiencies show much greater increase in power gains.
  - Stackable because they are optically driven.
  - Optical junction device behavior, active gate control. Doesn't latch up, not enough energy gain to cause breakdown.
  - System benefits of optical switching: will not short out to control. It will make system simpler.
  - There has been an optical thyristor in Si for ages. There is latch up with Si.
  - Need to factor on-state losses.
  - Devices based on recombination times. SiC is mature but GaN has fast recombination time.
  - Not really out of the box.
  - Direct optical triggering: (1) electrical-thermal-optical, (2) direct switching, and (3) enhance gain of devices.
  - **Question:** Is there an opportunity for HV and fast switching?

- IGBT and MOSFET is what people want. Are latching and optical desirable? Light triggered thyristors are used in generation.
- Need benchmarks and comparisons; the control and simple gate drives are opportunities.
- May be a disadvantage due to existing methods and paradigms.
- Defects and epitaxy are common issues.

- **Presentation #6**
  - Reliability, adiabatic limit.
  - State-of-the-art graph representation with on current and blocking voltage when off. A corner is chopped off due to thermal issues.
  - Cost is also important.
  - Current density for reliable switching >200 A/cm$^2$, defect density <100/cm$^2$, maximum junction temperature ($T_{jmax}$) >200$^o$C.
  - Si can do 150$^o$C.
  - It is not just the chip, but the module. Need to relate defect density and reliability, cost, yield of the system.
  - Need to find and establish metrics.
  - As frequency increases, the state-of-art keeps shrinking. More heat occurs for a given volume.
  - Three key metrics to think about manufacturing: (1) junction temperature, (2) defects, and (3) reliable current density.
  - Technology has led the science.
  - LEDs and power electronics are different.
  - Need to address fundamentals before manufacturing can be overcome. Need metrology.
  - Schottky diode failure is lower than Si but defects aren't as good.
  - Defects may not directly relate to reliability.
  - BPD are known to impact. There has been a good deal of work on understanding defects and electrical properties. This is important, but not entirely unknown. BPD is almost solved, proper technology for epitaxial growth.
  - Threading dislocations are less of a concern. There is an ongoing need, but may not be a fundamental limit.
  - Bipolar devices are a concern, but not a deal breaker.
  - By getting rid of 1C's, you can get closer to the edge. Can be a problem at higher voltages but can engineer around it.
  - Impact is on performance but not necessarily on reliability. There is a cost implication. Need to think about system reliability. Have good knowledge of reliability on devices at 700 V and below, but less so on higher voltages.
  - There is a difference between manufacturing reliability and design reliability. Design issues that impact reliability deal with hot spots. Need to factor in the lifetime of devices.
  - Opportunities for new epitaxy processes for control of thickness, doping, etc.
  - New precursors and other activities.
  - **Question:** How high of voltage can we get with SiC switches or GaN?
  - SiC has been demonstrated at 17 kV.
  - **Question:** How high do we need?
  - 25 kV is achievable, 40 kV.
  - **Question:** How thick can the epitaxy be?
  - Fabless capabilities are new for MEMS.
  - **Question:** Can you separate design and fabrication?
  - Leverage national lab capabilities to complement, not compete with, private sector.
  - Possibly unique process steps.
  - Cost is cost of the system, not just the device.

- o Larger dies are a good goal due to parasitics of control.
- o Unit processes, defects. Desired for full wafer devices, Japan proposed 300 A devices.
- o Manufacturing process, yield, and sizes.
- o Companies want reliability.
- o Compete with Si conditions.
- o Die size, cost, defect density, voltage, current, and reliability.

## (3) Solid-State Lighting

***Targets***

- 1°C results in 5 nm wavelength shift in the LED.
- Improved yield. Modest "bump" in uniformity of the wafer gives more LEDs for high brightness.
- Bulk GaN with 4- to 8-inch wafers, 150–200 mm, and defect densities $<10^4$.
- Multi-physics and multi-scale models.
- RF devices. Substrate must be semi-insulating.
- Physics of degradation and gate drives.
- Design out defects in the start. The wafers are bowed so you don't get thermal consistency. Other issues have been designed out. Modeling can help with the prediction of stresses and thermal uniformity used in reactor design. Model the process, thermal and flow gradients, etc.
- Also need to model the impact of the cost structure for the LED.
- Could deal with the increase in the substrate cost if you can get more out of the wafer.
- Practical GaN/GaN for LED is good. For other applications, you need to make the size of the substrate at least 4-inch.
- Substrates. Make better epitaxial wafers faster and cheaper.

***Out of the Box***

- Use photonic crystals not for light extraction but to increase the rate of spontaneous emission, and alter density of states. Photonic crystals, lattices, to increase radiative recombination rate. Engineering the optical density of states, higher efficiency. Competition between radiative and non-radiative emissions; we want radiative faster, internal quantum efficiency (IQE) 90% except for "green." This has been used in the laser area.
- Use of lasers for SSL devices rather than spontaneous devices. Carrier density clamps are used once you reach a limit. RYGB four laser colors, possible to get color rendering, do get speckle, as an initial experiment. RYGB or laser-pumped phosphor are used for projectors, why not for lighting?
- Processes:
  - o What is something you can do to Si to make it a better material from MOCVD? To make GaN grow on top better (have diameter and cost structure for Si), nanostructure on the microstructure. Zero defect density is not the target.
  - o MOCVD has massive issues, low throughput, high cost, and high footprint. What are some other processes that can be used? Can HVPE do the process?
- Nano- and mesoscale structures through bandgap engineering. Need other ways of managing stress, i.e., intermediate layer of nanorods or nanocolumns. Nanostructures can change the bandgap of the material; can change radiative recombination, i.e., transport properties; and can prevent nonradiative recombination. Example, GaN nanowires with InGaN layer on top to accommodate lattice strain.

- Substrates. "Universal substrate": $Al_2O_3$ layer on top of the sapphire using ALD. Other possibilities for substrates. Alternative substrate technologies. What would allow you to bridge the gap and make different compositions? Have to stabilize oxide substrates in a highly reductive environment to protect them. ALD is self-limiting, 1 monolayer at a time, very slow, need 10–20 nm of sapphire with GaN on top. There are improvements in ALD for speed and volume. Atomic layer for epitaxial growth.
- How do you get In into the nitride materials in high enough concentrations? Make a platform technology and have materials for optoelectronics as well as LED?
- Bulk In for substrates.
- Incorporating non-linear materials, at least two photons.
- Thermal management. Pump current through the layers to create cooling to control temperature. In-situ cooling. Make other functional components, such as active cooling of the packaging. GaN materials for active cooling/buffer layer or communications. Microchannel cooling and diamond. Improved thermal conductors, interface materials, and active cooling.
- Additional functionality in LEDs: communications, MEMS integration, directional control, and color tuning.
- Get rid of phosphors. Embed something else in phosphor-free device that gives the broadband emissions and integrate phosphor-like materials into the two-terminal device.
- Quantum dot phosphor replacements done with Cd, non-Cd quantum dots—rare earth mitigation and novel phosphors.

## III. THIRD BREAKOUT SESSION

The final session focused on summarizing the key ideas and takeaways from the previous sessions. The two Power Electronics groups merged to share thoughts and identify common themes.

### *(1) Power Electronics–Electric Vehicle and High Voltage Combined*

- **Facilitator:** What are the common challenges? In HV, price doesn't matter (current density, cost per unit area). How do you drive cost down? It's different for EV, larger areas and higher throughput.
- Near-term with manufacturing and device challenges or long-term new things such as bulk GaN, diamond? Platform ideas?
- **Facilitator:** Where are the opportunity and the gap? New cost metrics? Is there a new growth process? Are there new insights? Do we throw more money to bring cost down?
- Manufacturing maturity is unknown for WBG. Reliability improvements are required throughout the process (i.e., materials through devices), which impact costs, to make it to Si.
- SiC/SiC intrinsically should be more reliable. We need reliability in crystals and epitaxy.
- What problem do we want to fix? Is it a manufacturing or deployment problem?
- It's a portfolio approach.
- We don't know about reliability. Do we really know why they fail?
- There is an opportunity to be more reliable if it is done right. Is there a role for analysis and computation?
- SiC larger wafers are a real opportunity for reducing costs.
- **Facilitator:** Is there a good technoeconomic model for SiC? How does cost come down? Are we asymptotic? No. Is there an opportunity for that kind of modeling for levelized cost of energy (LCOE)?
- For 3-inch (100 mm) wafers, we saw how it impacted cost/yield in price. It will be more so at 4-inch (150 mm) wafers because they will use more Si tools.
- Experience base could be obtained utilizing conventional Si processing tools.
- 6-inch tools with donuts can be used to do 4-inch. We need to go to 6-inch to get higher voltage.
- 8-inch epitaxy has been done. Doing 6-inch is not a fundamental challenge.
- **Facilitator:** To recap so far in the EV session, we talked about:
  (1) User facility to solve some of the reliability for application issues. Identify physics of failure mechanisms and get around long-term lifetime testing through acceleration in a test bed, not SEMATECH. This is more of a manufacturing issue. Think about gate drives and other knowledge gaps that individuals are learning to address on their own.
  (2) Centers of excellence that bring in folks to meet with experts to accelerate level for an industry.
- For GaN/Si for lower voltage applications, can processes be shared?
- **Facilitator:** Not a user facility where processing demonstrations or process information are shown. A facility like MOSIS where reliability shows run and standardized reliability testing is developed. Folks pay fees underwritten by the government. Standard validation and verification is best since processes currently are not fluid enough to have a standard. Every customer and user does things slightly different. Shuttle with people bidding to run. From an OEM perspective, it makes folks uncomfortable when they don't understand fundamental failure mechanisms. Technology leads the science. Having long-term reliability data would be powerful. Devices are approaching maturity; we could envision this.
- Is this a government facility?

- **Facilitator:** Someone bids to run reliability testing. Device-level, material properties with devices, looking at the package and module level. Physics depends on geometry. Need to identify a device, like JEDEC. Vendors and early adopters come up with reasonable tests, with DOE in a convener role. Is there an appetite for a consortium model for WBG? Bridging between OEMs and vendors, like a public-private SEMATECH model? Generate a knowledge base.
- For early technologies, there are no examples of traction drives, for example with SiC. It is still early enough that it could be pre-competitive and good for a consortium. A good reference for this application would be a gate drive.
- On-board chargers and DC/DC converters are low-hanging fruits for near-term applications. Traction drive components are a bigger nut to crack as a value proposition.
- Consortiums to move on pre-competitive issues.
- **Facilitator:** Two most vocal themes: (1) reliability and understanding and (2) establishing the value proposition. Need to diversify and not choose one technology over another. Establishing benchmarks and standards would be more worthwhile. Need a standard for lifetime and an understanding of the physics.
- How would this be different from existing testing work?
- The goal is to do long-term reliability testing against a standard. More likely a relationship from a federally funded activity and manufacturer.
- **Facilitator:** Third theme: Vertically integrated system teams with a specific, fleshed-out system and cost targets. Most direct way to answer establishing the value proposition across the value chain. This is more demonstration than manufacturing.
- The team is made up with people who will make all the parts.
- You have to have a device development track to get performance, but need to also have knowledge on application side.
- How is that not picking winners and losers?
- You need to have enough teams. Different OEMs might have different challenges and issues they want to address, i.e., smaller hybrid, packaging really tight. One manufacturer may want to focus on another vehicle size or type.
- **Facilitator:** You have to have the end goal to pull development out. The entire supply chain to support is important.
- Would the team define itself?
- **Facilitator:** Example, DOE says, "chargers" (example with broad cost targets), but the OEM defines the rest (i.e., the final application). You encourage people to have targets. More like Sunshot with targets than ARPA-E Agile Delivery of Electrical Power Technology (ADEPT) portfolio.
- How big would the award need to be?
- Does the device need to be developed or do we also need to manufacture? Is it more about tuning development?
- **Facilitator:** Why don't we set a timeline that is as equally aggressive as the Japanese OEMs?
- Can we use a 10-year timeframe from the Japanese OEMs as a benchmark?
- **Facilitator:** For each of these scenarios, which requires the least amount of money?
- Consortium needs least amount.
- **Facilitator:** How much is needed from a vertically integrated team to be able to compete in 2017? For reliability, long-term testing, and diving deep into understanding the failure of physics, how much is needed?
- Different technology readiness levels (TRLs) will require different funding levels. Can be an indicator for cost share.
- **Facilitator:** Could we say that for different TRL levels we have different metrics?
- Cost-matching in a consortium, if underwritten, can take away risk. DOE doesn't have to support the entire cost.

- Could we have a Manufacturing Demonstration Facility for GaN/GaN? This would be good for hard-wired loop testing to get to utility scale.
- Once you get to a device with a vertically integrated team, i.e., build up packaging, components entire devices through device testing, a model like this could work. Individual programs, for example, to test a sample converter at certain specifications.
- We can do defect analysis. Few people can afford a center of excellence on their own.
- **Facilitator:** How do we encourage more diversity at different levels? Is there a mechanism at different levels of development?
- Incubator program for early stage, new ideas; not quite Small Business Innovation Research (SBIR), but more of an ARPA-E model to stimulate innovation and diversify players. The problem in the past is we haven't had a critical mass to carve out.
- Need end use drive, not just device manufacturers.
- Need hardware in the loop testing. Control circuitry is needed to take advantage of new properties.
- Changing architecture becomes expensive, but depending on what piece you pick, you don't necessarily have to worry about it.
- Becomes more of an issue if someone wants to incorporate now.

### (2) Solid-State Lighting

- **Facilitator:** Cross-cuts with SSL and power electronics. Where is the link to manufacturing?
- As you improve efficiency, you would remove heat if you don't have a phosphor.
- Epitaxial process is a critical aspect: yield/throughput/consistency of the epitaxial process and improved reactor design.
- Engineered substrates including GaN, InGa, GaN/Si. Use "flip chip" processing for lighting but people are moving away from it, may be because of yield for displays, etc.
- Higher cross-cut importance includes substrates, epitaxial process, and thermal management, important to LED specifically, to improve efficiency across the visible spectrum.

***Major Barriers and Current Gaps***

- Wafer bowing: issue as diameters increase from 6-inch to 8-inch which affects doping control and breakdown voltage. Epitaxial versus substrate thermal expansion, sapphire substrate with the epitaxial layer on top at 1,000°C, cool, and wafer "potato chips."
- Lower defect density is needed.
- Reliability still in question for GaN/SiC.
- Efficiency across the full spectrum.
- Shared cost/impact modeling might be needed to the extent that people would share information.
- Alternative growth techniques.

# APPENDIX A. WORKSHOP AGENDA

| Time (CDT) | Activity | Speaker |
|---|---|---|
| **8:00am-9:00am** | *Registration and Breakfast* | |
| **9:00am-9:05am** | ***Welcome.***<br>*Advanced Manufacturing Office* | Robert Gemmer<br>Advanced Manufacturing Office |
| **9:05am-9:20am** | ***Setting the Stage.***<br>*EERE Thrust in Wide Bandgap Semiconductors for Clean Energy* | David Danielson<br>Assistant Secretary, EERE |
| **9:20am-9:40am** | ***Leveraging Past Government Investments.***<br>*Current State-of-the-Art Technology and Challenges for Wide Bandgap Semiconductors* | Mark Johnson,<br>Advanced Research Projects Agency-Energy |
| **9:40am-9:50am** | *Instructions for Breakout Sessions* | Marina Sofos<br>Advanced Manufacturing Office |
| **9:50am-10:00am** | *Break* | |
| **10:00am-11:55am** | ***Breakout Session #1:*** *(3 groups)*<br>• *Power Electronics (EV & Motor Drives)* Lead: Steve Boyd<br>• *Power Electronics (HV & Grid Integration)* Lead: Mark Johnson<br>• *Optical (Solid-State Lighting)* Lead: Colin McCormick | All Participants<br>*Concurrent Groups* |

Breakout Session #1:
- *Introductions and discussion of current state-of-art of the breakout group's focus area.*
- *What would impact in this focus area look like?*
- *What are the necessary performance and cost targets?*
- *What are the major barriers and current gaps?*

| Time (CDT) | Activity | Speaker |
|---|---|---|
| **11:55am-12:30pm** | *Lunch* | |
| **12:30pm-2:00pm** | ***Breakout Session #2:*** *(3 groups)*<br>• *Power Electronics (EV & Motor Drives)* Lead: Steve Boyd | All Participants<br>*Concurrent Groups* |

- *Power Electronics (HV & Grid Integration)*
  Lead: Mark Johnson

- *Optical (Solid-State Lighting)*
  Lead: Colin McCormick

Breakout #2:
- *What are the major pathways to identified cost reduction and performance targets?*
- *What are the highest-impact critical technology breakthroughs (game changers) to address gaps?*
- *Are there "out of the box", risky, or other approaches that should be considered?*

**2:00pm-2:15pm** *Break*

**2:15pm-3:30pm** ***Breakout Session #3:*** *(3 groups)* — All Participants, *Concurrent Groups*

- *Power Electronics (EV & Motor Drives)*
  Lead: Steve Boyd

- *Power Electronics (HV & Grid Integration)*
  Lead: Mark Johnson

- *Optical (Solid-State Lighting)*
  Lead: Colin McCormick

Breakout #3:
- *Develop action plan of ideas*
- *Prepare slides of major findings*

**3:30pm-3:40pm** *Reassemble* — All Participants

**3:40pm-4:25pm** *Breakout Sessions Report Out/ Question & Answer* — Discussion Leads

**4:25pm-4:30pm** *Closing Remarks*

# APPENDIX B. WORKSHOP PARTICIPANT LIST

**Bunmi Adekore**
RamGoss

**Nisha Agrawal**
ANSER

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# APPENDIX C. ACRONYMS AND ABBREVIATIONS

| | |
|---|---|
| A | ampere |
| Å | angstrom |
| AAAS | American Association for the Advancement of Science |
| ADEPT | Agile Delivery of Electrical Power Technology |
| Al | aluminum |
| ALD | atomic layer deposition |
| AlGaN | aluminum gallium arsenide |
| AlN | aluminum nitride |
| $AlO_2$ | aluminum dioxide |
| AMO | Advanced Manufacturing Office |
| ARPA-E | Advanced Research Projects Agency-Energy |
| BPD | basal plane defect |
| C | carbon |
| °C | degrees Celsius |
| CEC | California Energy Commission |
| Cd | cadmium |
| CFD | computational fluid dynamics |
| cm | centimeter |
| CMP | chemical-mechanical polishing |
| CRI | color rendering index |
| DC | direct current |
| DARPA | Defense Advanced Research Projects Agency |
| DOD | U.S. Department of Defense |
| DOE | U.S. Department of Energy |
| EERE | Office of Energy Efficiency and Renewable Energy |
| EQE | external quantum efficiency |
| Eu | europium |
| EV | electric vehicle |
| FET | field-effect transistor |
| Ga | gallium |
| GaAs | gallium arsenide |
| GaN | gallium nitride |
| GTO | gate turn off |
| H | hydrogen |
| HEMT | high electron mobility transistor |
| HV | high voltage |
| HVPE | hydride vapor phase epitaxy |
| Hz | hertz |
| IGBT | insulated-gate bipolar transistor |
| In | indium |
| InGaN | indium gallium nitride |
| IP | intellectual property |
| IQE | internal quantum efficiency |
| ITRS | International Technology Roadmap for Semiconductors |
| JBS | junction barrier Schottky |
| JEDEC | Joint Electron Devices Engineering Council |
| JFET | junction field-effect transistor |
| kHz | kilohertz |

| | |
|---|---|
| kV | kilovolt |
| LCOE | levelized cost of energy |
| LED | light-emitting diode |
| lm | lumens |
| LPE | liquid phase epitaxy |
| LV | low voltage |
| MEMS | microelectromechanical systems |
| Mg | magnesium |
| mm | millimeter |
| MOCVD | metal organic chemical vapor deposition |
| MOS | metal-oxide-semiconductor |
| MOSFET | metal-oxide–semiconductor field-effect transistor |
| MOSIS | Metal Oxide Semiconductor Implementation Service |
| MV | megavolt |
| MW | megawatt |
| N | nitride |
| nm | nanometer |
| NREL | National Renewable Energy Laboratory |
| O | oxygen |
| OEM | original equipment manufacturer |
| PSS | patterned sapphire substrate |
| PV | photovoltaic |
| R&D | research and development |
| RF | radio frequency |
| $R_{ON}$ | on resistance |
| RYGB | red yellow green blue |
| S | sulfur |
| SBIR | Small Business Innovation Research |
| Se | selenium |
| SEGIS | Solar Energy Grid Integration Systems |
| SEMATECH | Semiconductor Manufacturing Technology |
| SJ-MOSFET | super junction metal-oxide-semiconductor field-effect transistor |
| Si | silicon |
| SiC | silicon carbide |
| $SiO_2$ | silicon dioxide |
| SOI | silicon on insulator |
| SSL | solid-state lighting |
| SST | solid-state transformer |
| TARDEC | U.S. Army Tank Automotive Research, Development and Engineering Center |
| Te | telleride |
| TRL | technology readiness level |
| UMOSFET | U-shape metal-oxide-semiconductor field-effect transistor |
| V | volt |
| VJFET | vertical junction field-effect transistor |
| W | watts |
| WBG | wide bandgap semiconductor |
| ZnO | zinc oxide |
| 2D | two-dimension |
| $\lambda$ | wavelength |
| $\mu m$ | micrometer |

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Summary Report

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