Breakage Mechanism(s) of Photovoltaic Silicon Wafers: Theory and Experiment

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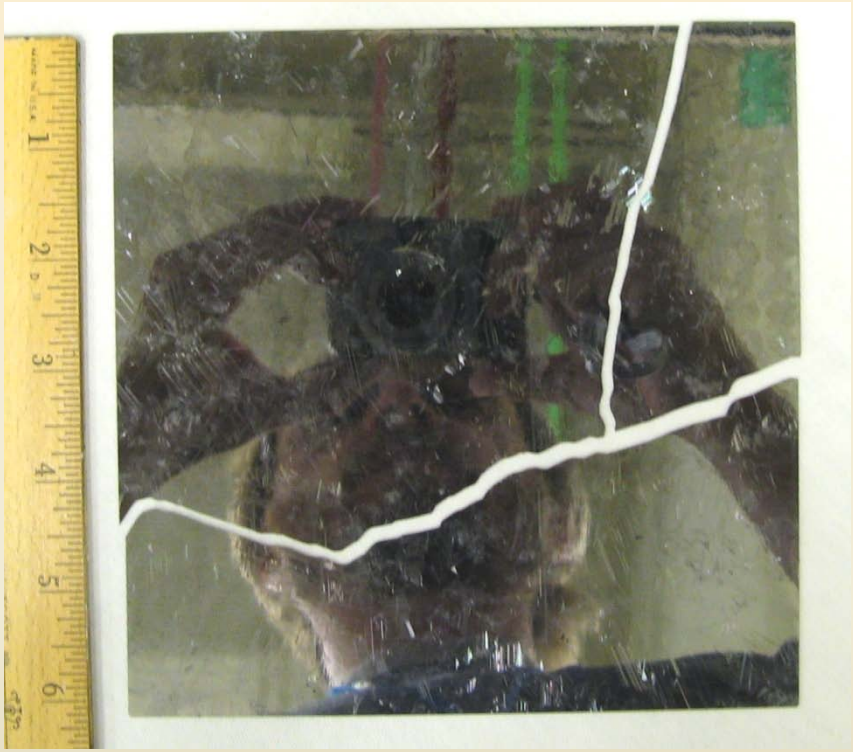
Introduction

- Wafer breakage is a serious problem in the photovoltaic industry, particularly for “thinner” wafers.
- 5-10% of the wafers break during cell/module fabrication
- Value of a wafer increases with number of process steps it undergoes.
- A detailed study of mechanisms of wafer failure & possibly solution(s) is needed.



wafer thickness 200µm

Why do wafers break?

- Wafer handling
- Structure of the device — for example asymmetry in the device configuration due to depositions of dielectric and/or metallic thin films can cause wafer loading
- Device processing —stresses induced by thermal treatments or rapid thermal processing, laser cutting, during cell encapsulation, and module operation

The critical stress (σ_c) for Si > 100 MPa

Wafer breakage is not a major problem in μ-electronics industry

Strength of a wafer is lowered by the presence of microcracks and other defects

μ-cracks $\Rightarrow$ *Result of incomplete saw-damage removal, rough or texturing, edge geometry*

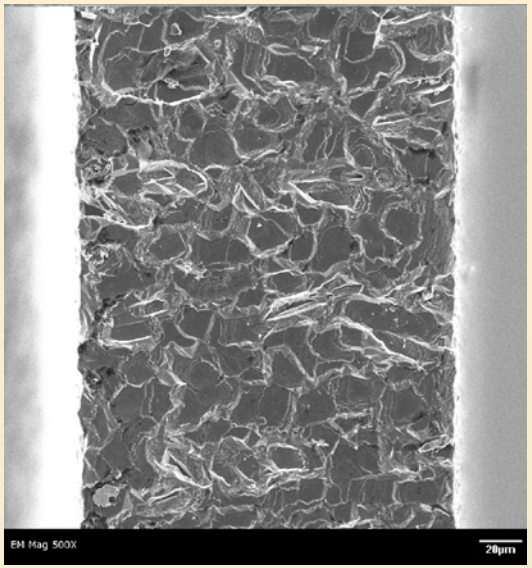
OUTLINE

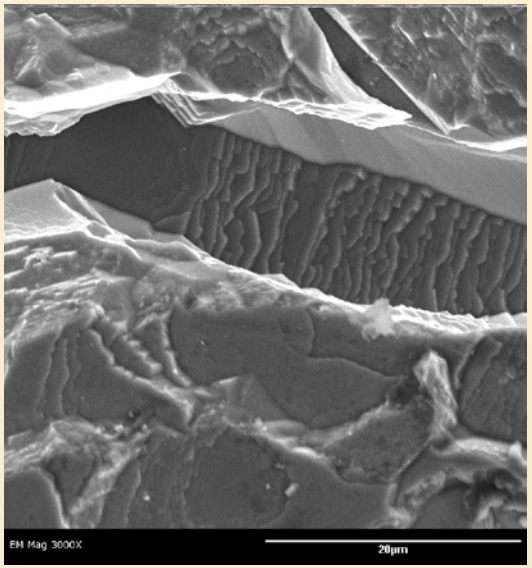
- *A brief summary of our modeling results on the effects of μ-crack(s)*

  ⇒ surface and near the edge
- *Effect of randomly distributed μ-cracks on the strength of a wafer*
- *A wafer screening technique*

(detection of μ–cracks alone is not enough because different process conditions can tolerate different density/size of cracks)

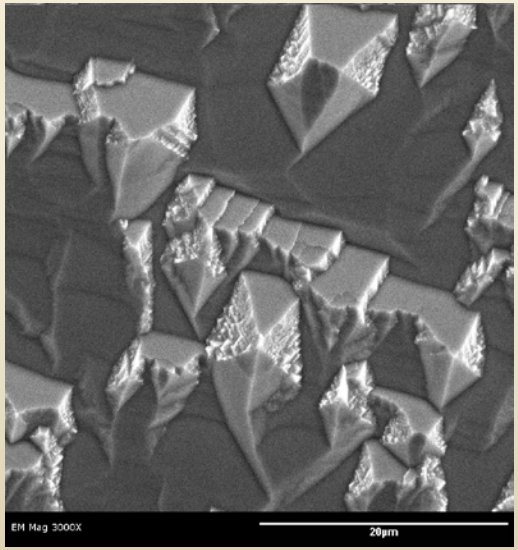
- *Conclusions: comments on breakage in cell processing and in the module*

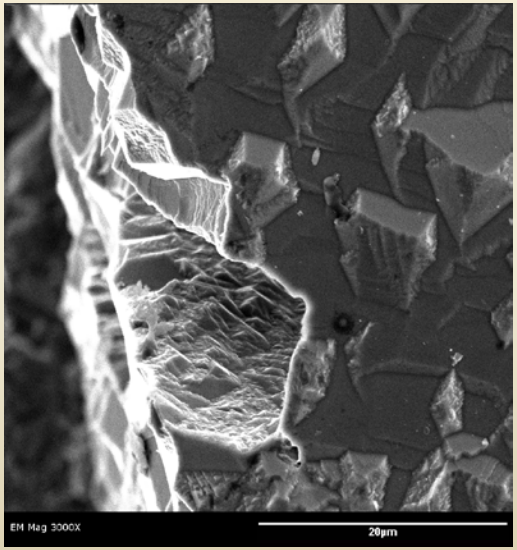




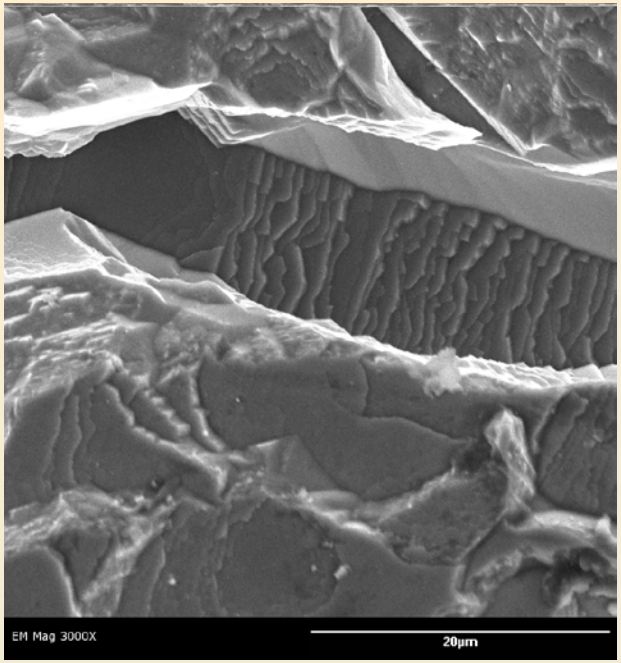
← Wafer edge

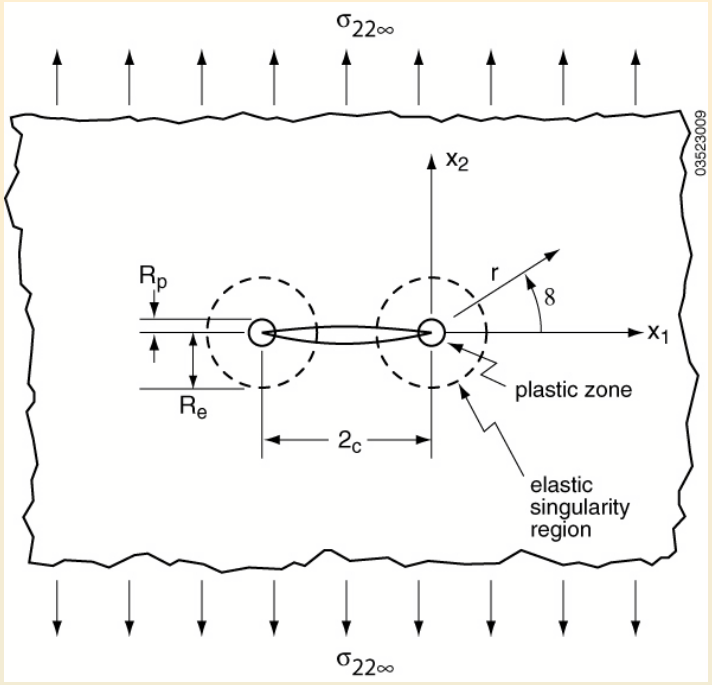
SEM images of a Si wafer after standard saw damage removal





← Wafer surface





The breaking strength in tension due to a microcrack of length 2c

$\sigma c = (2\gamma E/ \pi c)1/2$

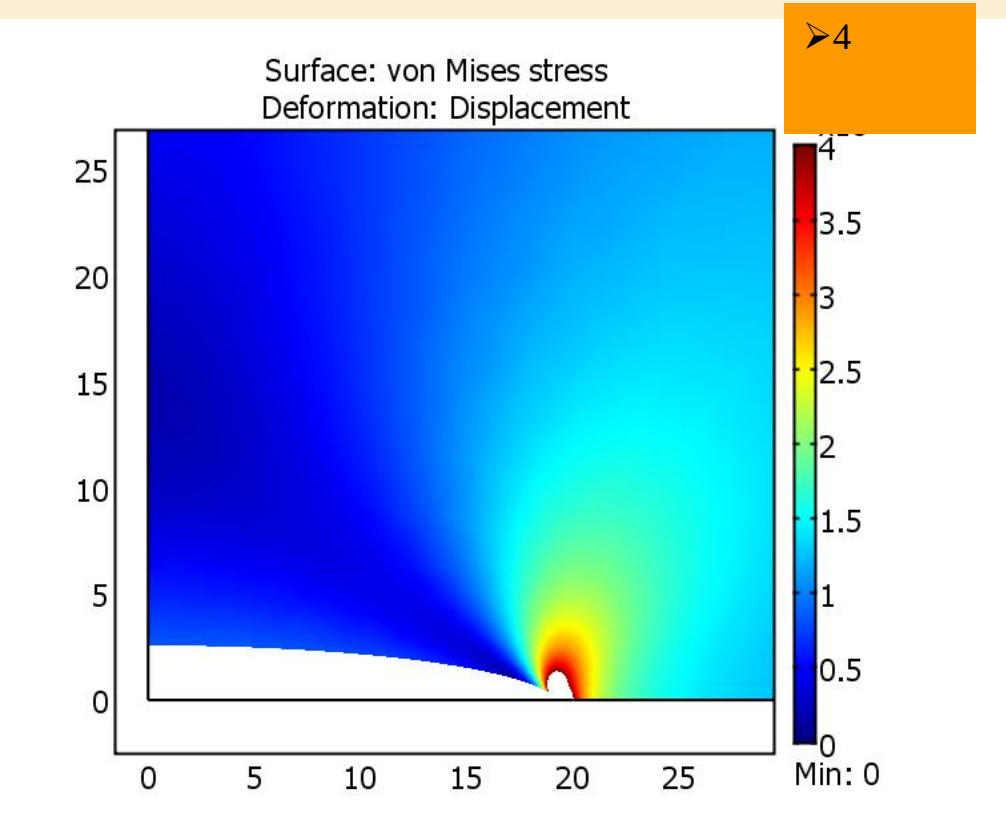
Here, γ is the specific surface energy of the material, E is the Young's modulus. This expression can be approximated as:

$\sigma c \sim [E /20] \times (a /c)1/2$

a is the atomic radius

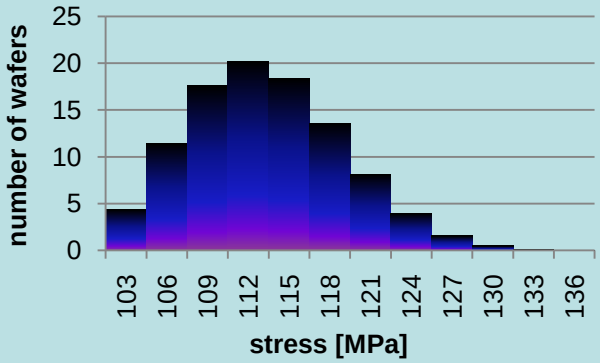
Strength of PV wafer – effect of flaws

- Silicon at room temperature is very brittle
- Its strength is limited by structural imperfections
  - micro cracks
  - voids
  - grain boundaries
  - dislocation networks
  - precipitated impurities
- The imperfections serve as stress concentrators and crack nucleation spots.
- In the vicinity of defects the stresses can be much higher than the load applied to a sample.



Strength of PV wafer – can we describe it?

- Classical approach for brittle materials
  - Relates the strength of a specimen to its volume
  - Probability that a wafer survives load σ is given by Weibull distribution :



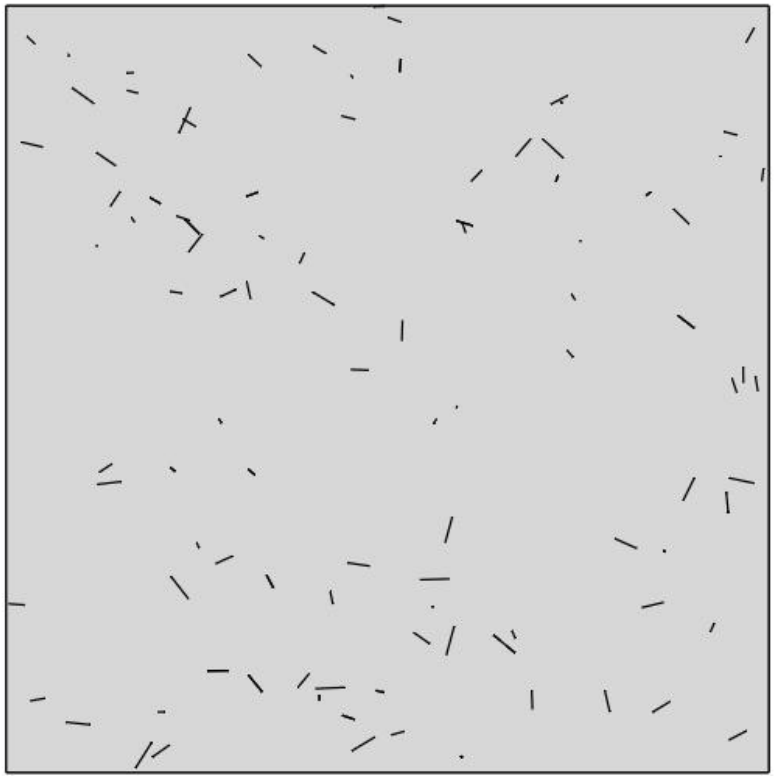
$$F_V(\sigma) = \exp\left(-\int_V \left(\frac{\sigma - \gamma_V}{\alpha_V} \right)^{\omega_V} dV \right)$$

  - γ_V, α_V and ω_V are the three parameters of Weibull distribution.
  - Non-uniform stress is handled.
  - In the case of multi-axial stress, regard σ as a position dependent effective stress.

- The model of PV wafer needs to be extended so that the surface and edge effects are taken into account.

Monte Carlo simulations - method

- To perform MC simulations we virtually generate a set of 100 wafers.
- Each wafer contains 100 surface cracks (50 on each side), which are randomly distributed and oriented.
- Maximum load for each wafer is calculated using fracture mechanics method combined with the weakest link principle.
- Statisticaly analyze the results for all 100 wafers to obtain the strength distribution.
- Determine if Weibull distribution can accurately fit the obtained results and we find the corresponding Weibull parameters.



Example of wafer with cracks used in MC simulation.
For legibility the cracks are magnified 20 times.

Monte Carlo simulations - assumptions

a) Surface energy of silicon, γ_0, equals to 2.475 J/m^2 and density of subsurface micro-cracks is 0.32/cm^2.

b) The cracks are of semi-elliptical shape and the crack plane is perpendicular to the wafer surface.

c) The size of cracks varies randomly within the specified ranges: the length, *L*, from 0 to 200 μm and the depth, *D*, from 0 to 20 μm.

d) We also assume that entire wafer fractures once a single crack starts to propagate.

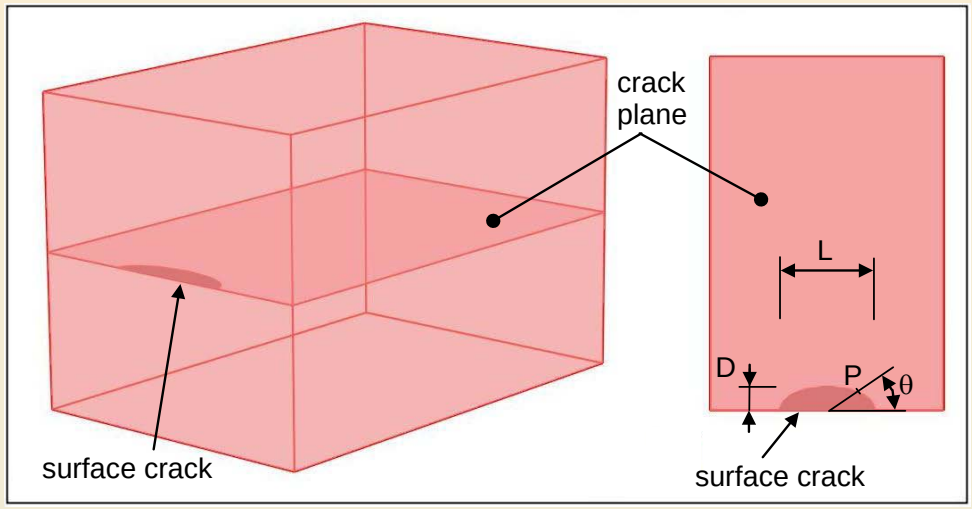
e) The entire system is linearly-elastic.

f) The cracks interact neither with the wafer edge nor with each other.

Fracture Mechanics modeling

- Stability of each crack can be analyzed separately (no interaction).
- To predict the ultimate load for a wafer with one crack we apply the fracture mechanical computations based on gamma integrals and finite element method.
- Empirical relations for surface cracks are available only for some special cases. We need to use finite element method (any orientation, any loads).

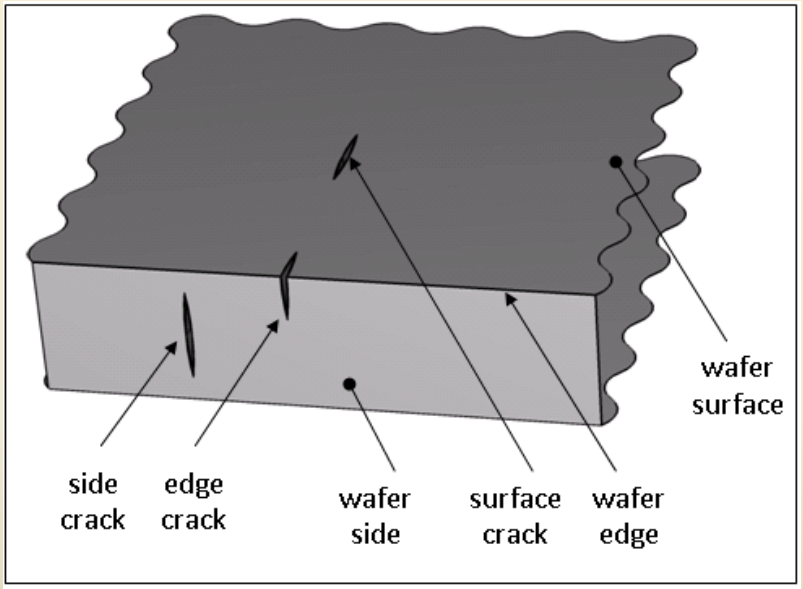
Fracture Mechanics modeling - methods



A geometrical representation of a semi-elliptical surface crack

1. Stresses, σ_{ij}, strains, ε_{ij}, and displacements, u_i, are obtained using FEM.
2. Energy release rate vector, Γ_k, is computed as a function of angle θ.
3. Finally, the strength of a wafer is determined using fact that Γ_k is proportional to σ^2.

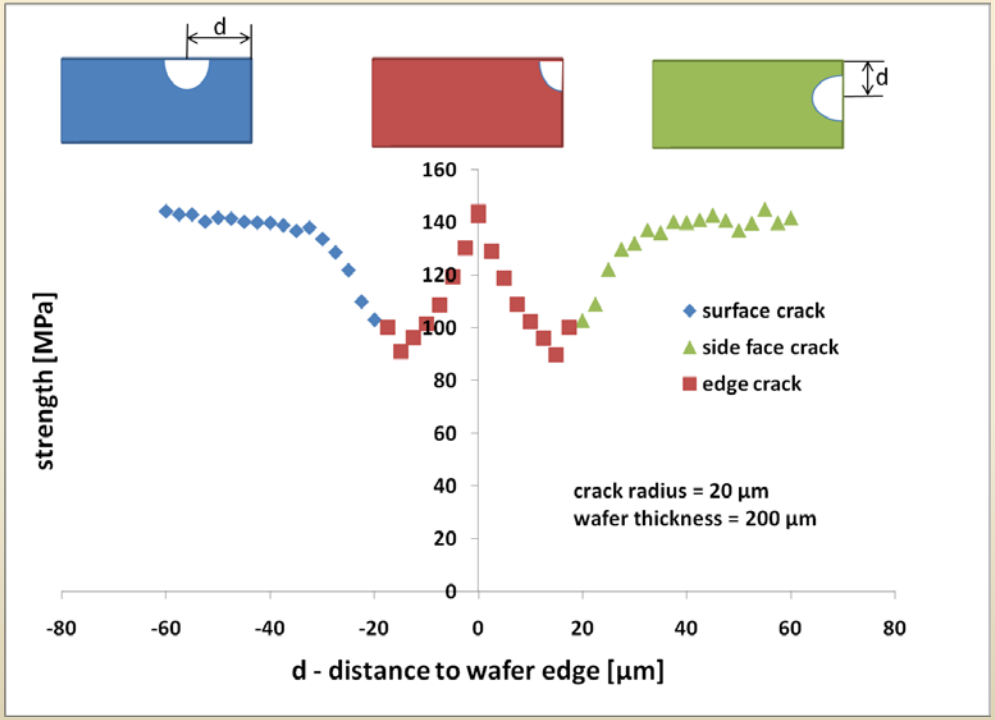
Surface, edge and side cracks.



- The type of stress concentrators is dictated by the wafer manufacturing process
- As a result of sawing, the main stress concentrators take the form of microcracks
- The wafer strength is directly related to the density, location, orientation, shape, and size of these microcracks

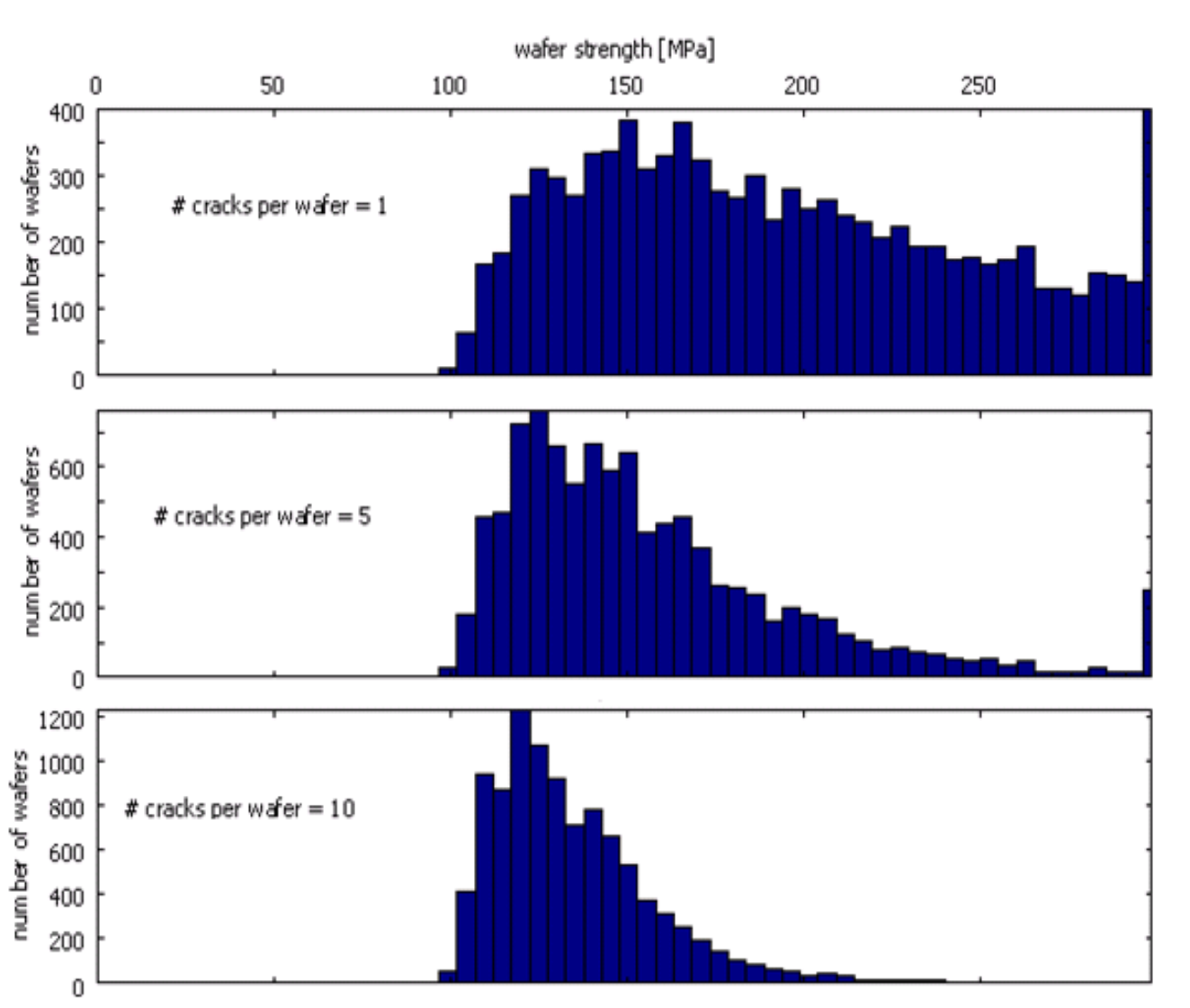
Strength of a wafer with a single surface edge and side crack

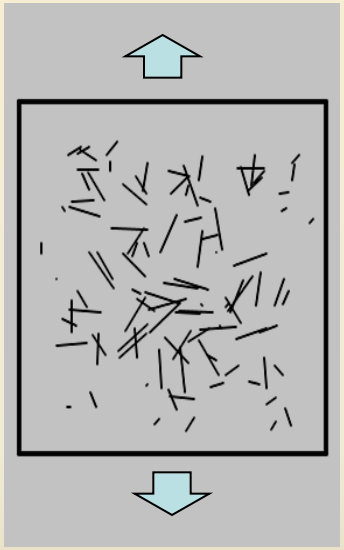
Strength was computed as a function of distance from the wafer edge to the center of the crack.



- Surface crack far away from the wafer edge =>
  - strength = ~140 MPa (constant)
- Crack moved closer to the wafer edge =>
  - strength drops to 90 MPa
- Side crack behaves like surface crack
  - reason: crack radius << wafer thickness

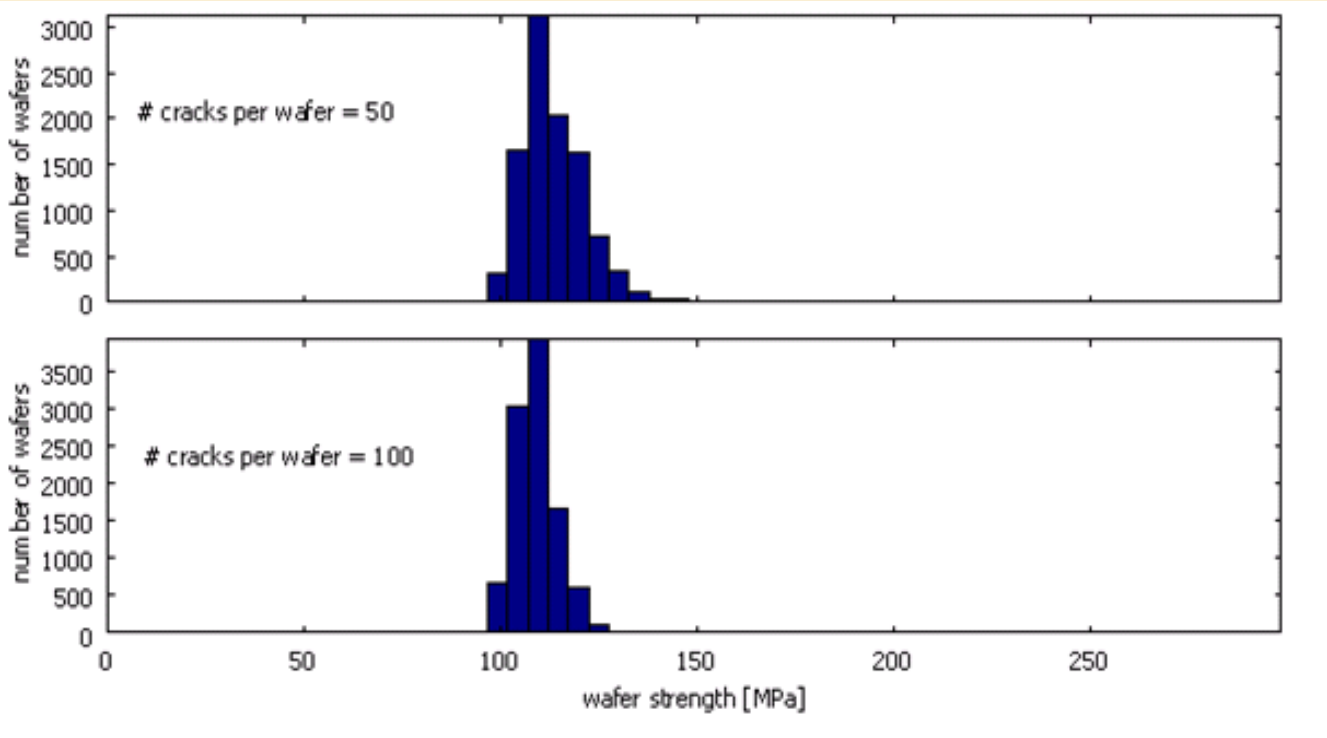
Cracks located far away from wafer edge





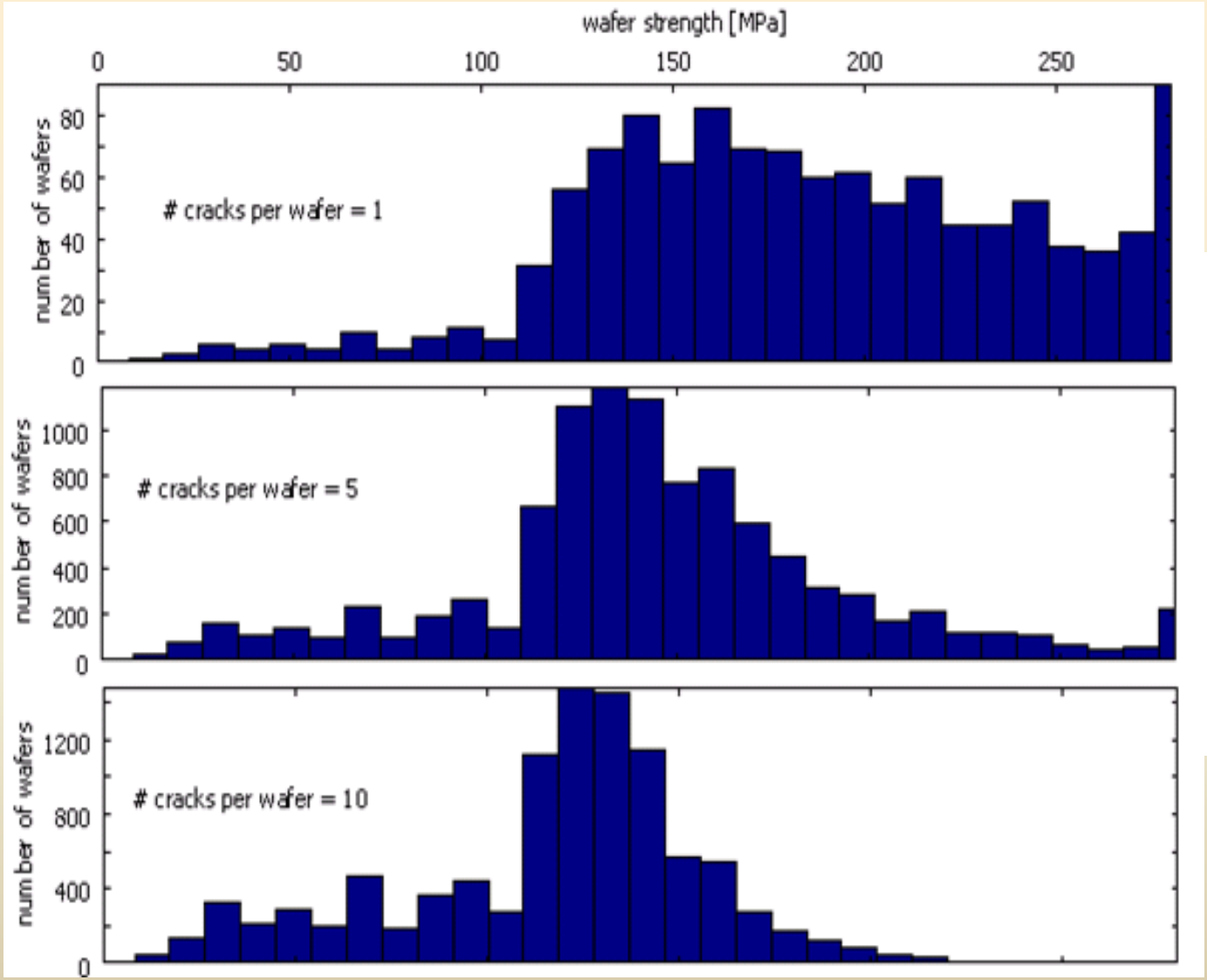
Cracks in the figure are magnified 100 times

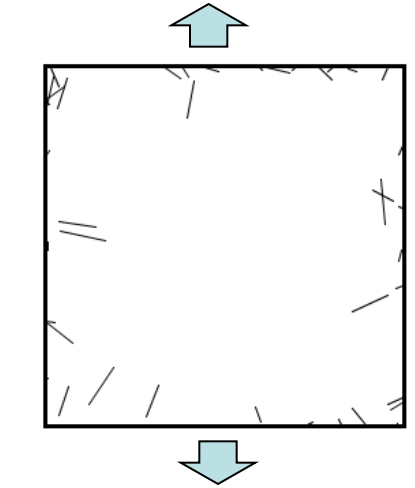
Cracks located far away from wafer edge - continued



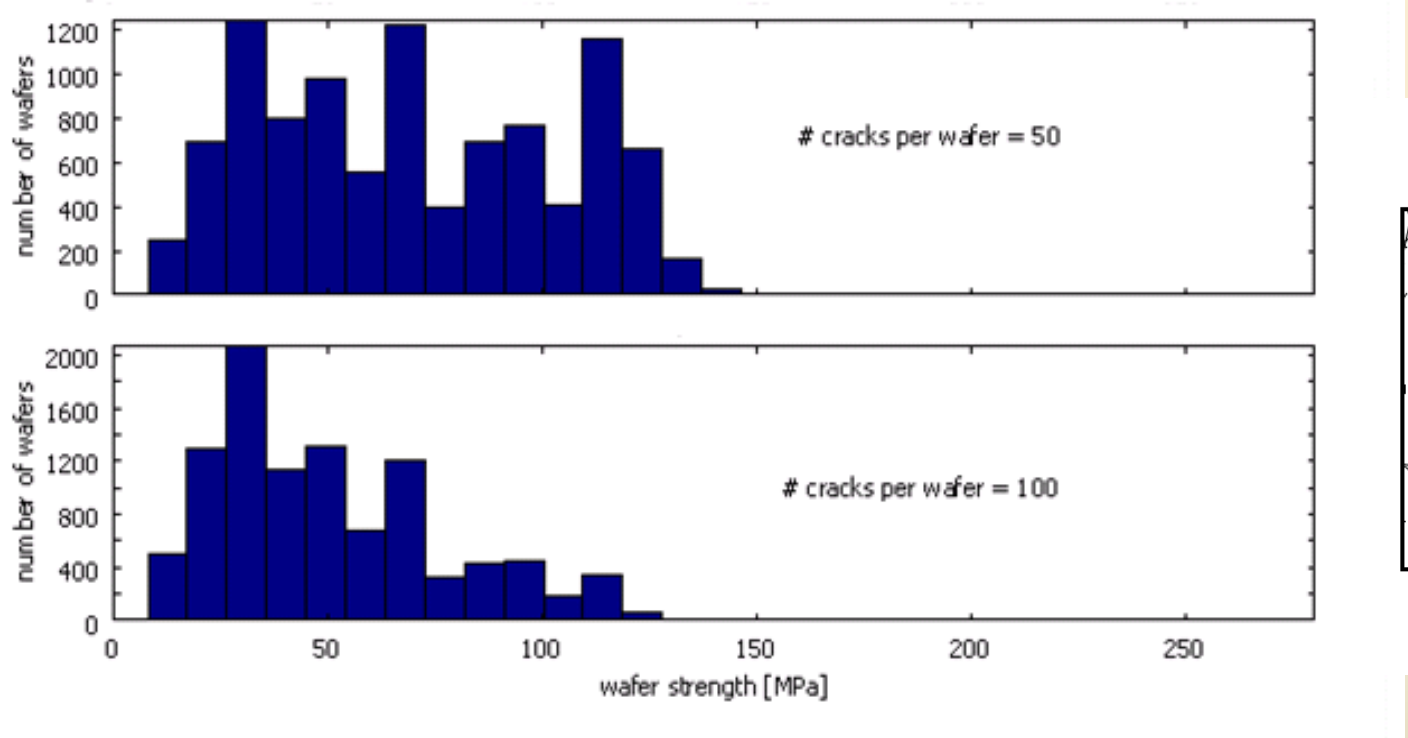
- Strength histograms take form of asymmetrical peaks of various width
- Minimum strength is fixed and equal to ~100 MPa
- Width of the peaks is inversely proportional to the number of cracks

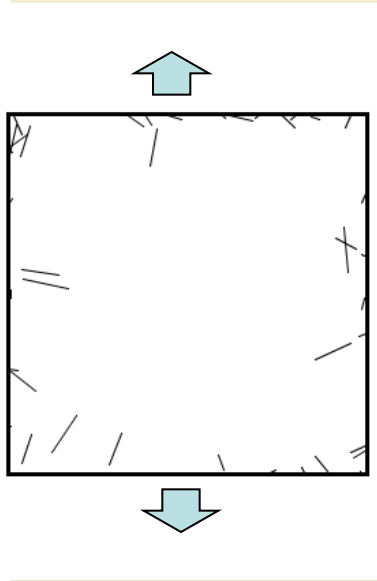
Multiple microcracks located at/close to wafer edge





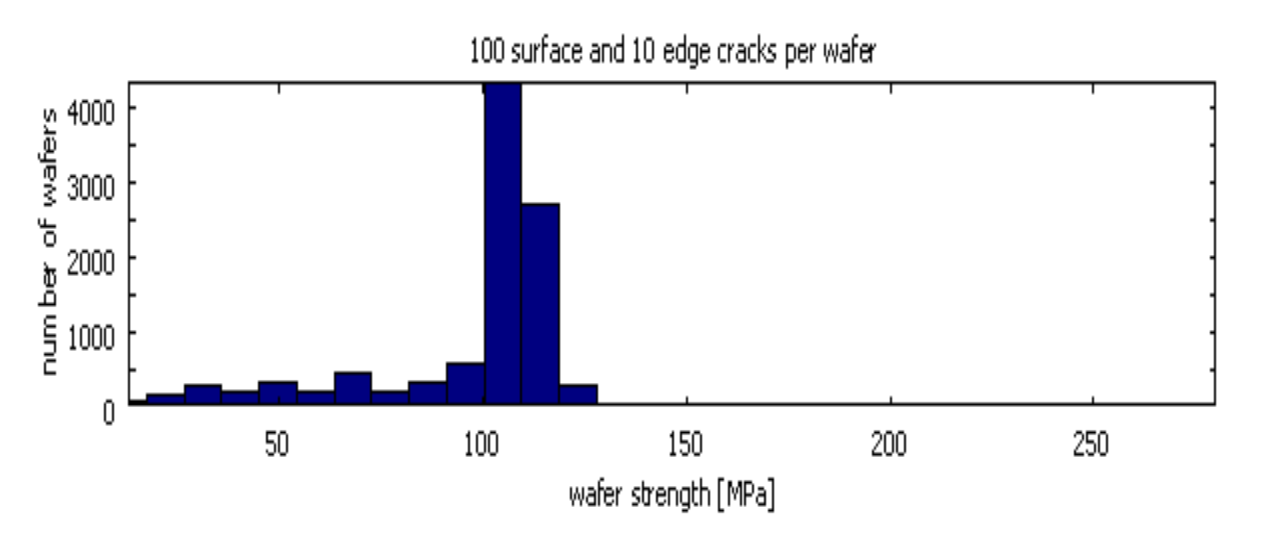
Multiple microcracks located at or close to wafer edges - continued

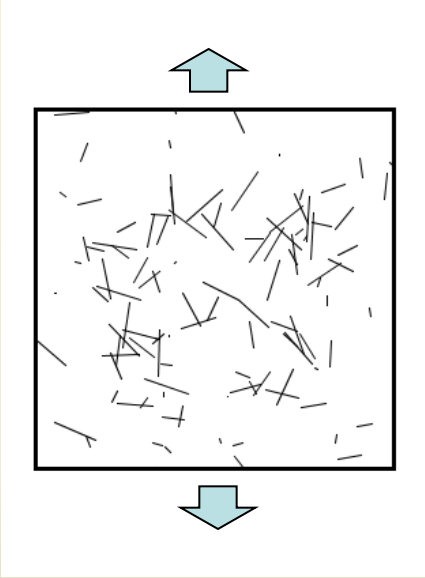




- Strengths of wafers with edge effect can reach very low values of ~ 20 MPa.
- Number of very weak cracks is relative low
- They start to dominate the fracture response of a wafer when their number is 50 or more

Strength of wafer with both types of microcracks





- Our model can predict strength histograms for wafers containing both types of defects (the weakest link principle).
- Example histogram: each wafer contains 100 microcracks located away from and 10 defects near the wafer edges.
- Wafer fracture is caused by both the edge and surface damage.

Wafer screening

Current approaches for studying cracks

IR Imaging: similar to an IR microscope (camera attachment) – transmission mode

It is difficult to image cracks because they can be very small and surfaces are rough

Thermal imaging

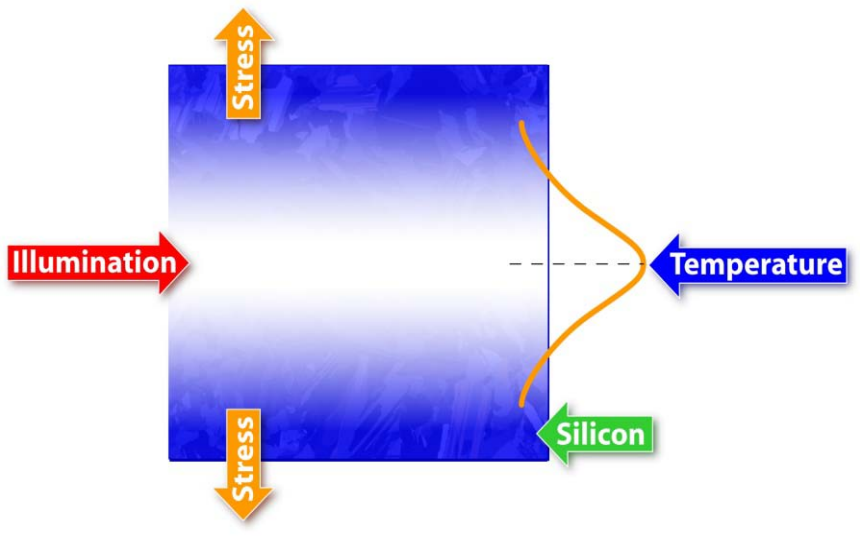
A crack produces discontinuity in the thermal impedance of the wafer. Hence, if a wafer is heated, there will be a temperature discontinuity at the crack site.

These approaches have not worked well and do not take into account processing/handling specific to the vendor

It seems reasonable to identify wafers that are likely to break during the solar cell processing and remove them.

A non-contact Wafer screening

Principle



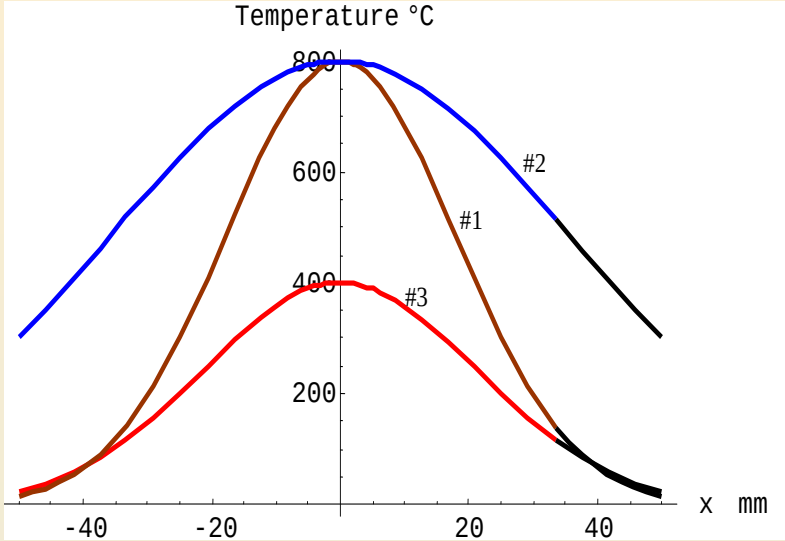


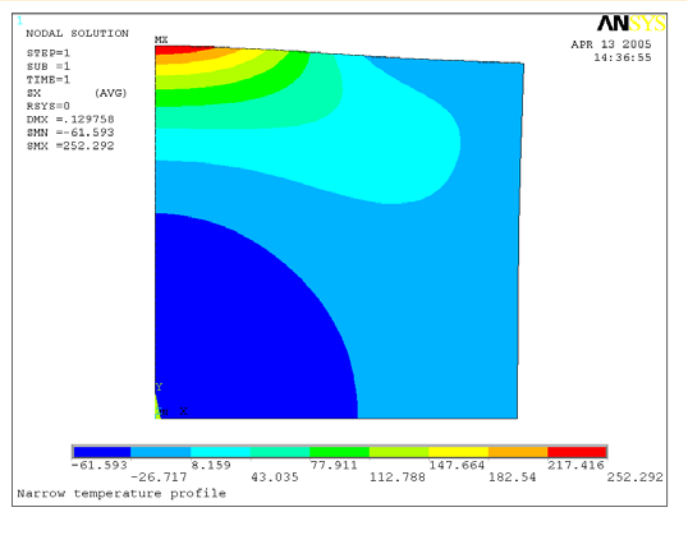
Illustration of a temperature gradient and stress produced by optical illumination of a Gaussian profile along x-direction

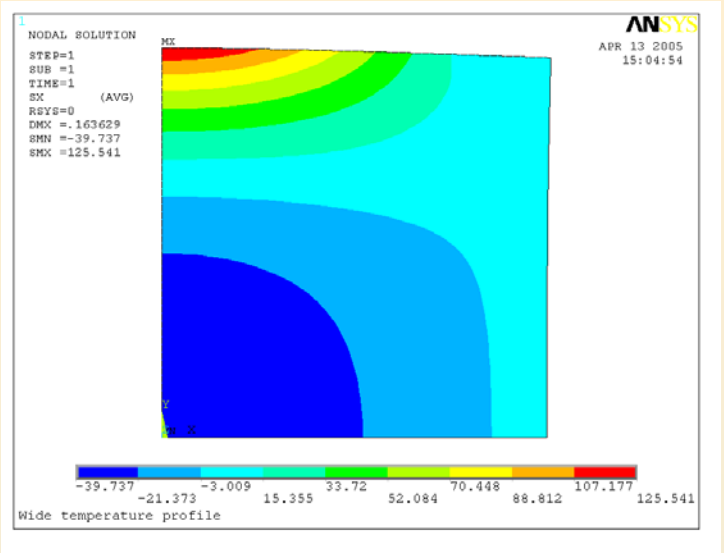
Gaussian temperature profiles

Profile #1 (narrow): T(0)=800°C, T(25)=300 ° C

Profile #2 (wide): T(0)=800, T(50)=30 ° C

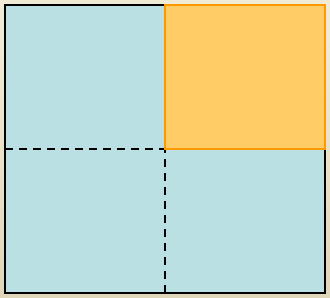
Profile #3: T(0)=400, T(25)=200 ° C

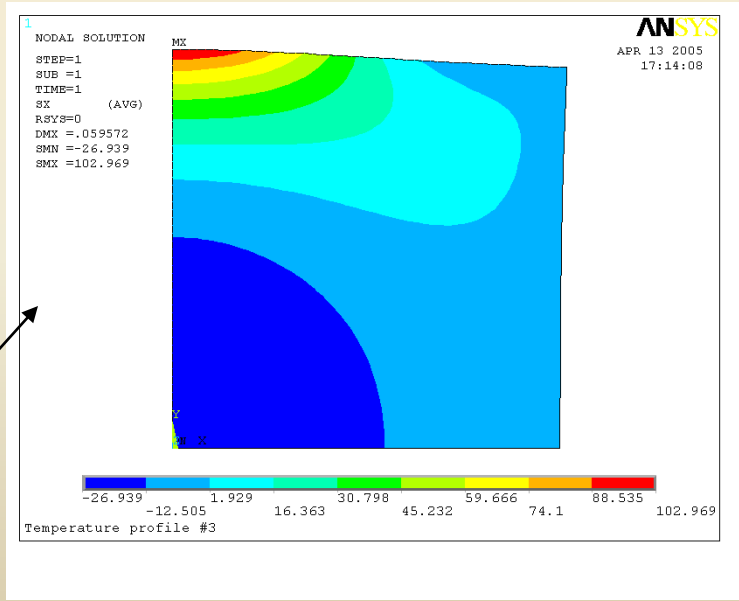




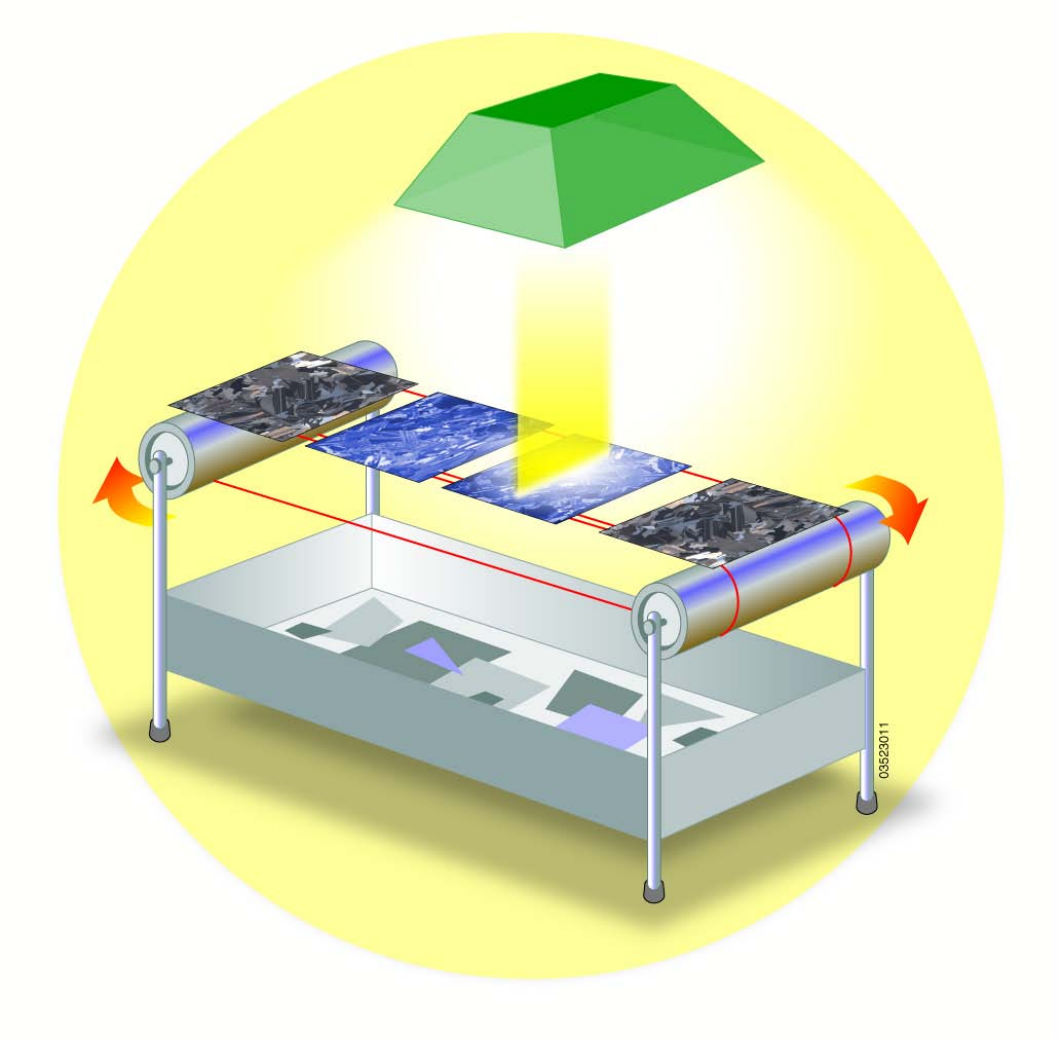
$T_{max} = 800\ °C$

A comparison of σ_x distribution for three temperature profiles





$T_{max} = 400\ °C$



A schematic of a simple setup for isolating wafers likely to break during solar cell processing

CONCLUSIONS

1. The dominant cause of wafer/cell breakage is the presence of μ-cracks

⇒ etching surface damage, edge grinding, gentle handling/processing can mitigate

⇒ *texturing exposes cleavage planes*

2. *Strength of the wafers/cells can be improved by suitable wafer preparation*

- *Gentler sawing, Edge grinding, chemical etching*

3. *Improved wafer handling and wafer transport*
4. *Improved temperature uniformity during processing*
5. *Cell designs that produce flat cells*
6. *Introduce some kind of wafer screening*