Solar Cell Grid Finger Failure due to Micro-cracking

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Abstract

The Semprius high concentration photovoltaic module (CPV) achieved the world record efficiency by utilizing a micro-transfer printing technique, small high efficiency cells, low loss optics and mature surface mount technology. The III-V triple junction cells are printed on an alumina interposer (Cell on interposer, COI) and a thin film metallization process is used to form the cathode and anode interconnection. Arrays of surface-mountable COI with thru-wafer vias are assembled onto printed-circuit boards using industry standard solder reflow. The combination of these technologies offers additional benefits of high reliability, low cost and scalability to high volume production for Semprius' modules.

Each COI undergoes stringent pass/fail criteria during the wafer probing test, including inspection of the cell electroluminescence (EL) image during forward bias. We have occasionally observed non-uniform EL images after several hundred temperature cycles (-40˚C to 85˚C) in an on-going internal reliability program. The dark-IV and light-IV performance of these defective cells was found to be nearly identical to "good" cells that are within specification.

The root cause of the non-uniform EL images was found to be related to micro-cracking of the metallization near the junction of interconnect metal and the cell grid finger, thereby resulting in an electrical open, along that grid finger.

We reduced the incidence of micro-cracking of metallization significantly by optimizing the plated metal thickness in the thin film metallization process. Modeling of the strain energy near the grid finger junction indicated that reducing the plated metal thickness would mitigate the incidence of micro-cracking.

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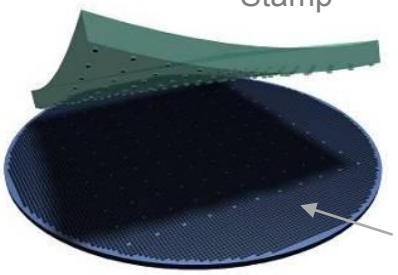
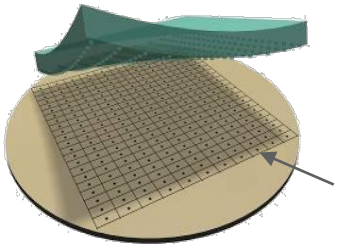
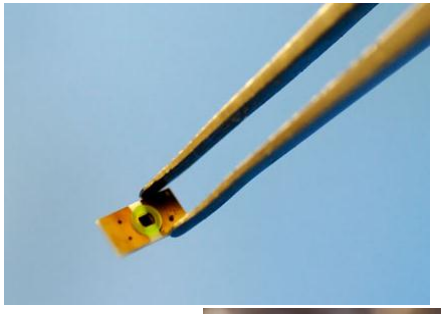
Key Semprius CPV technologies

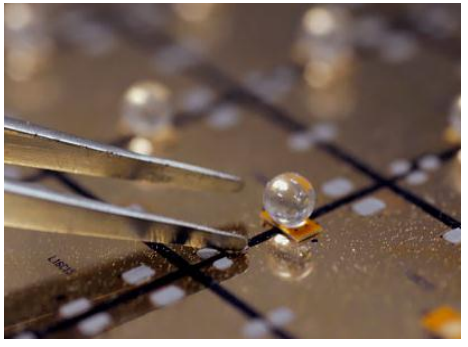
- Micro-transfer printing
  - Release and transfer large arrays of cells from EPI source wafer onto interposer substrate
  - Reduce wafer level processing and re-use source substrates
  - Is compatible with SMT technology
- Small and thin high efficiency cells on interposer
  - III-V triple junction cells printed on an alumina interposer (COI)
  - Forming the cathode and anode interconnect by a thin film metallization process
  - No need for active thermal management
- Low loss optics
  - Plano-convex primary and glass lens secondary
- Mature surface mount technology
  - Assembling arrays of surface-mountable COI with thru-wafer vias onto backplane using industry standard solder reflow
  - High reliability, low cost and scalability to high volume production





COI-High efficiency small receiver (>40%)





COI mounted on backplane using standard surface mount technology

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Selection of COI for backplane assembly

- Each COI undergoes stringent pass/fail criteria, ensuring reliable operation of the module with a large number of cells.
- The COI substrate level testing before dicing includes:
  - Dark IV (DIV)
  - Light IV (LIV)
    - Determine I_{sc} (short circuit current), V_{oc} (open circuit voltage) and other parameters using a spot focused Xenon light source
  - Cell temperature rises
    - Derived from the band gap shift of the InGaP sub-cell at a fixed power load
  - Quality of EL image

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On-going reliability testing

- COI bonded on the test boards (using with the same material and re-flow process as the backplane used for the module) for on-going reliability testing:
  - Temperature cycle (TC from -40˚C to 85˚C)
  - Damp heat (DH) exposure (85˚C/85%RH)
  - High temperature and current aging

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Onset of dark grid fingers after temperature cycles

- Observed dark grid fingers in some EL images after several hundred temperature cycles
- Cells with or without dark grid finger, showed no significant difference in DIV/LIV characteristics
- Dark grid fingers or other EL defects were identified by a comparison of EL images with a reference cell EL image

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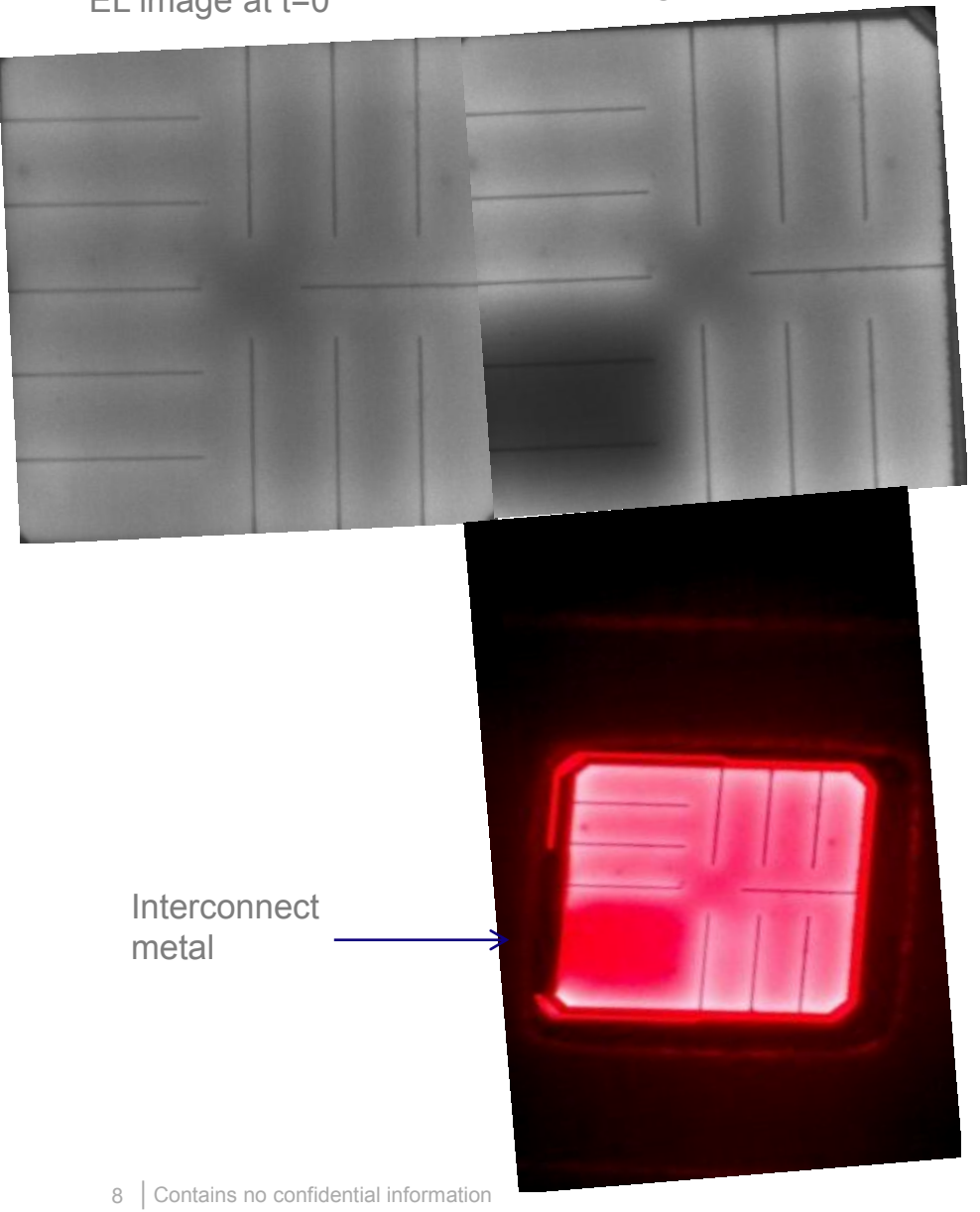
EL images at t=0 and after 427 TC for a cell (L2C2) with dark grid fingers

L2C2

EL image at t=0

EL image after 427 TC



- Two dark grid fingers were observed after 427 TC.
- The entire cell EL image indicates the dark region started from the interconnect metal edge.

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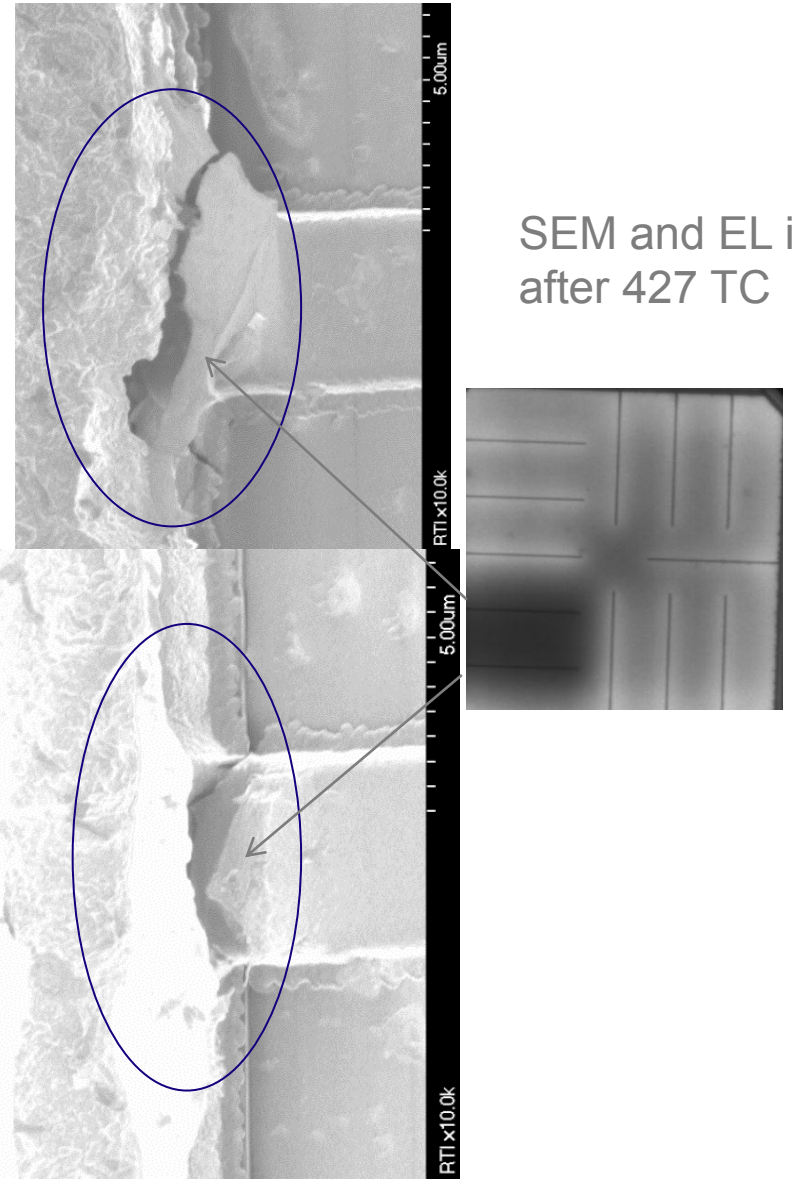
SEM images near the junctions of interconnect and grid finger (L2C2)



SEM and EL images after 427 TC

- Two micro-cracking occurred near the junctions of interconnect and two dark grid fingers
- This cell with thick plated interconnect metal

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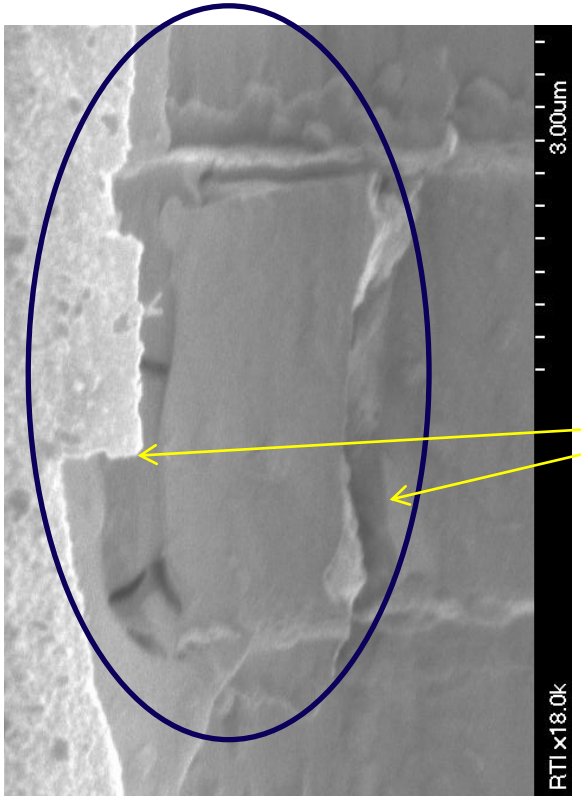
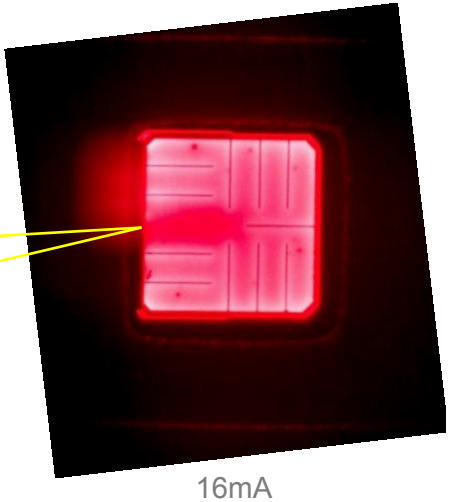
The 2nd example showing a dark finger after 427 TC



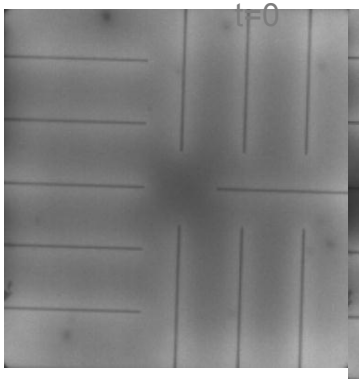
L2C3



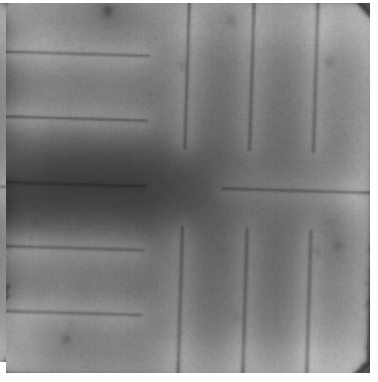
16mA

- A micro-cracking occurred near the junction of interconnect and the dark grid finger.
- This cell with thick plated interconnect metal.

EL image at t=0



EL image at t=427



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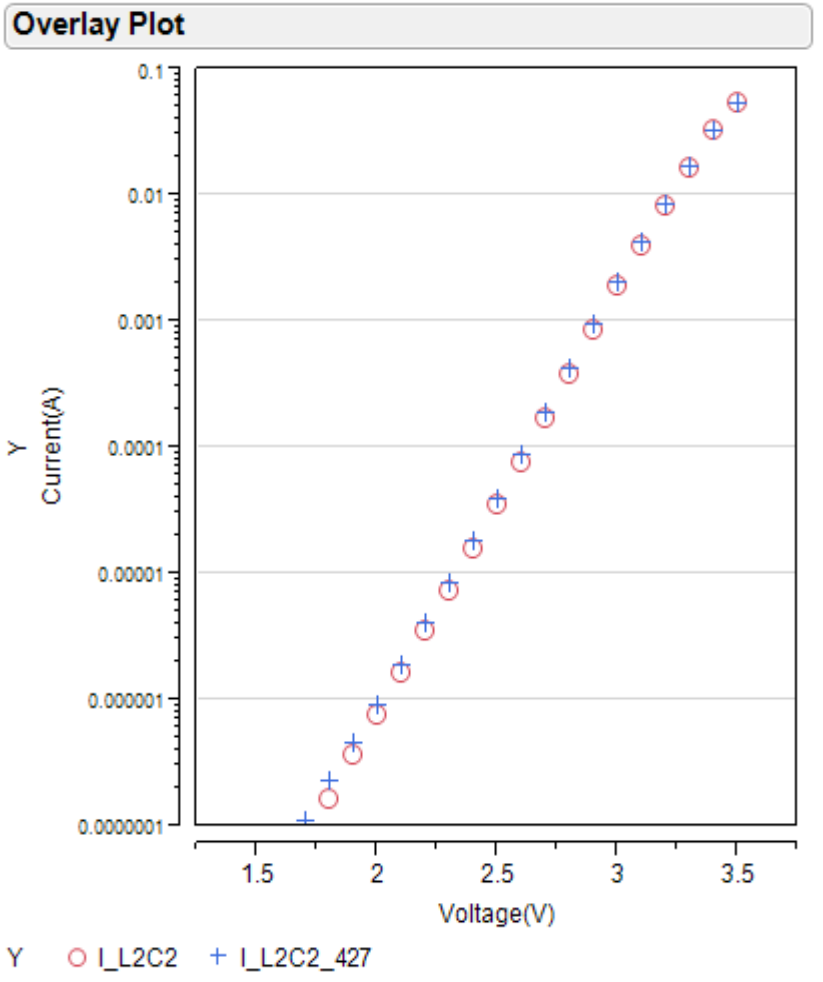
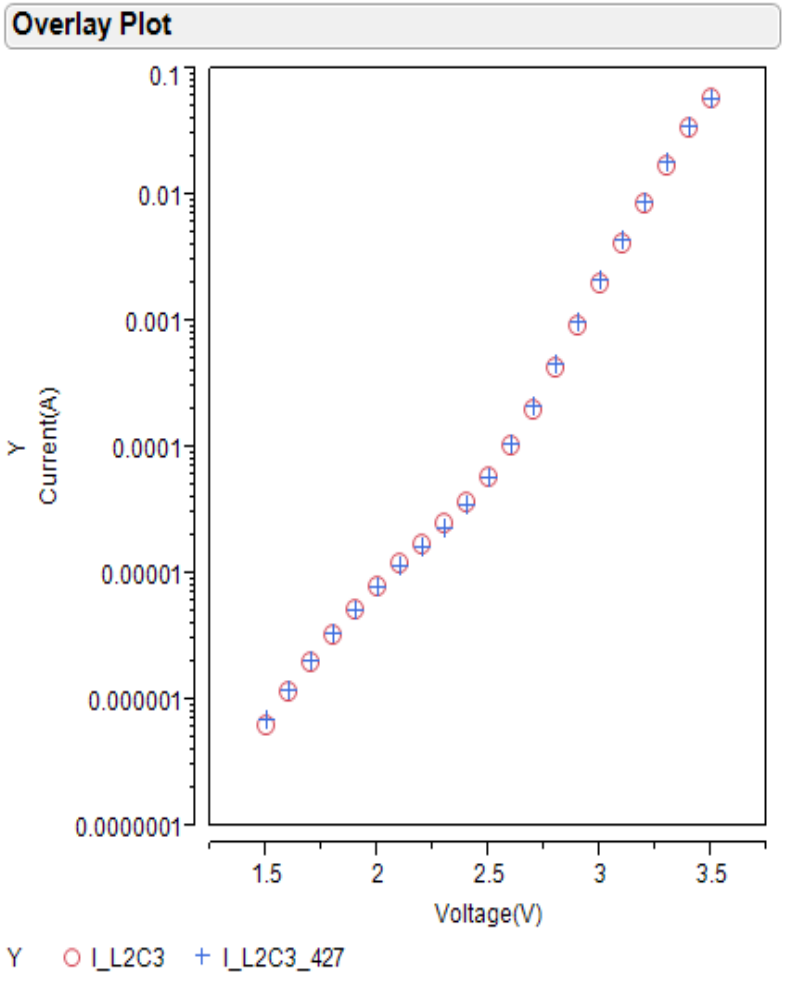
Comparison in DIV characteristics before and after 427 TC for cells with micro-cracking

- Nearly identical DIV characteristics (Current measured at t=0 and after 427 TC were plotted as a function of voltage), as shown below, for these cells (L2C2 and L2C3) with micro-cracking

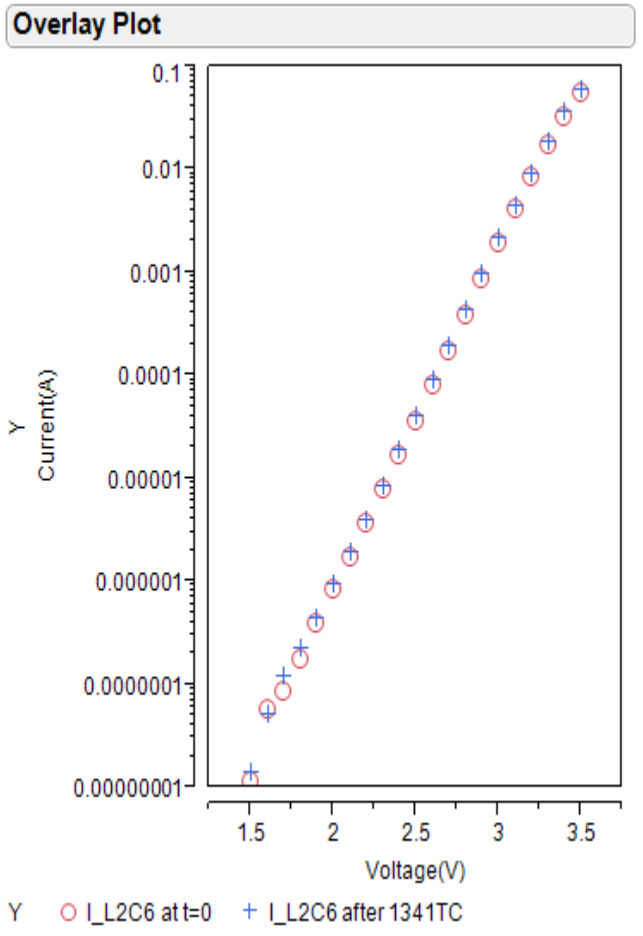




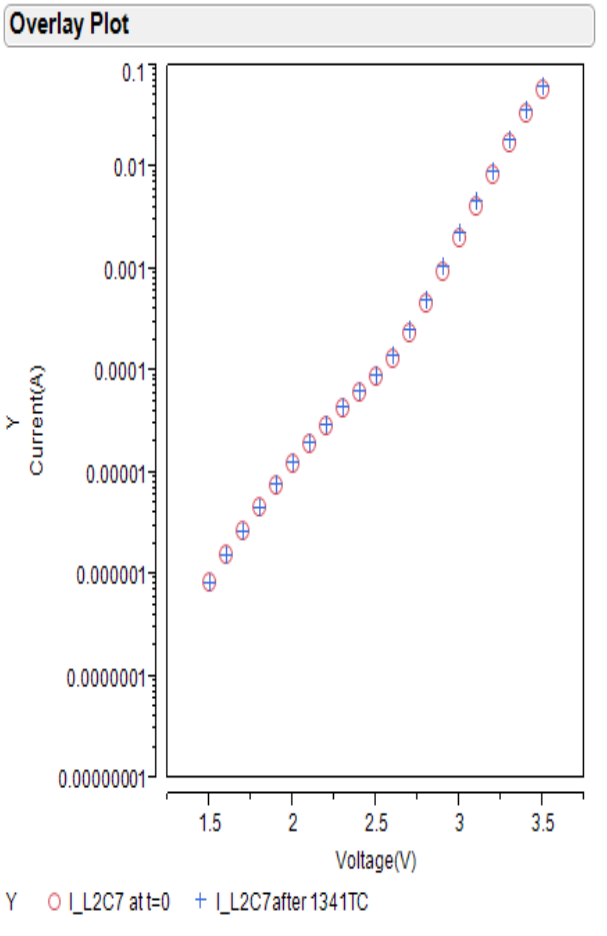
Comparison in DIV characteristics before and after 1341 TC

- No significant change in DIV characteristics (Current measured at t=0 and after 1341 TC were plotted as a function of voltage) for cells with or without dark grid finger
- These cells with thick plated metal

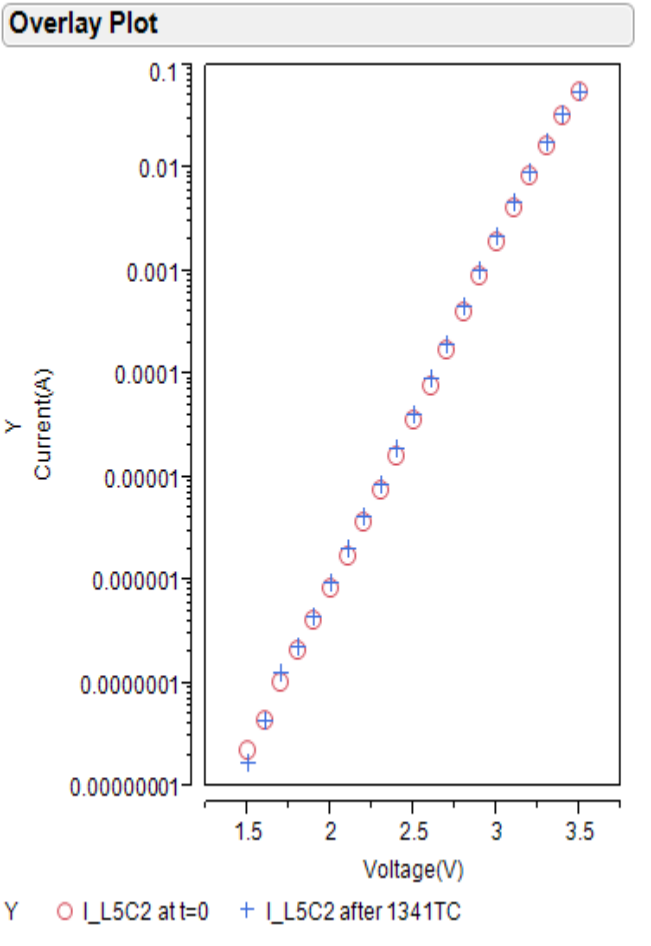
Cell without dark finger



Cell without dark finger



Cell with one bad grid finger



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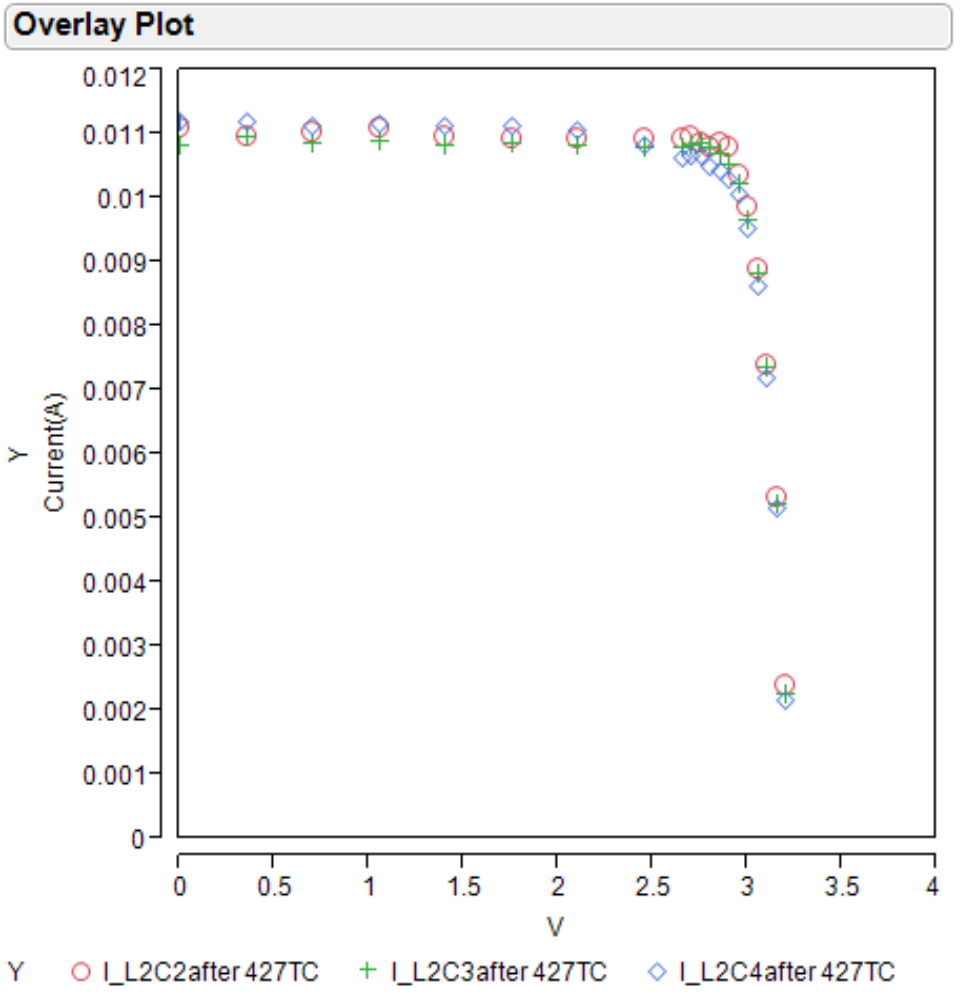
Comparisons in Light IV (LIV) characteristics for cells with or without dark grid finger after 427 TC



- L2C4-no dark grid finger
- L2C3 with one (1) and L2C2 with two(2) dark grid fingers, respectively.
- Nearly identical LIV traces for cells with/without dark grid finger
- These cells with thick plated metal

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Comparison in LIV characteristics for cells with different numbers of dark grid fingers from the same COI substrate after 1341 TC

- Below showed the mean and standard deviation of I_{sc} ,V_{oc} and field factor(FF) with different numbers of dark grid fingers.
- Due to a rather large standard deviation, the differences listed below are not statistically different.
- Due to small changes in LIV characteristics and instability of the Xenon light source, it is not feasible for monitoring LIV changes as a function of TC.

	I_{sc}			V_{OC}			FF		
Number of dark grid fingers after 1341 TC	Mean (mA)	Mean (ratio)	Std. Dev. (mA)	Mean (V)	Mean (ratio)	Std. Dev. (V)	Mean (%)	Mean (ratio)	Std. Dev. (%)
0	11.54	1.000	0.459	3.246	1.000	0.0076	88.95 (Note1)	1.000	0.69
1	11.39	0.987	0.486	3.240	0.998	0.0059	88.44	0.994	0.78
2	11.27	0.977	0.259	3.237	0.997	0.0049	88.04	0.990	0.87

Note1: Due to cell current matching, higher operating temperature and current in the module, the module level has a lower FF, compared to the individual COI.

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Strain energy simulation

- Dark grid fingers were observed mainly on the left side of cell (cathode side)
- We suspected that the high strain, resulting from the high step coverage and large mismatch in CTE of various layers, was the root cause of the micro-cracking after temperature cycles.
- Strain simulation by the finite element analysis with:
  - A fixed dielectrics thickness
  - Different plated metal thickness

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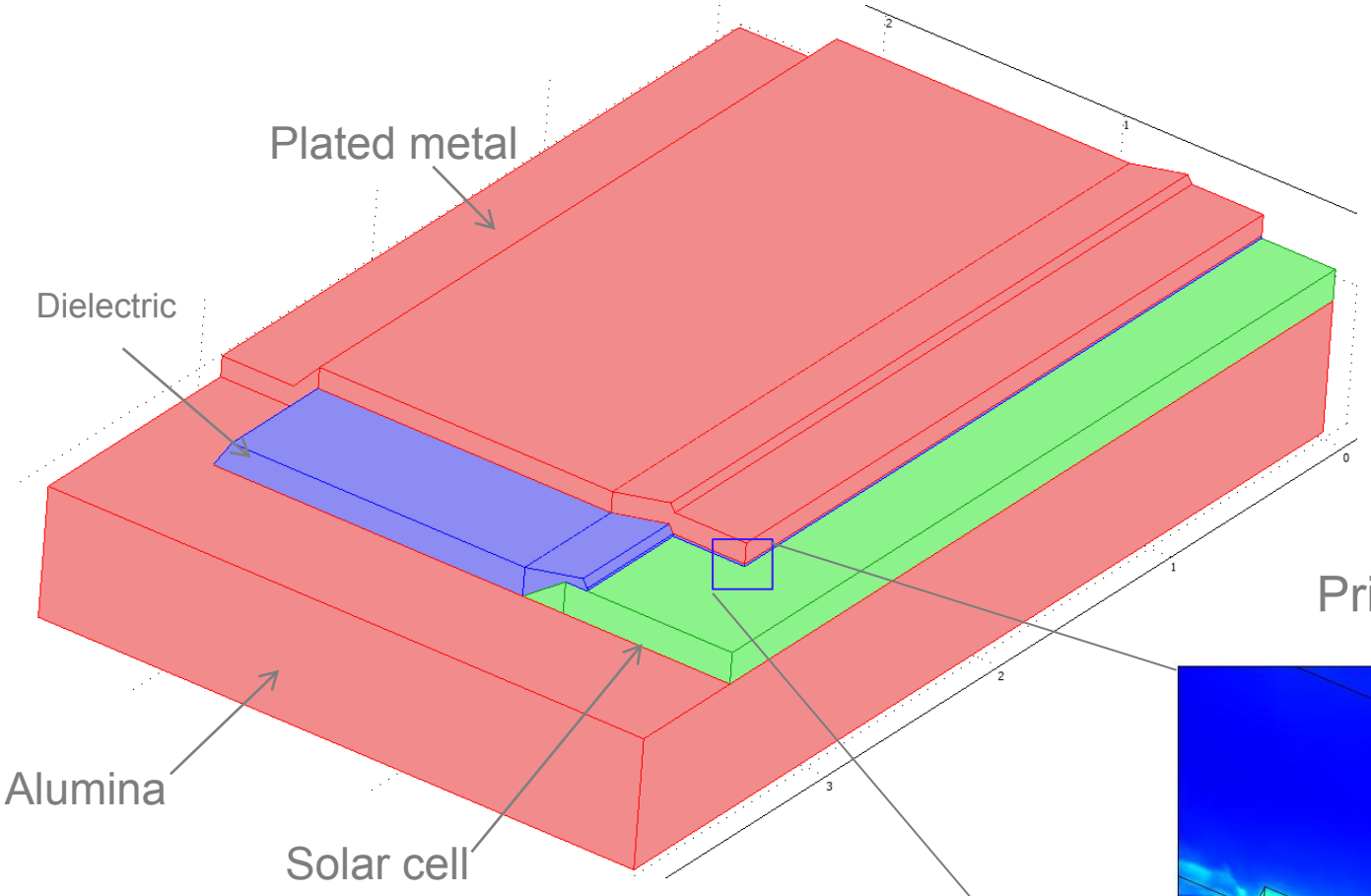
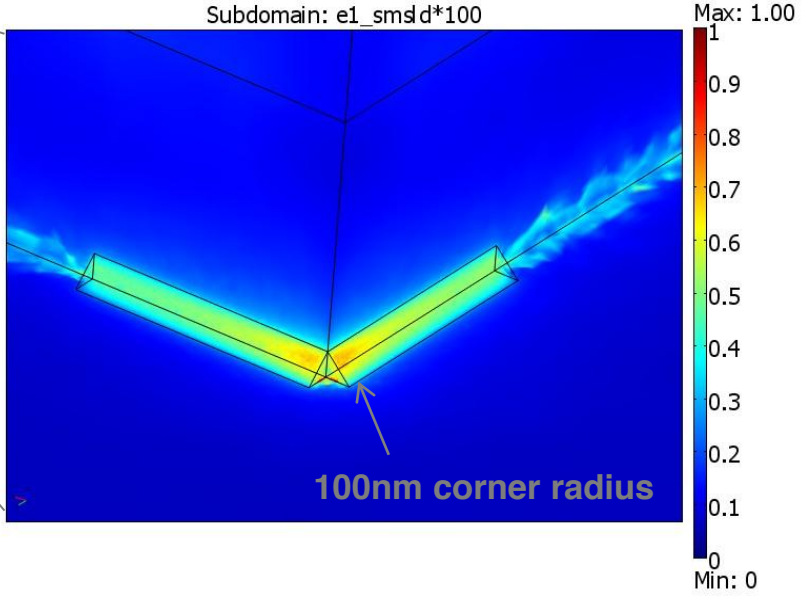
Finite Element Analysis for strain energy



Principal strain (%)



Structure is fully relaxed at 20C
Temperature raised to 85C (65C delta)

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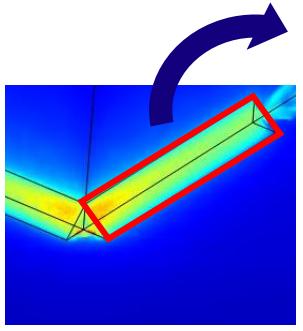
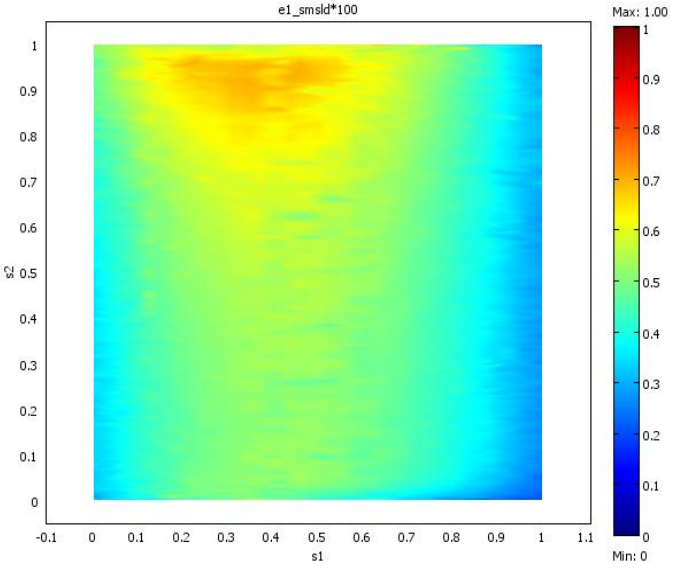
Strain with different plated metal thickness

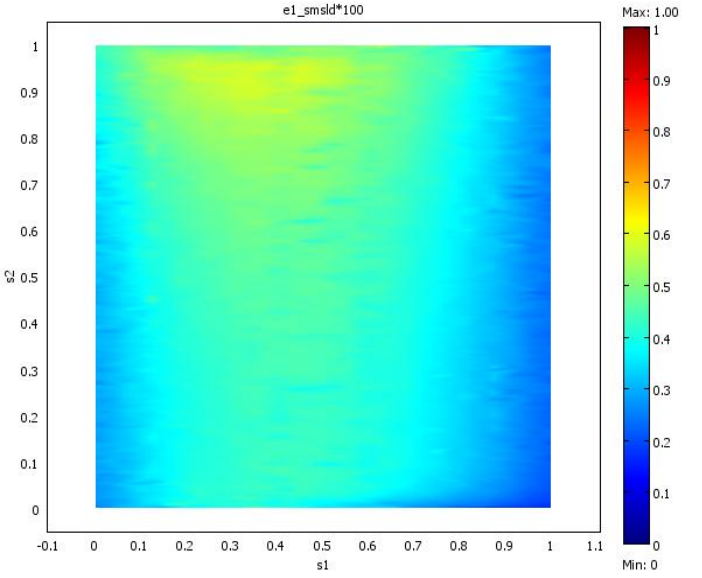
Plated metal thickness : 4 AU (arbitrary unit)



Principal strain (%)

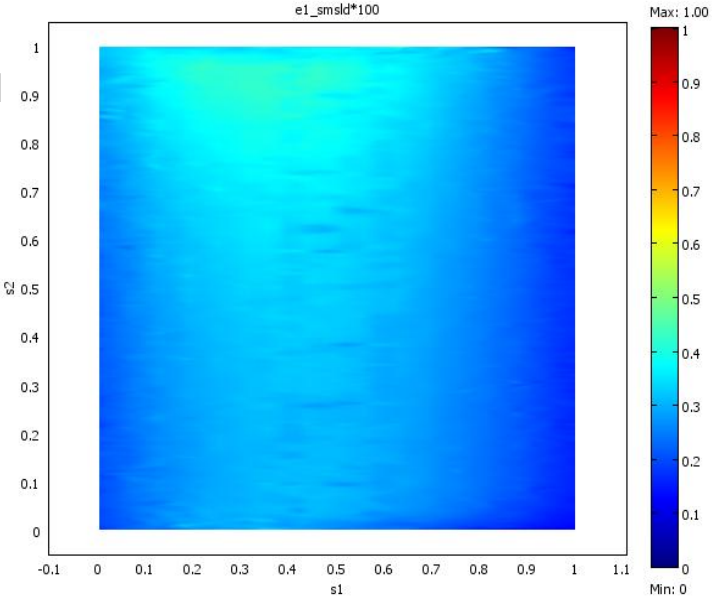


Plated metal thickness : 3 AU

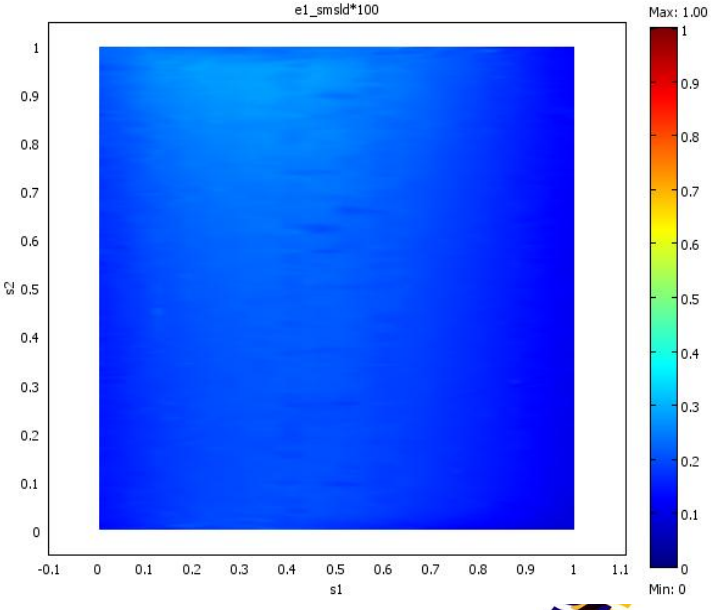


~2x reduction in strain by using thin plated metal

Plated metal thickness : 2 AU



Plated metal thickness : 1AU



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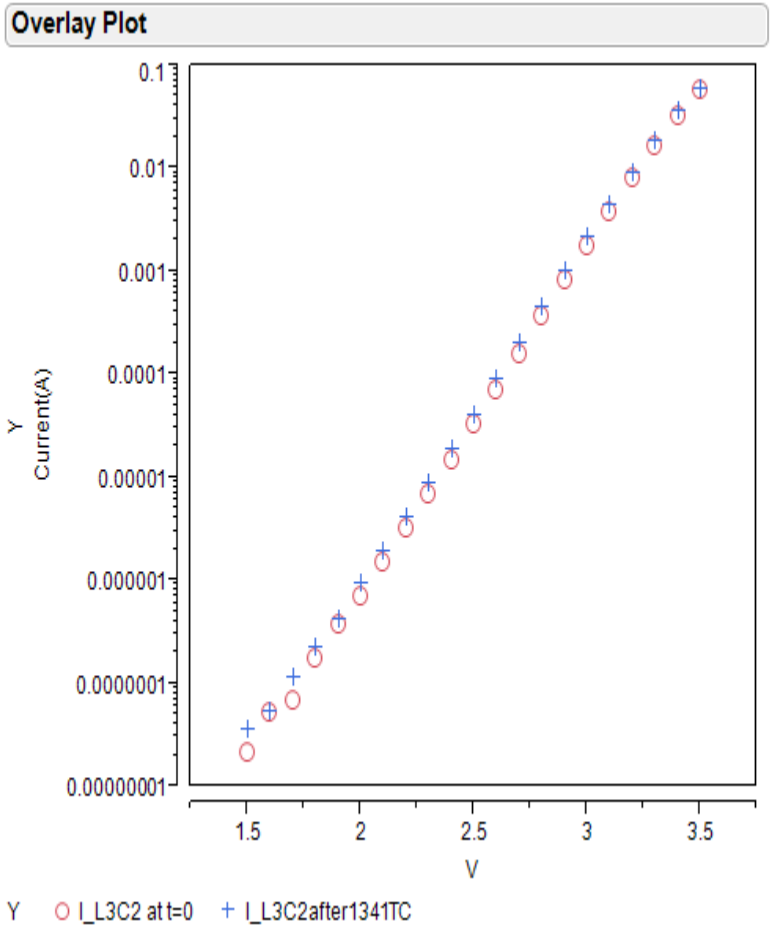
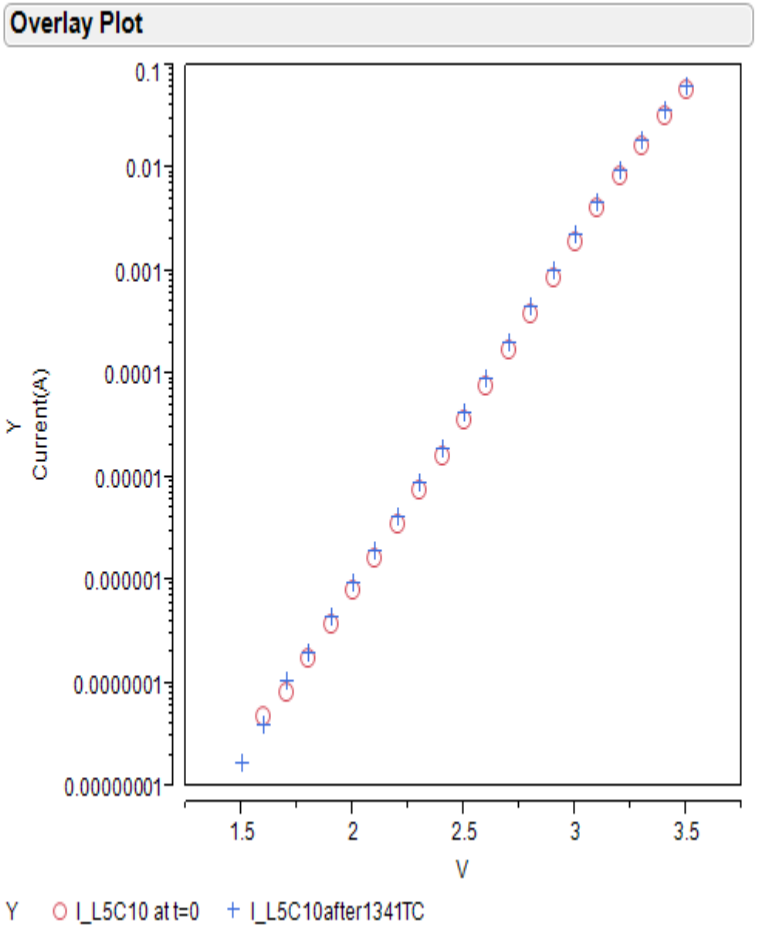
Examples of DIV characteristics before and after 1341 TC for cells with thin plated metal





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Comparison in LIV characteristics for COI with two different plated metal thickness

- Comparison in LIV characteristics after 1341 TC, between two COI substrates with different plated metal thickness (cells printed from the same source wafer)
- Two COI substrate tested at about the same time frame
- Observed a significant number of cells with dark grid fingers from the COI substrate with thick plated metal after TC
- No dark grid finger from the COI substrate with thin plated metal
- Slightly higher mean and lower standard deviation for COI with thin plated metal

	I_{sc}		V_{OC}		FF	
After 1341TC	Mean (mA)	Std. Dev. (mA)	Mean (V)	Std. Dev. (V)	Mean (%)	Std. Dev. (%)
COI without dark grid finger (with thick plated metal)	11.54	0.459	3.246	0.0076	88.95	0.69
COI without dark finger (with thin plated metal)	12.00	0.224	3.247	0.0043	89.02	0.38

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Summary

- SEM images indicated that the dark grid fingers were related to micro-cracking of the metallization
- No significant degradation in DIV and LIV with the onset of the dark grid finger, resulting from the temperature cycling
- COI with thin plated interconnect metal showed a significant reduction in micro-cracking, which is consistent with the strain simulation results
- The elimination of dark grid fingers could be responsible for the slight improvements in LIV characteristics

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