SOLON Corporation

Potential Induced Degradation

William Richardson

NREL PVRW, February 1^{th}, 2011

Don't leave the planet to the stupid

SOLON

SOLON at a Glance

- One of the largest manufacturers of solar modules in Europe
- Large scale rooftop and greenfield installations
- Founded in 1997
- Production sites in Germany, Italy and the U.S.
- Employees: approx. 900

SOLON Corporation at a Glance

- 80 MW of annual manufacturing capacity in Tucson, AZ
- Large scale rooftop and Utility-scale installations
- Founded in 2007
- Wholly-owned subsidiary of SOLON SE
.
- Employees: approx. 150

Solar modules

Power plants

Industrial rooftops

Content

- Introduction & Motivation
- Background & Approach
- Results
  - Cell level
  - Panel level
  - System level
- What's Next?
- Summary & Conclusion

Motivation

Objective: To make Solar Energy even more competitive

→ Reduction of $/kWh

→ Two approaches:

1. Reduction of $/kWp

   → Become as cheap as possible!

2. **Increase lifetime/ Decrease degradation**

   → Become as stable/long-lasting as possible!

→ Both tracks have to be pursued in parallel …

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Potential Induced Degradation

- Power degradation due the exposure to an external potential

- External potential = Potential relative to ground

→ High Voltage Stress

= Power Degradation caused by the exposure to a potential relative to ground, and dependent on its magnitude and sign

→ Two cases: Reversible (Polarization)

Irreversible (Electro corrosion)

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Background

- First addressed by Hoffman and Ross (JPL) 1978: Impact of voltage-biased humidity exposure of solar panels on long term stability – “Bias Humidity test… as a candidate for module qualification”
- Prominent cases such as Sunpower’s Polarization effect
- More recently NREL: Degradation caused by HVS not covered by IEC or UL standards right now
- Increasing importance because:
  - → Increasing need to push down overall degradation
  - → Increasing system voltages
  - → Increasing variety of solar cell technologies

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Approach

Objective: Minimizing / Avoiding PID

→ On cell level

→ On panel level

→ On system level

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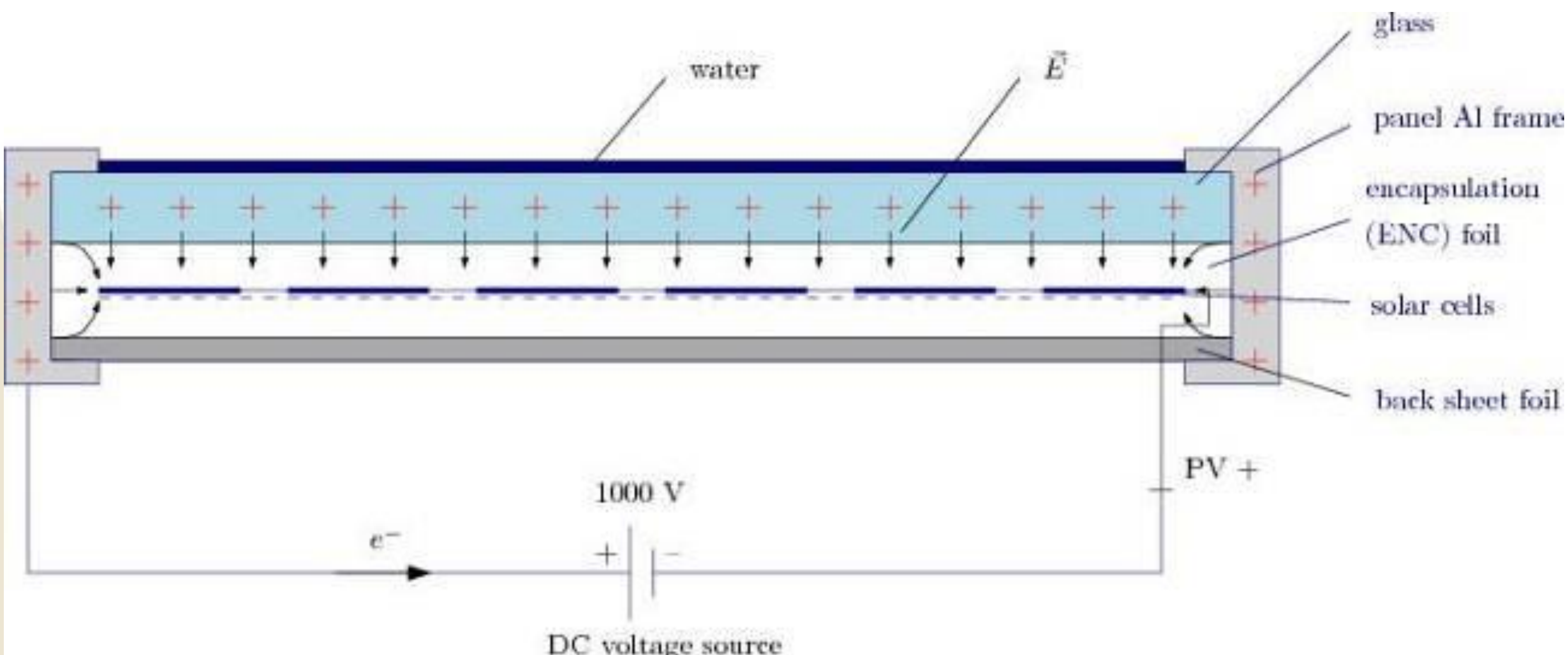
Test Set up

- Worst case scenario
- Simulation of potential relative to ground



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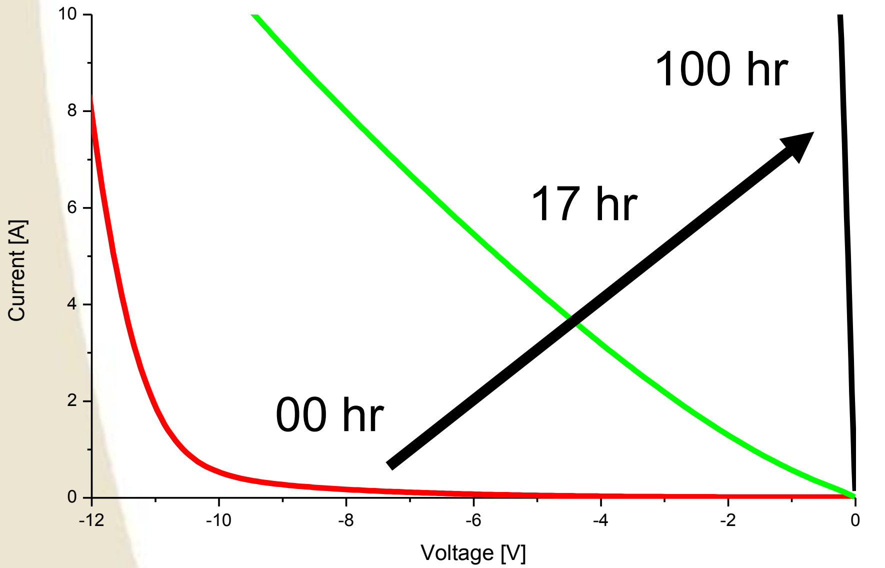
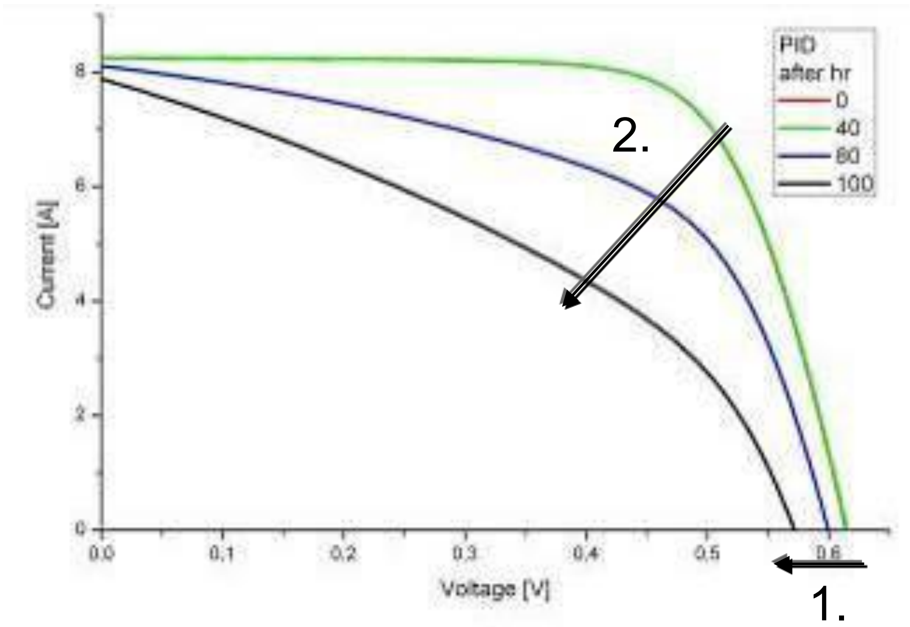
Cell Level

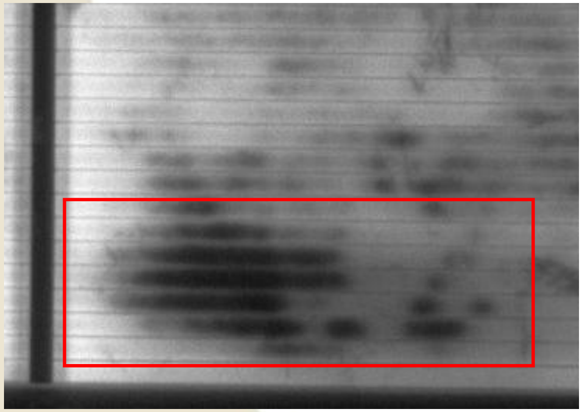




- Decrease of overall shunt resistance

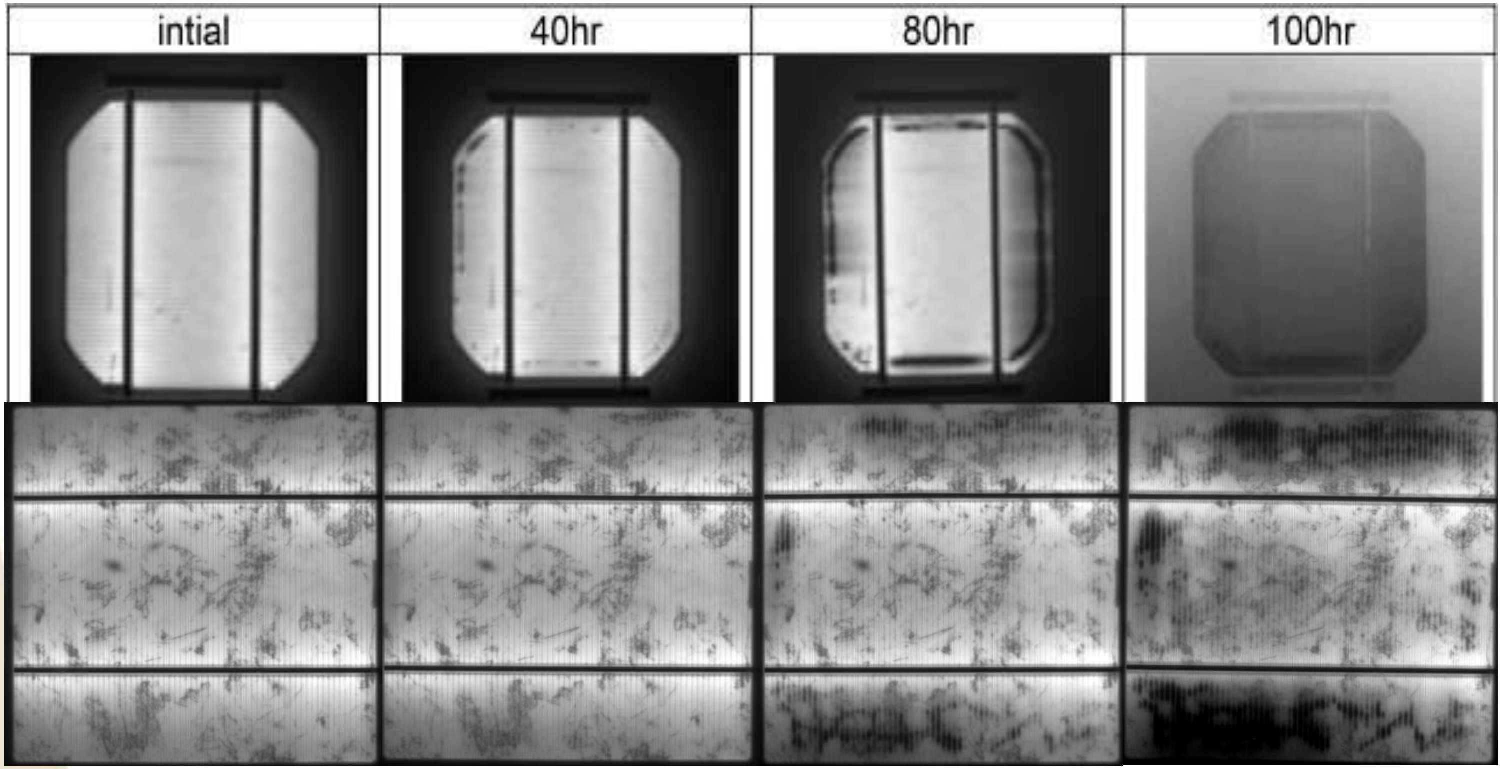
→1. Loss FF

→2. Loss in open circuit voltage



→Local short circuit of the pn-junction

Cell Level



EL images of a cell during PID test (1000V, 100h)

Tendency for PID very different for different cell manufacturers

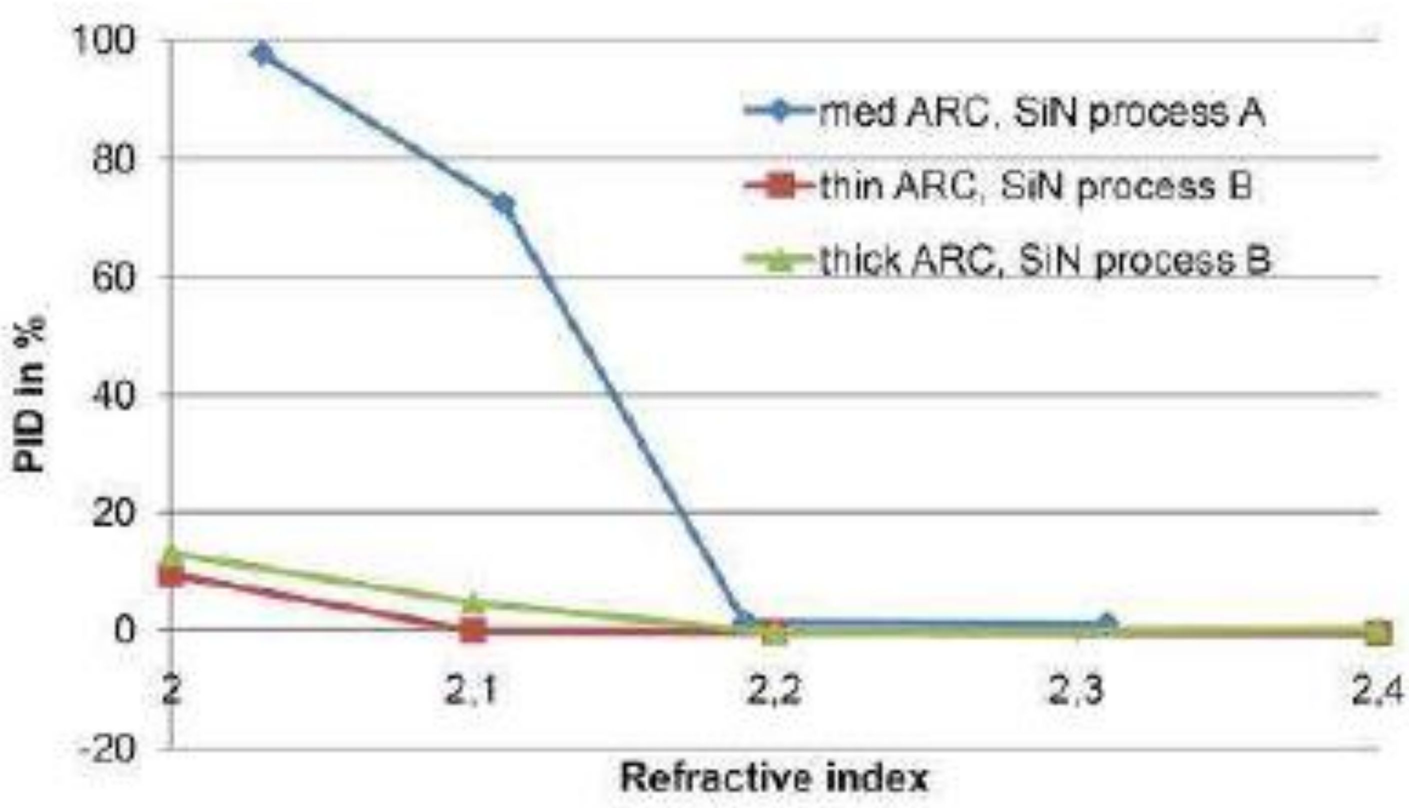
→ Impact factors on cell level?

Cell Level

Impact factors:

- Base resistivity of wafer material → significant influence
- Emitter sheet resistivity → significant influence
- **ARC deposition → key feature**
  - Ratio of Si to N
  - Thickness
  - Homogeneity

Cell Level



By choosing suitable parameters for ARC deposition PID can be minimized/ stopped on cell level

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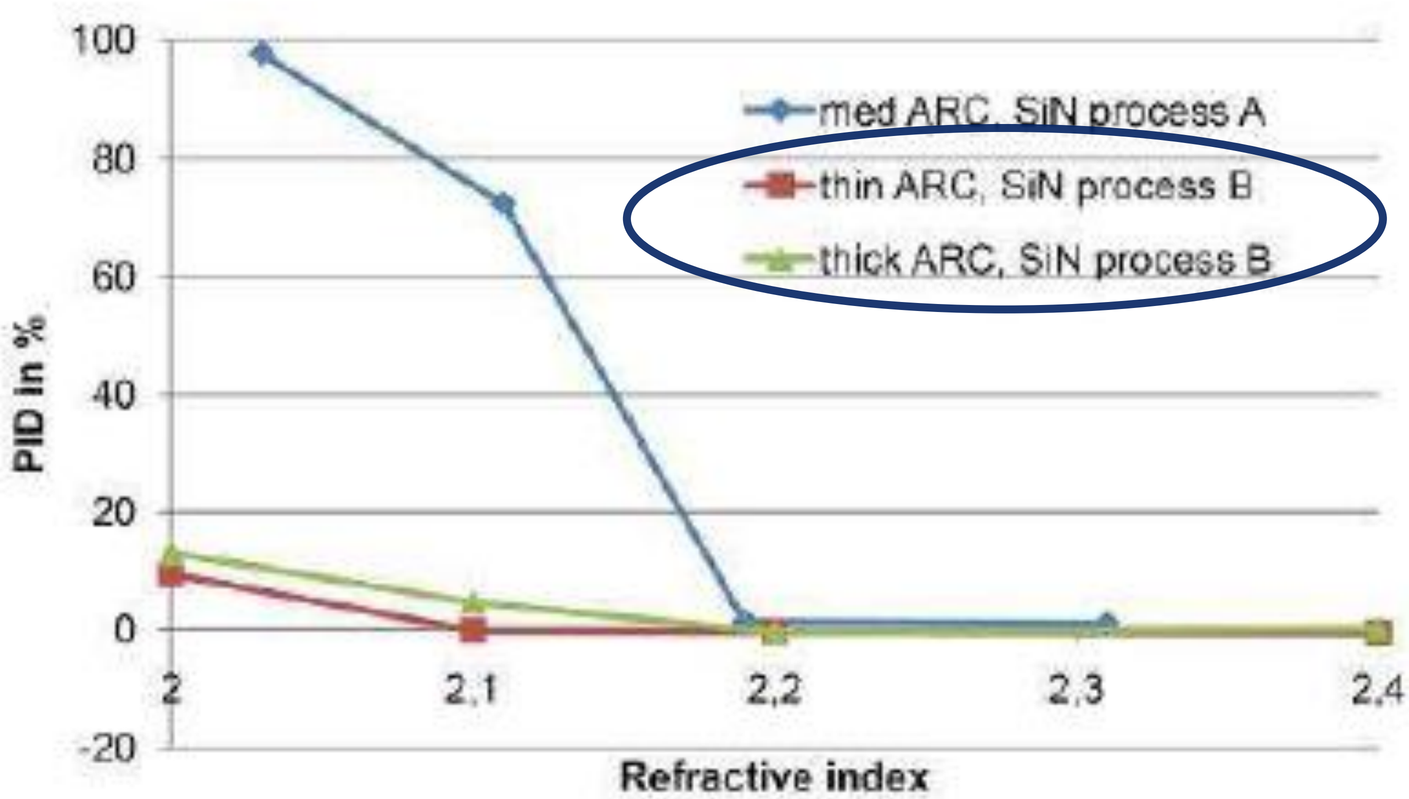
Cell Level



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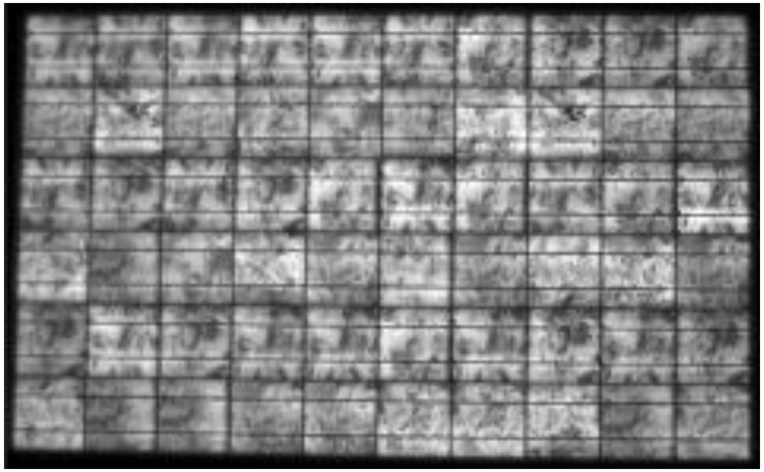
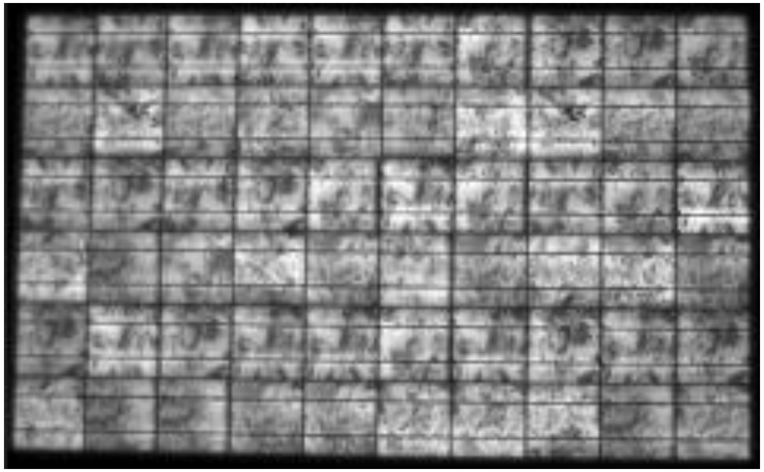
Panel level



EL image of a panel before
100hr 1000V PID...

Panel level



EL image of a panel before
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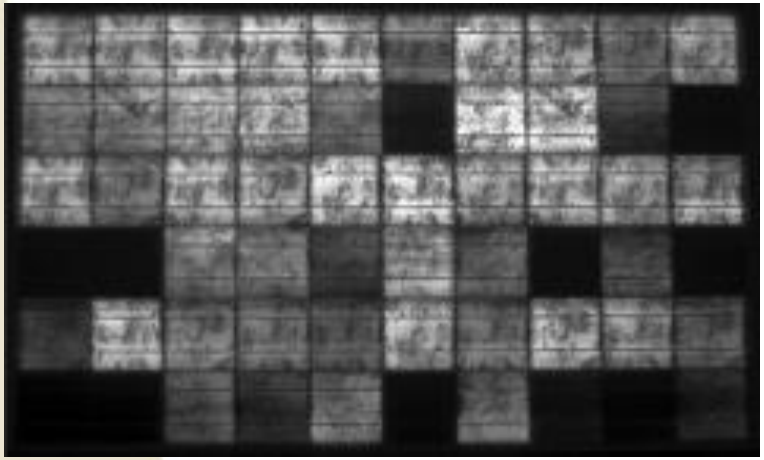
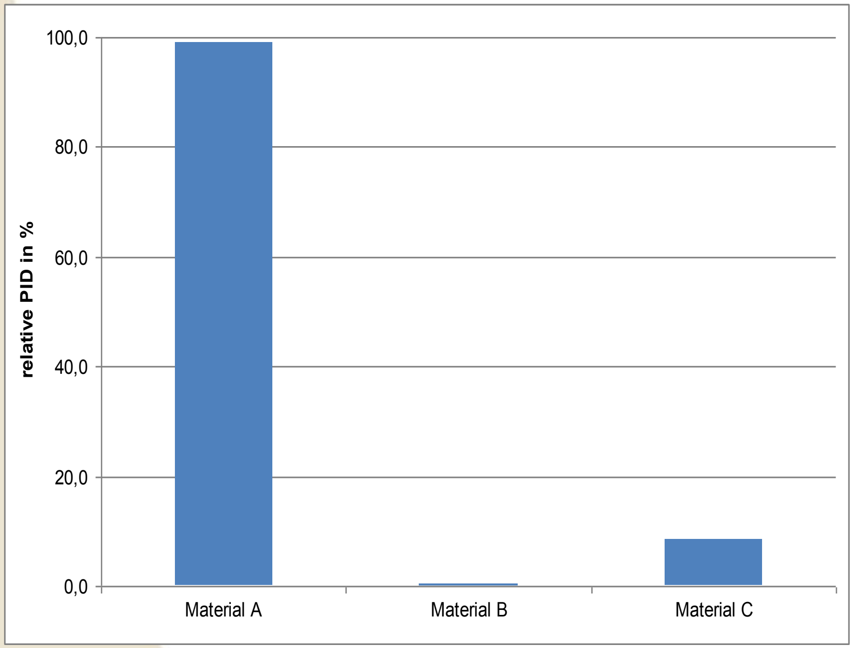
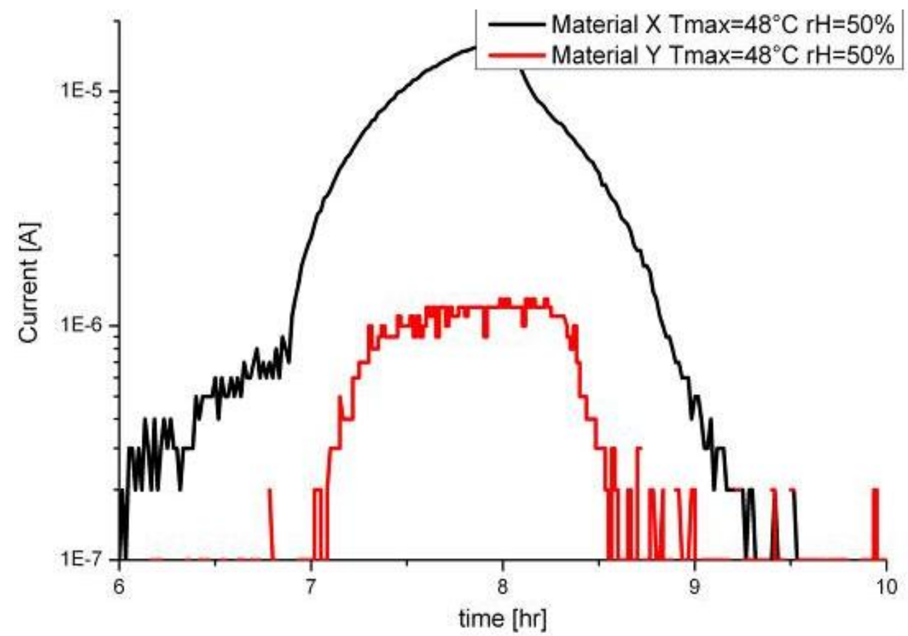


...and after.

Key feature: Leakage current

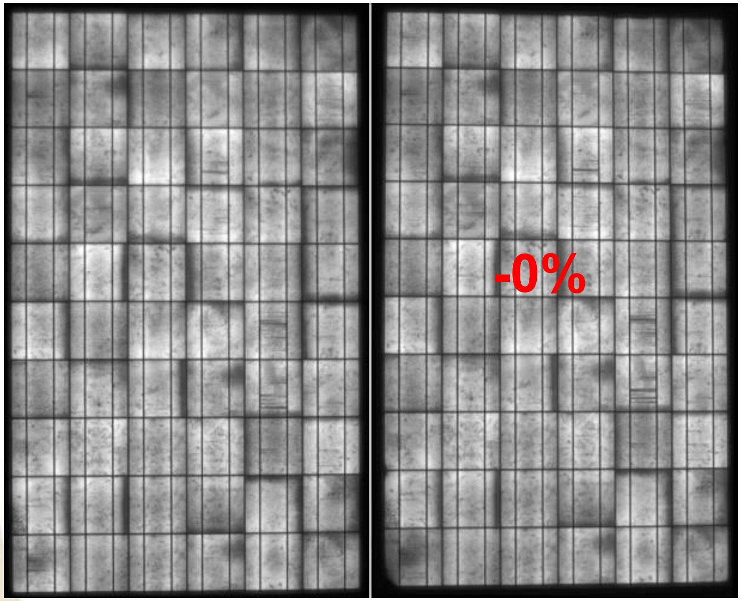
Panel level I

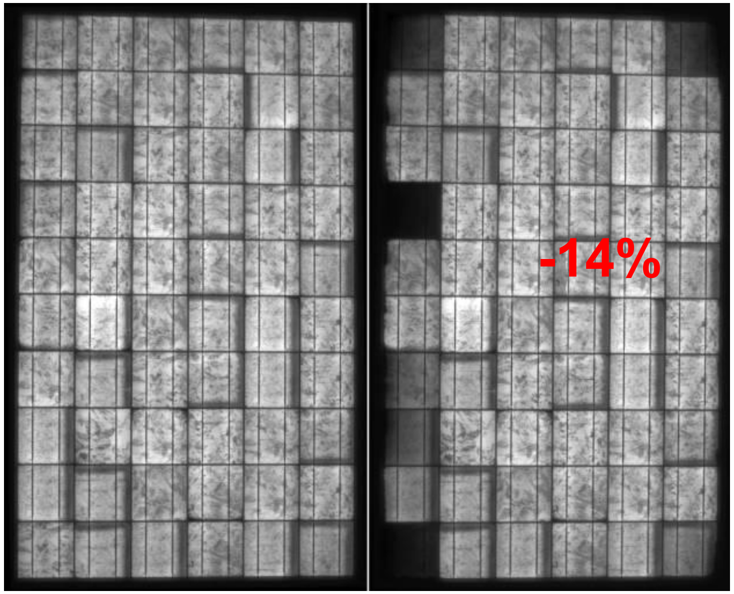




PID can be stopped/ minimized on panel level
by minimizing leakage current → Choice of suitable encapsulation

Panel level II





Time: 100h

Voltage: 1000V

Temperature: 48°C

Humidity: 50%

Material: X

Time: 100h

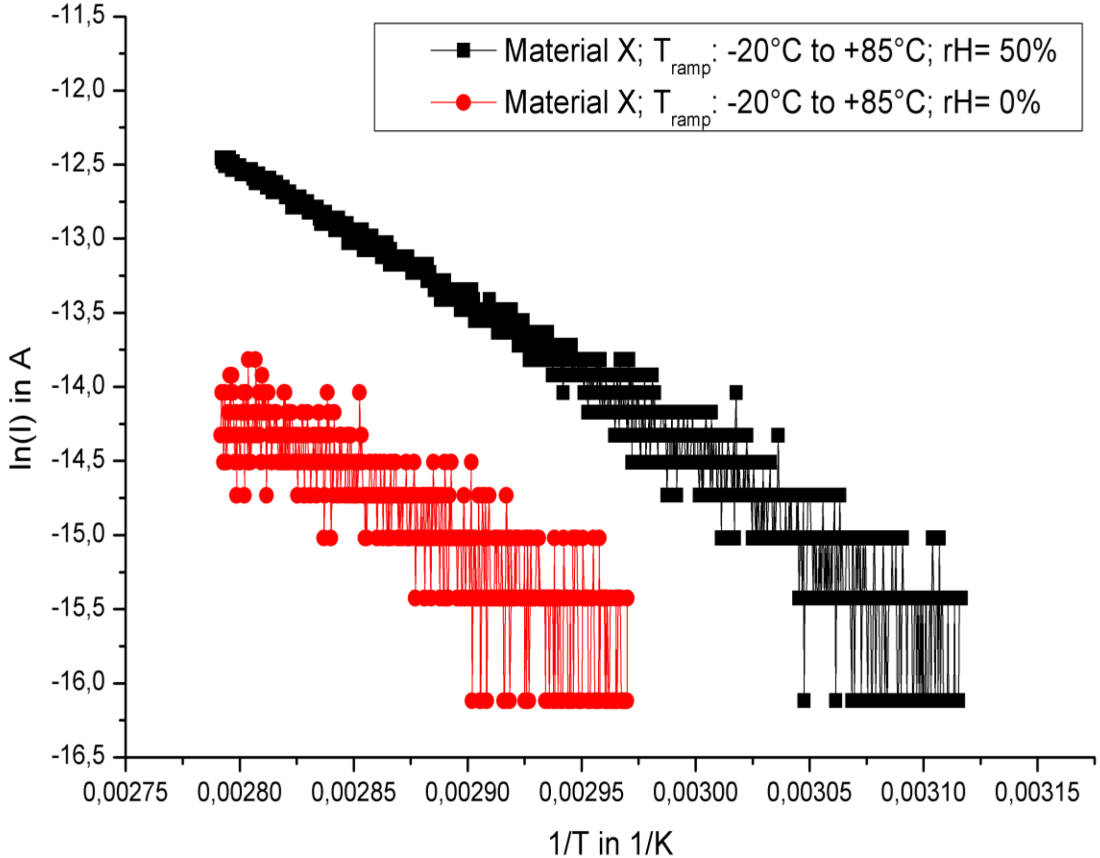
Voltage: 1000V

Temperature: 48°C

Humidity: 50%

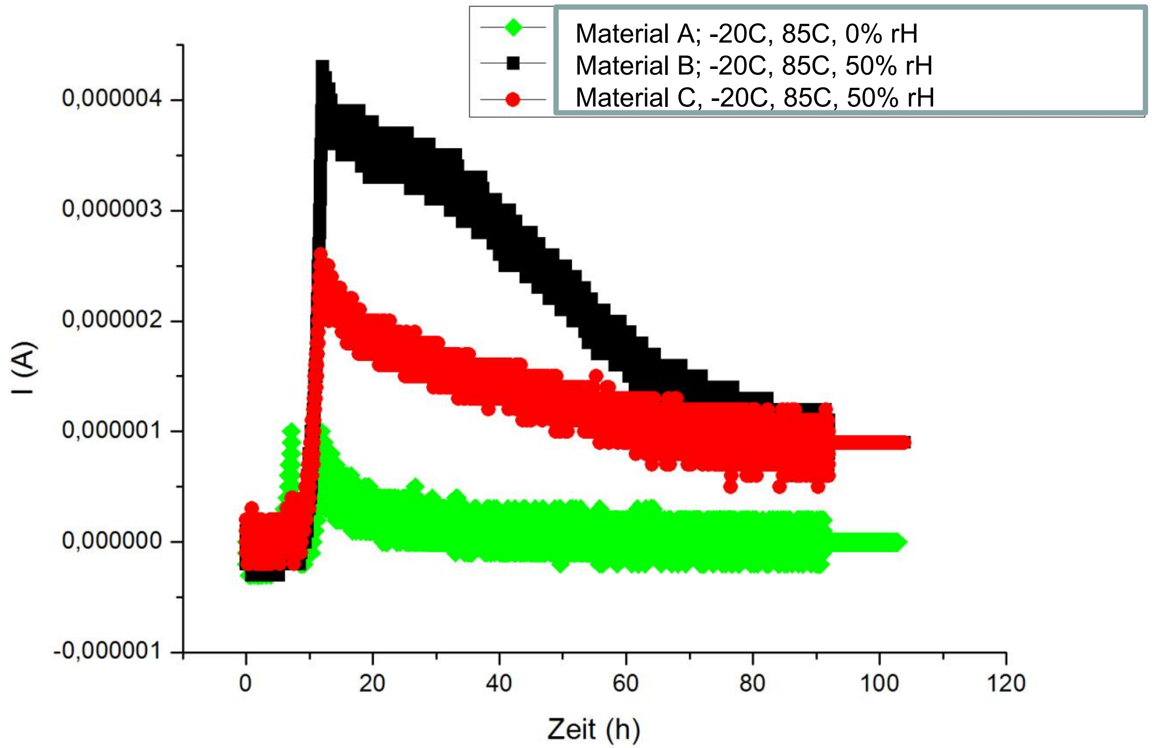
Material: Y

Panel level



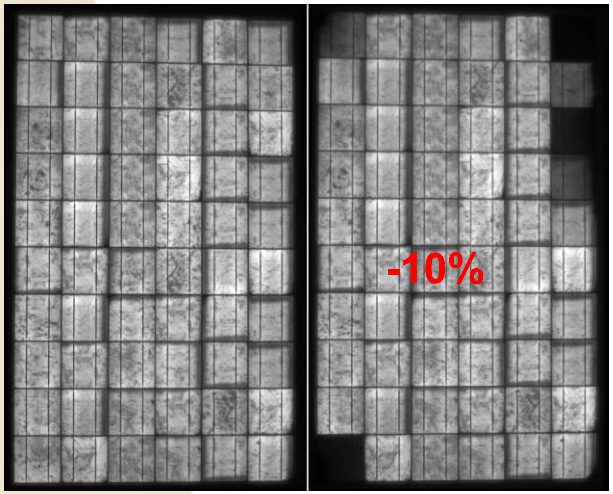
Leakage current and cooresponding PID strongly dependent on temperature and humidity

Panel level



Leakage current and cooresponding PID strongly dependent on temperature and humidity

Temperature and humidity

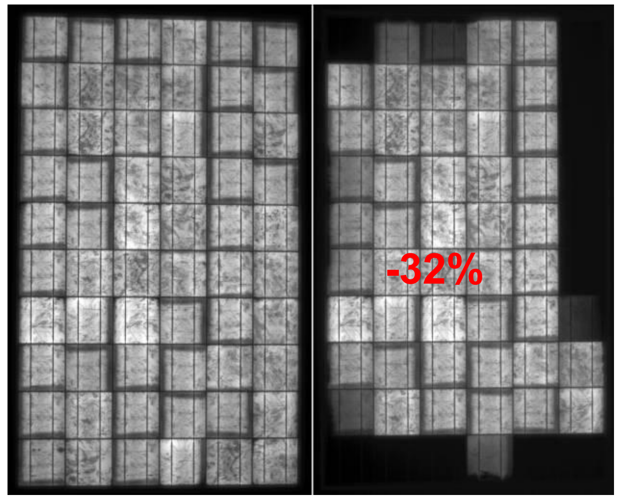


Time: 100h

Voltage: 1000V

Temperature: 85°C

Humidity: ≈ 0%

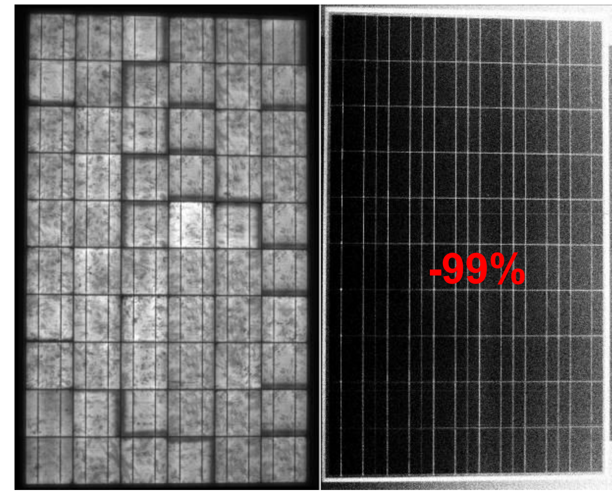


Time: 100h

Voltage: 1000V

Temperature: 85°C

Humidity: 50%



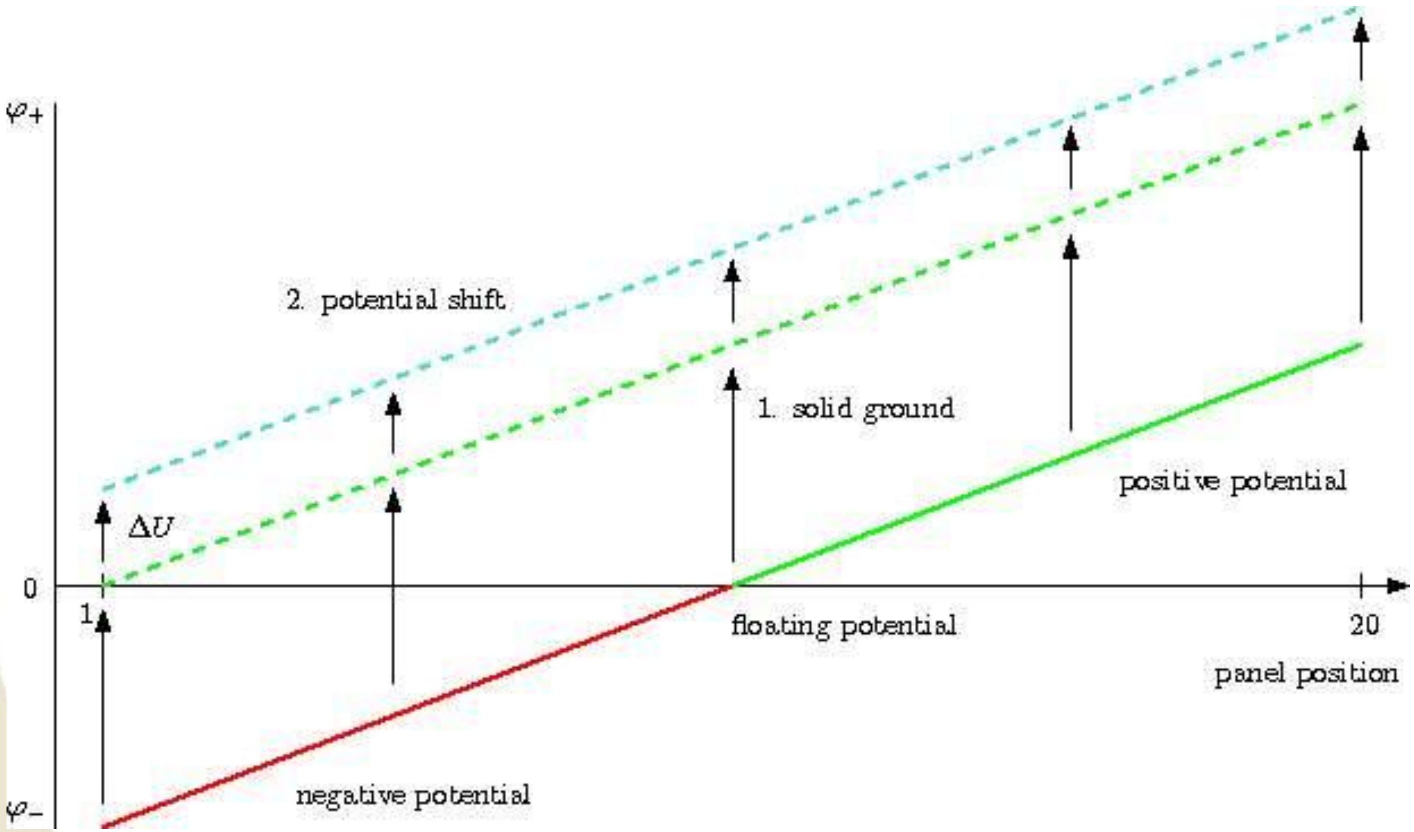
Time: 100h

Voltage: 1000V

Temperature: 85°C

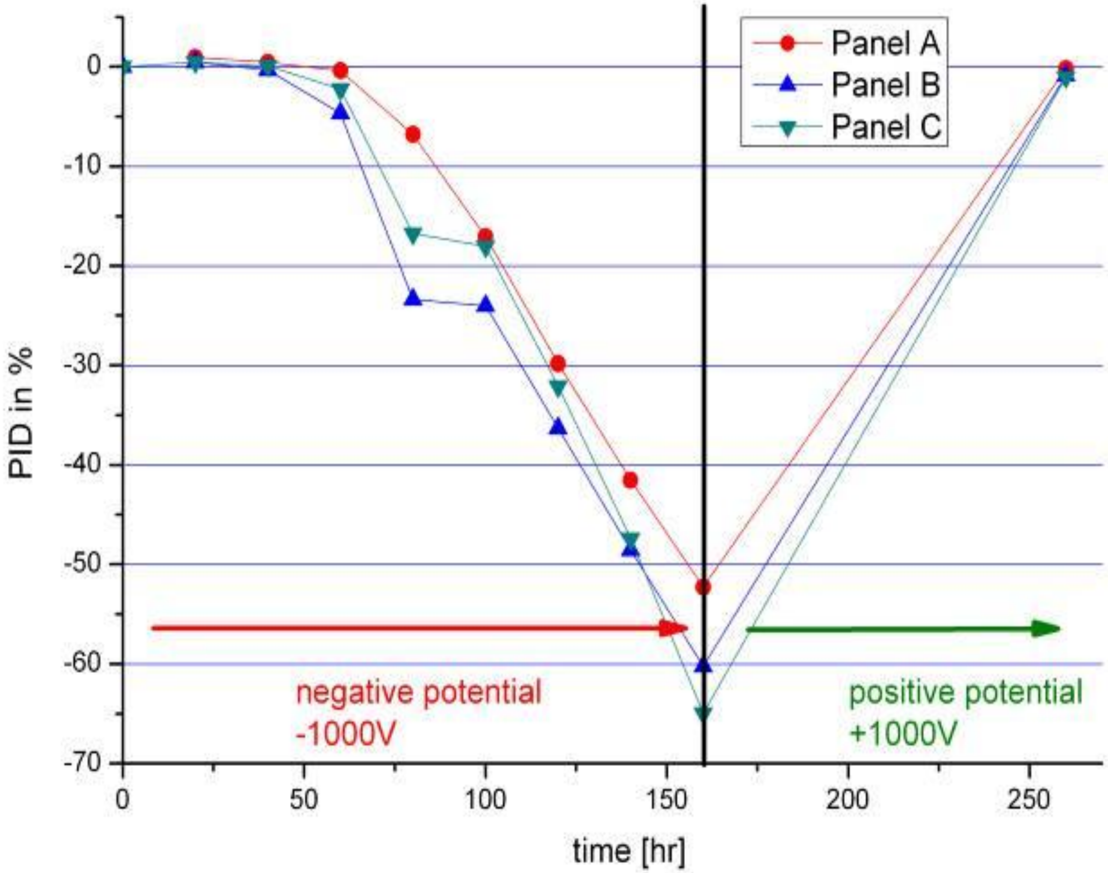
Humidity: 100%

System level



→ Potential relative to ground is determinded by grounding configuration

System level



Degradation and recovery of panels in the lab

PID can be stopped/ reversed by avoiding a negative potential
→ Suitable grounding configuration

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What's next?

How do laboratory results correlate to real life?

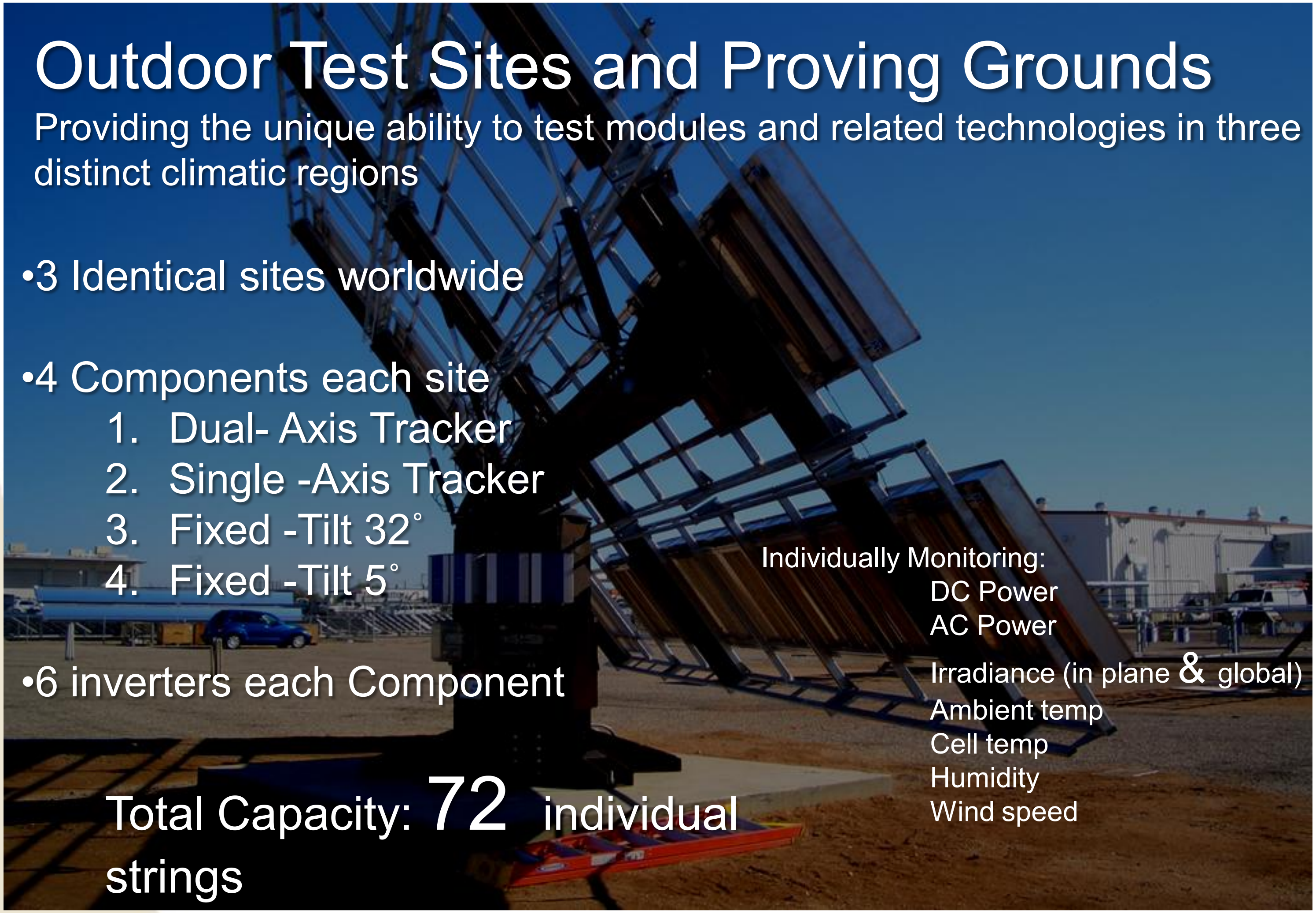
The concept:

- 2 different types of "laboratory proven" PID panels
  - High PID tendency
  - Low PID tendency
- 3 different climatic regions

The need:

- 3 identical test sites in 3 different regions

Global Test Site Network



Outdoor Test Sites and Proving Grounds

Providing the unique ability to test modules and related technologies in three distinct climatic regions

- 3 Identical sites worldwide
- 4 Components each site
  1. Dual- Axis Tracker
  2. Single -Axis Tracker
  3. Fixed -Tilt 32°
  4. Fixed -Tilt 5°
- 6 inverters each Component

Total Capacity: 72 individual strings

Individually Monitoring:

DC Power
AC Power
Irradiance (in plane & global)
Ambient temp
Cell temp
Humidity
Wind speed

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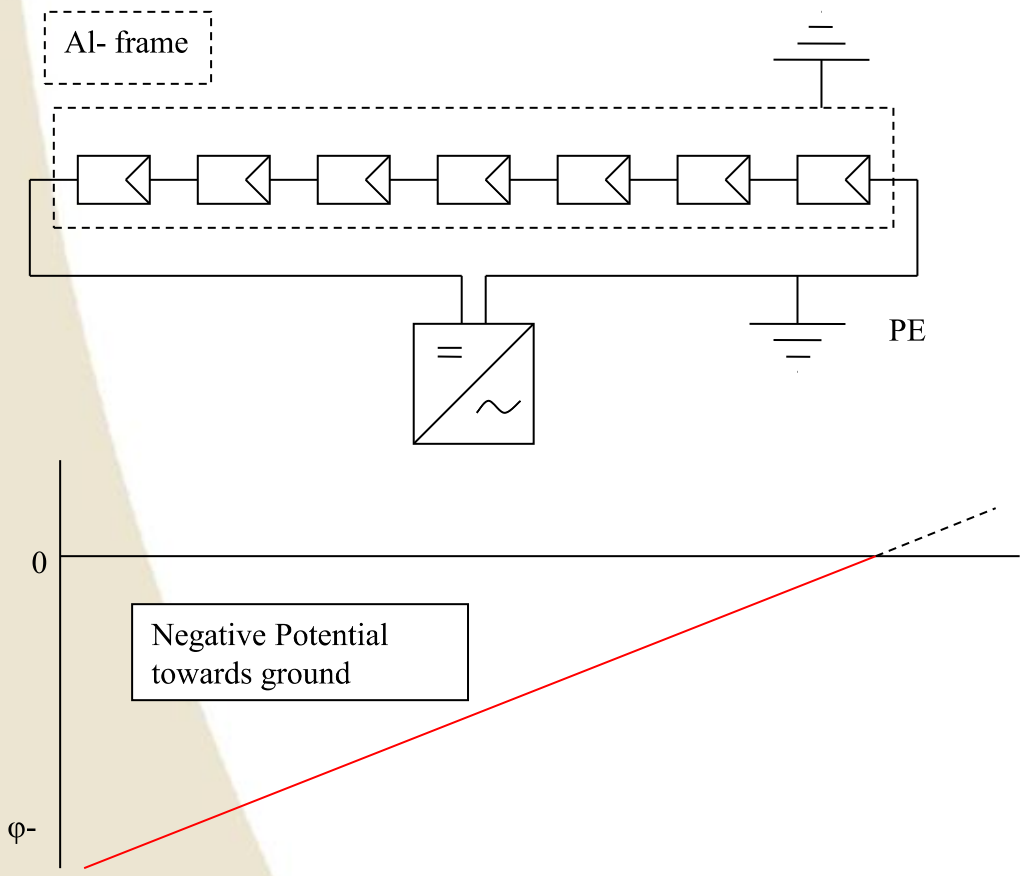
Global Test Site Network – The Locations

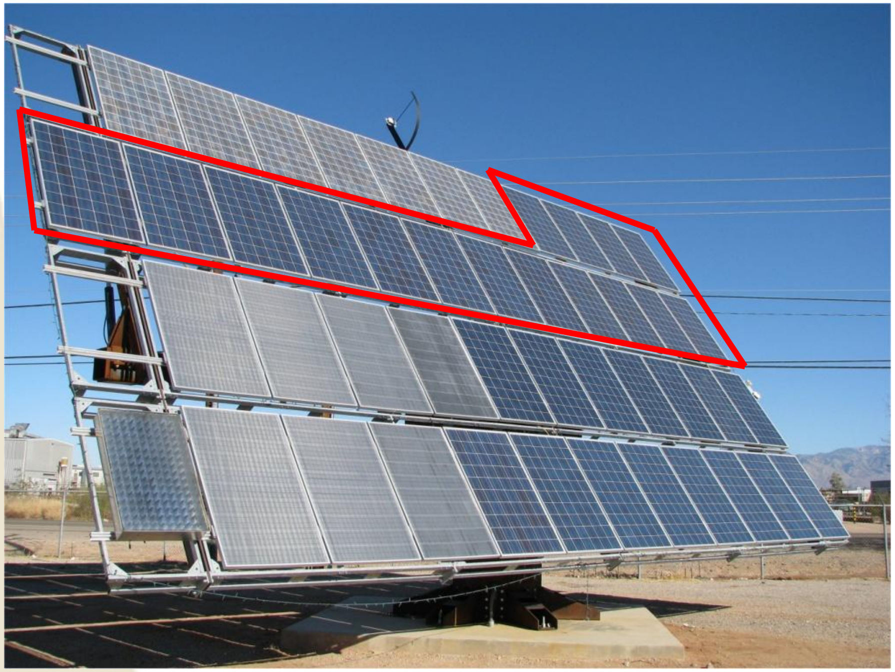
What's next?

Setup on test sites:



- 3 test sites with identical system configuration and technology
- 2 strings of 7 modules each site – total 6 strings
- Two different materials (high and low PID tendency)
- Positive pole is grounded to simulate the worst case scenario
- Meteorological stations log environmental conditions at the different test sites

What's next?



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What's next?

Solar Cell Level

→ Cooperation with different cell suppliers to modify the ARC according to cell spec

Module Level

→ Electrical characterization of encapsulation foils with high and low PID prevention

System Level

→Evaluating suitable inverter suppliers and proposed solutions

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Content

Summary and Conclusion

- Origin of PID: Properties of solar cell
  → PID can be excluded/minimized on cell level
  → ARC

- Leakage current on panel level key feature for PID
  → PID can be excluded/ minimized on panel level
  → Encapsulation

- Sign and magnitude of the external potential critical for PID
  → PID can minimized on system level
  →Grounding

- Avoiding PID on panel level favourable since
  → Independent of cell technology
  → Independent of system / grounding configuration

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Thank you for your attention!

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