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Failure Modes of CPV Modules and How to Test for Them

19-Feb-10

This presentation does not contain any proprietary or confidential information.

- **Intro**
 - This talk will include both failure modes we have detected at Emcore along with the techniques that we have used to reveal them.
 - The Issues Matrix will guide the discussion and is loosely modeled after the IEC 62108 CPV systems qualification standard.
- **Damp heat cell failures**
 - Easily detectable in EL.
 - Electrolytic corrosion (also a wet insulation issue).
 - Lens warp.
- **Thermal Runaway**
 - ESD
 - Thermography
 - Vaporized ribbons,
- **Power Thermal Cycle**
 - Many assume this means $1.25 \times I_{sc}$ but this leads to very high junction temperatures
 - Also too hard on the DBC (CSLM failure)
- **Melting Coverglass**
- **Summary**

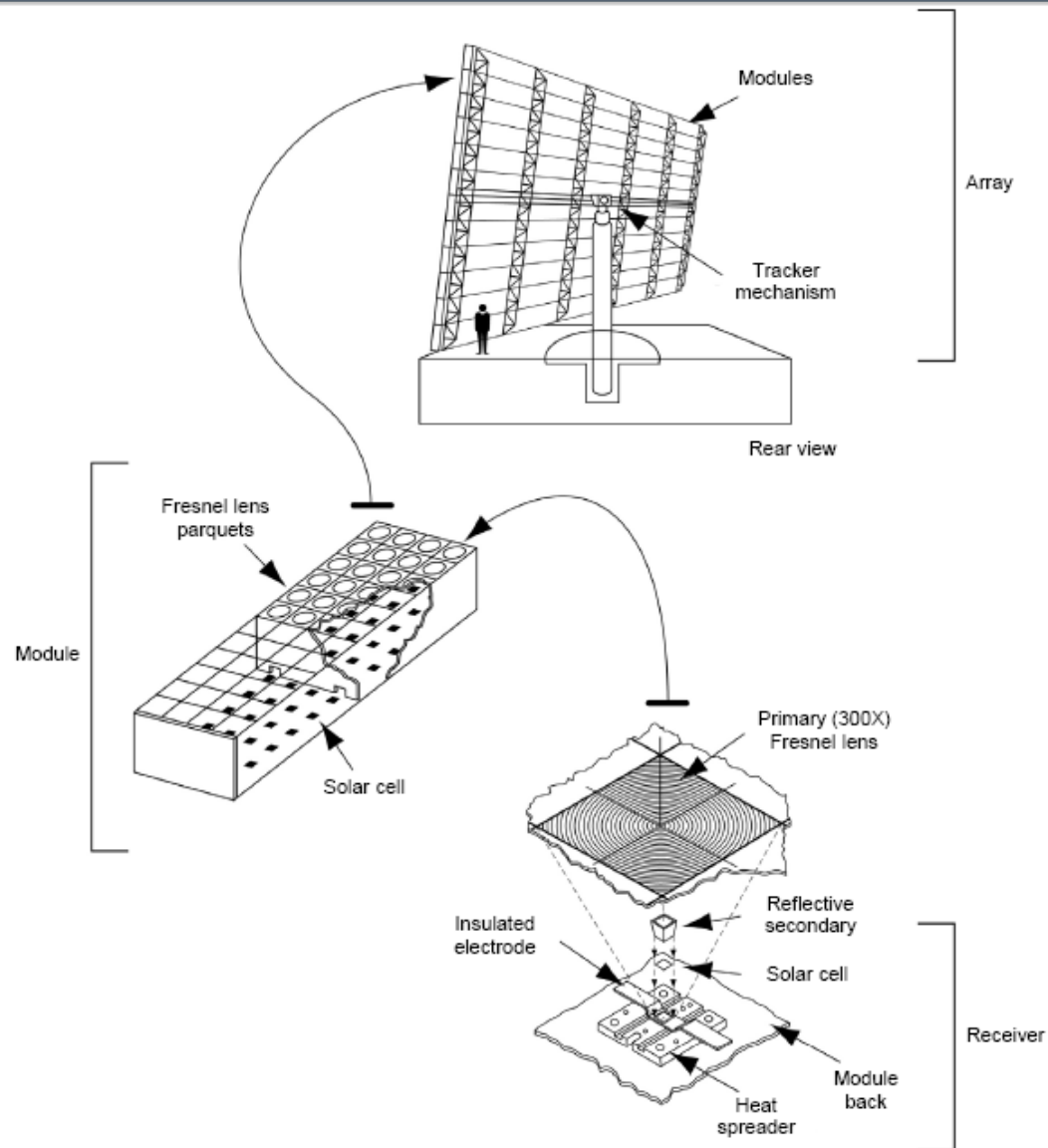
Emcore's Latest Gen II Installation



Gen III



Point-focus Fresnel Lens HCPV System (IEC 62108)

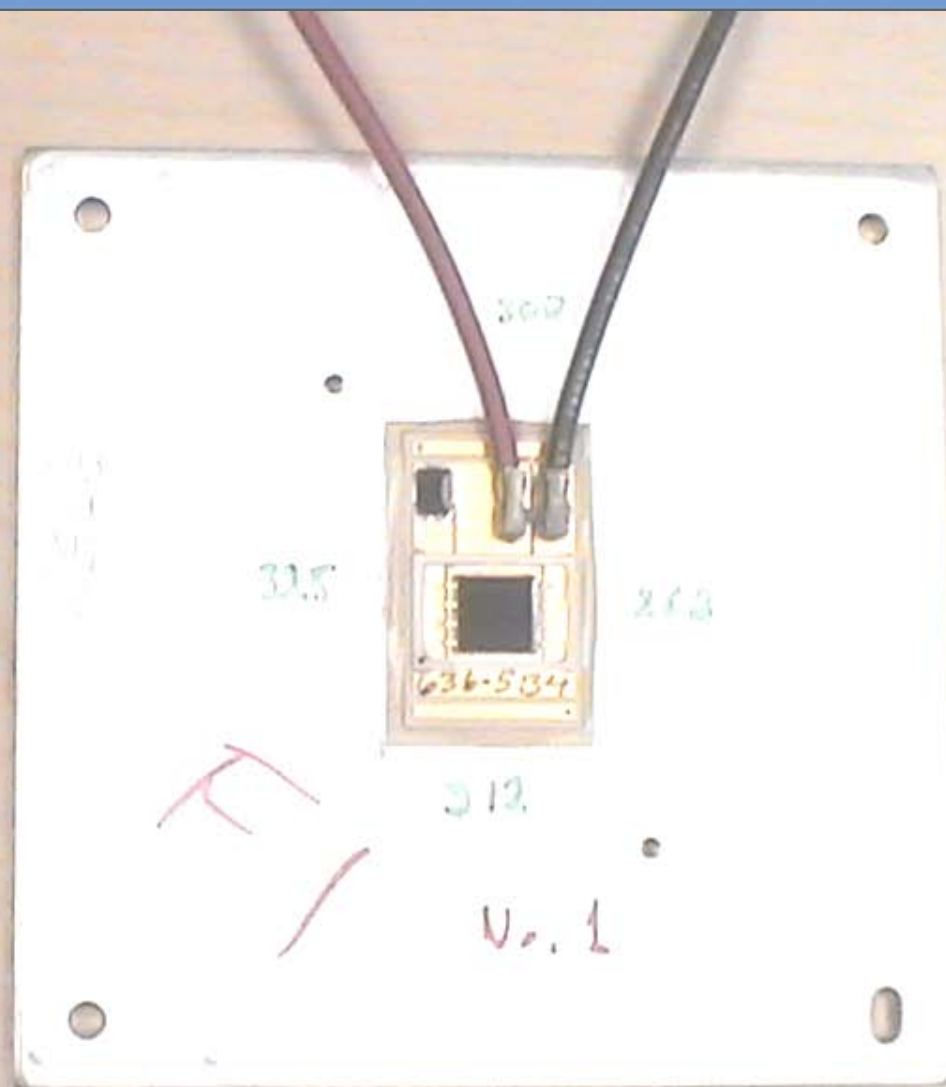




Bare Cell
or
Device

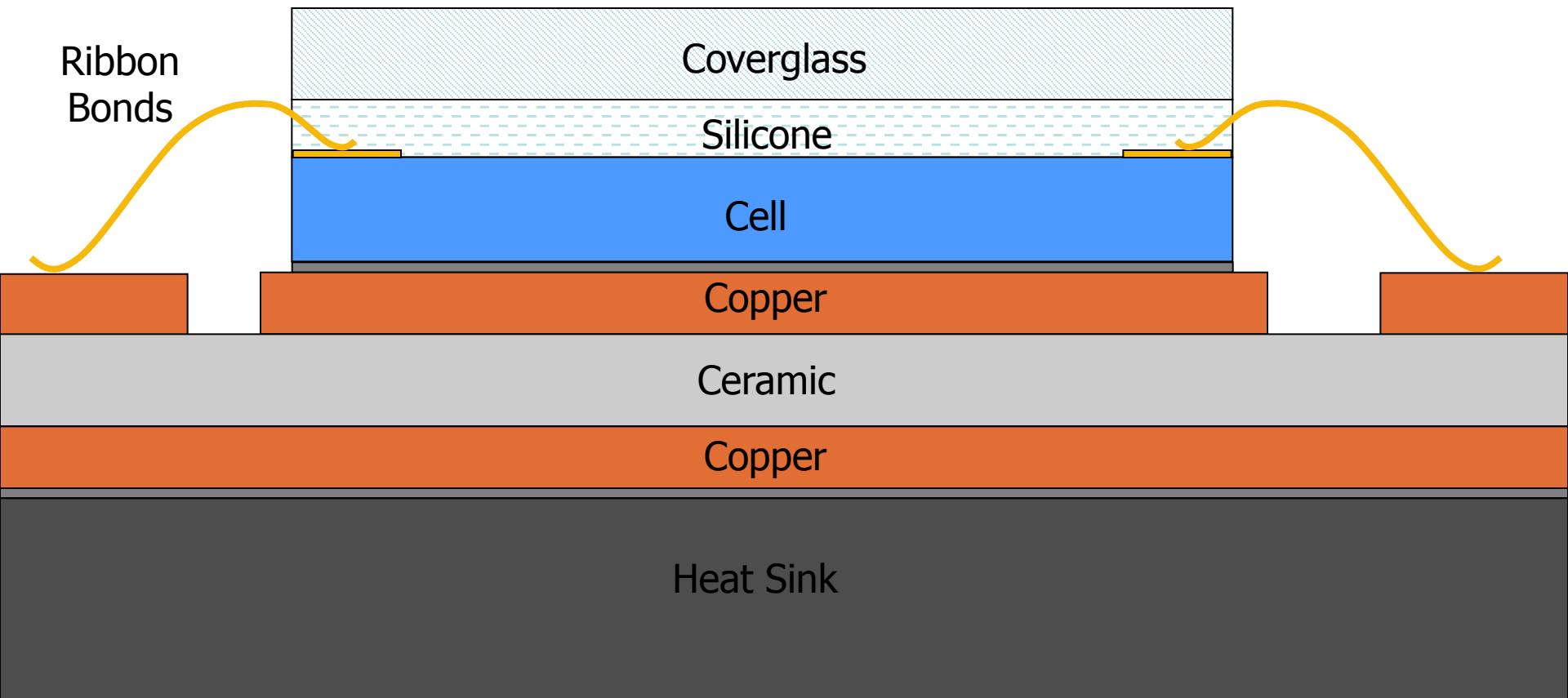


Receiver
(Rx)



Receiver Assembly

Rx Cross Section



CPV Module Reliability Issue Matrix

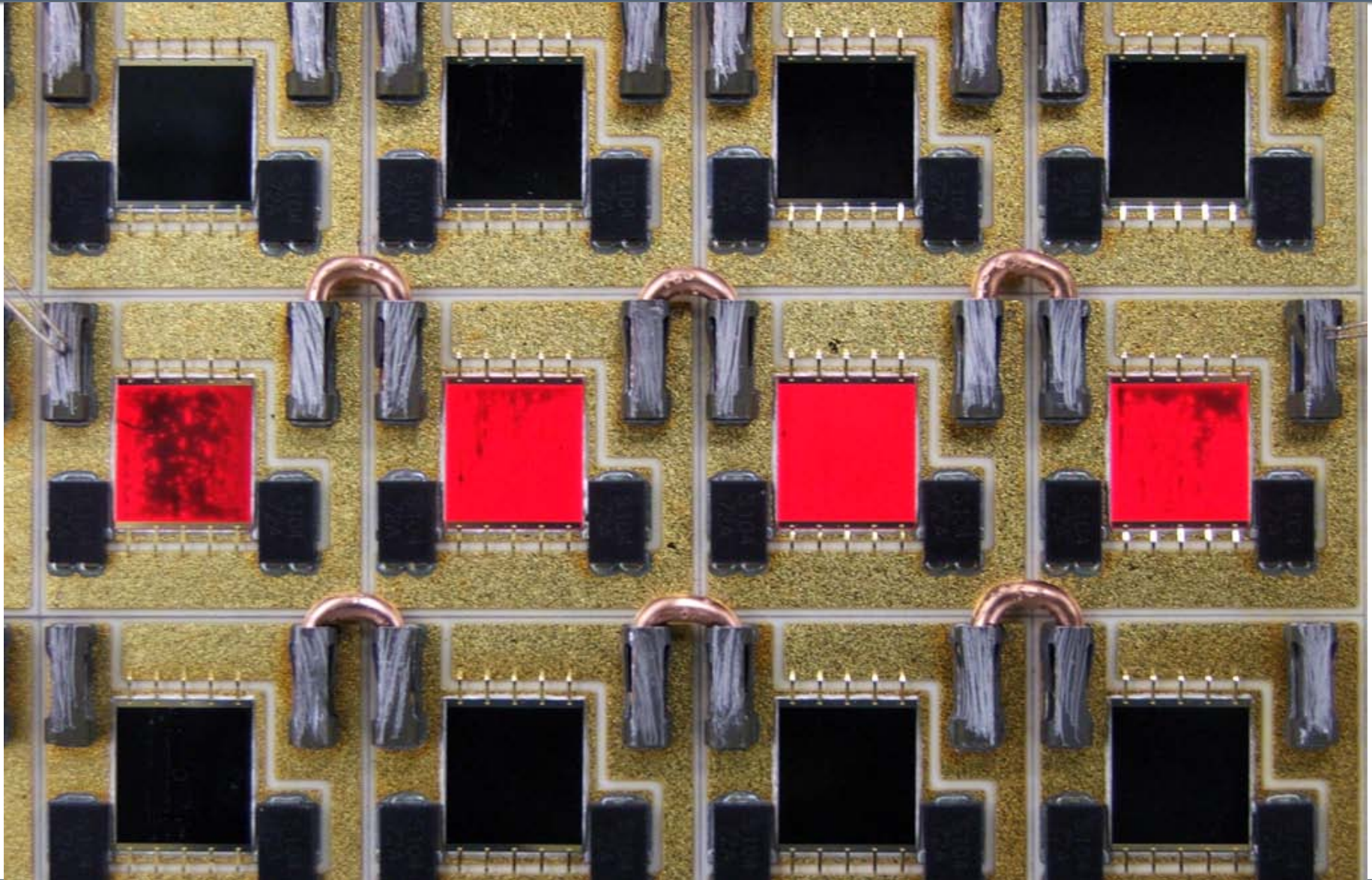
	Cell	Reciever	Reciever Subassembly	Module
Damp heat	Cell Corrosion		Electrolytic corrosion	Acrylic Lens Warp
Wet insulation			Must pass at Rx level for non-hermetic modules	
Dry Insulation				Hard Shorts
Outdoor Exposure		Melting coverglass	Yellowing of encapsulants	
Damp Freeze			Rx attach failures	
Power Thermal Cycle	Thermal Runaway	DBC Conchoidal Fracture		
ESD	Bare cells vulnerable			

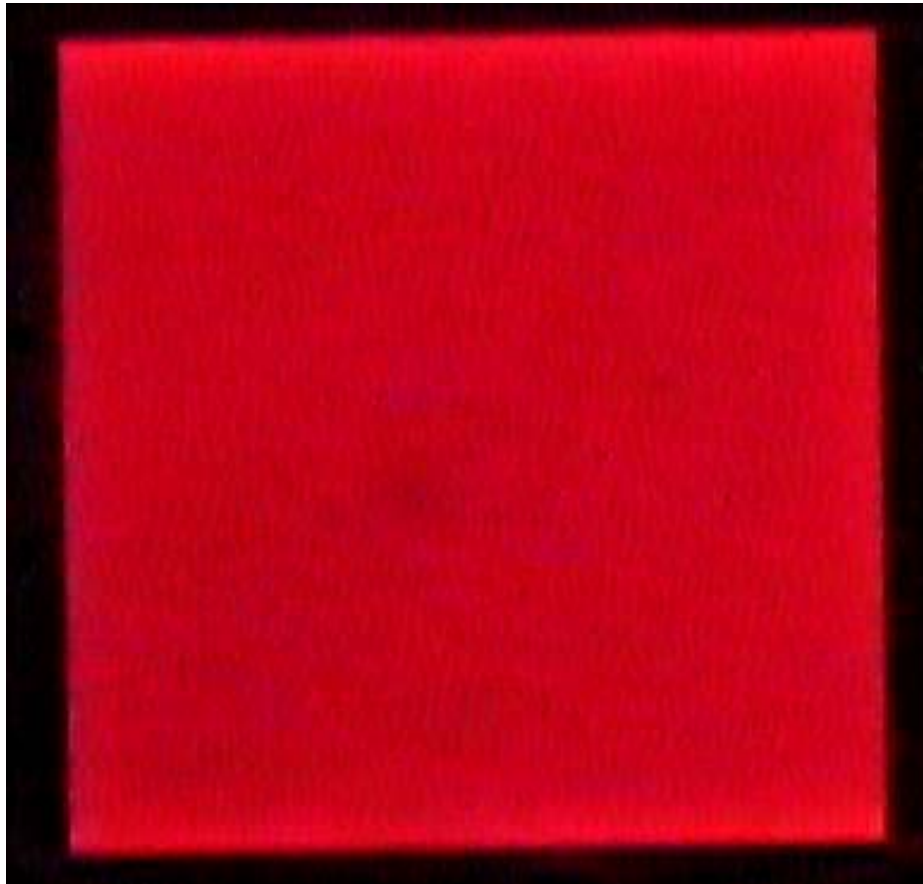
- One of the really cool features of current III-V compound semiconductor multi-junction solar cells is that if you run them backwards they make a pretty good LEDs!
- The top junction is the most spectacular because it is visible with the naked eye, but the other two junctions also emit.
- This makes EL a powerful analysis technique at all levels of CPV system assembly.



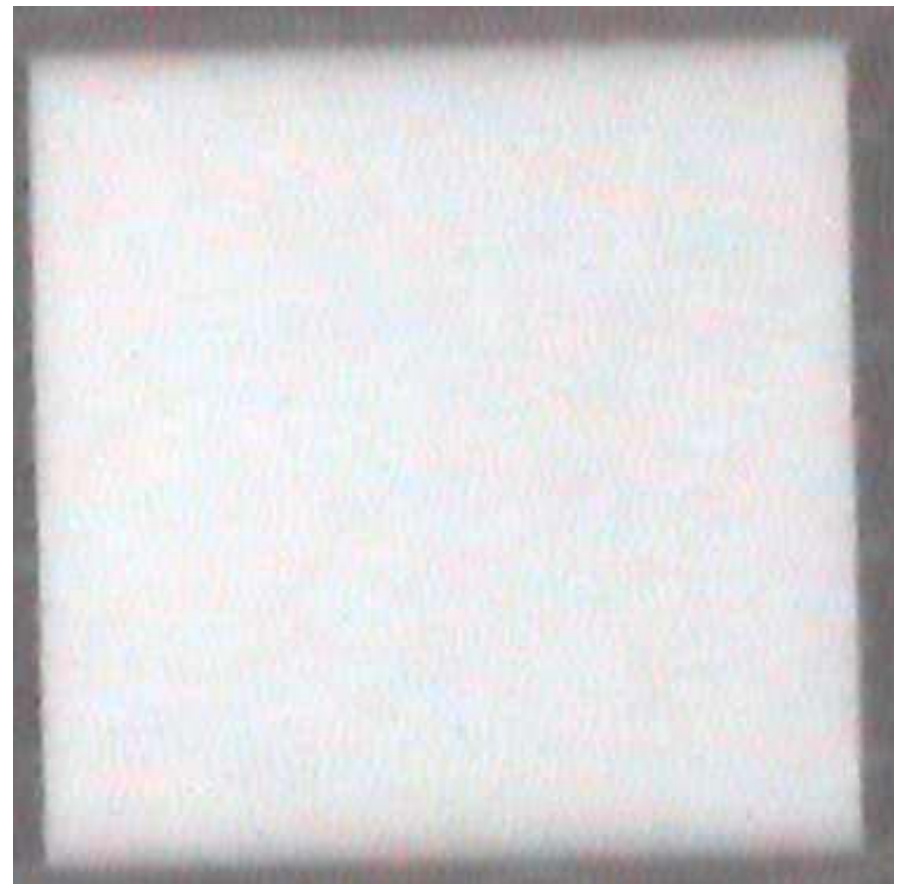
Damp Heat

TC EL After Damp Heat Exposure





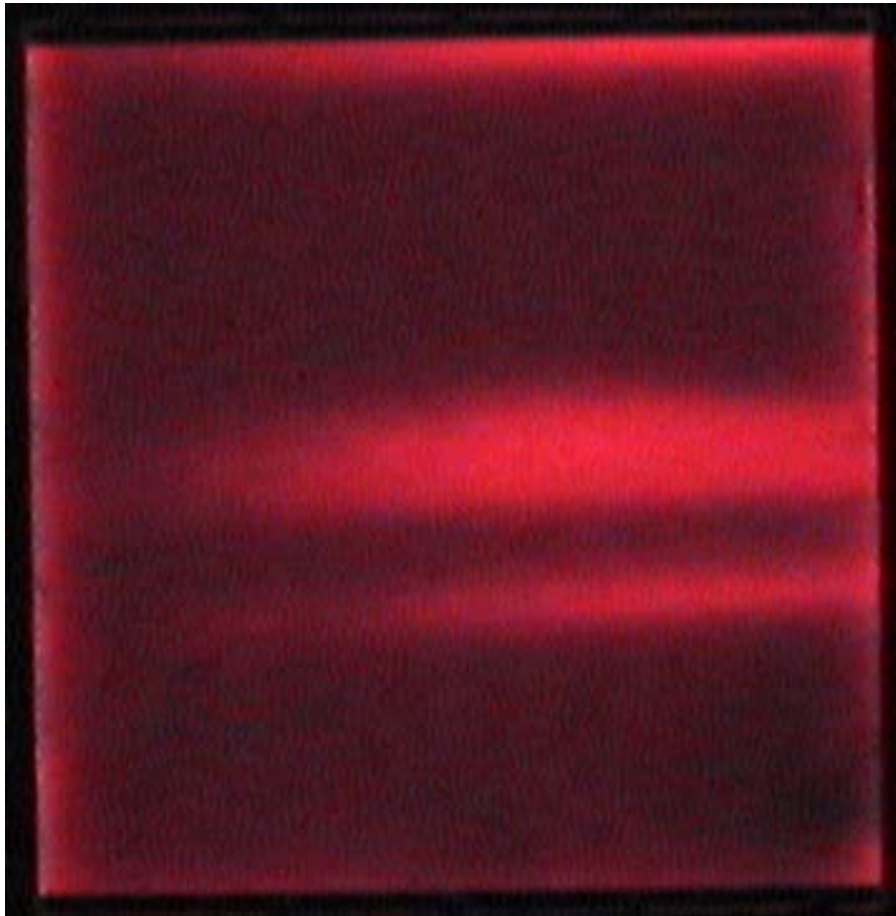
Top Junction



Middle Junction

- **Grid Finger Delamination.**
 - Dark areas appear to be aligned along GFs.
- **Degradation of Anti-Reflective Coating (ARC).**
- **Top cell shunting.**
- **Accumulation of opaque surface contamination.**

EL Example of Counter-contrast in TC and MC

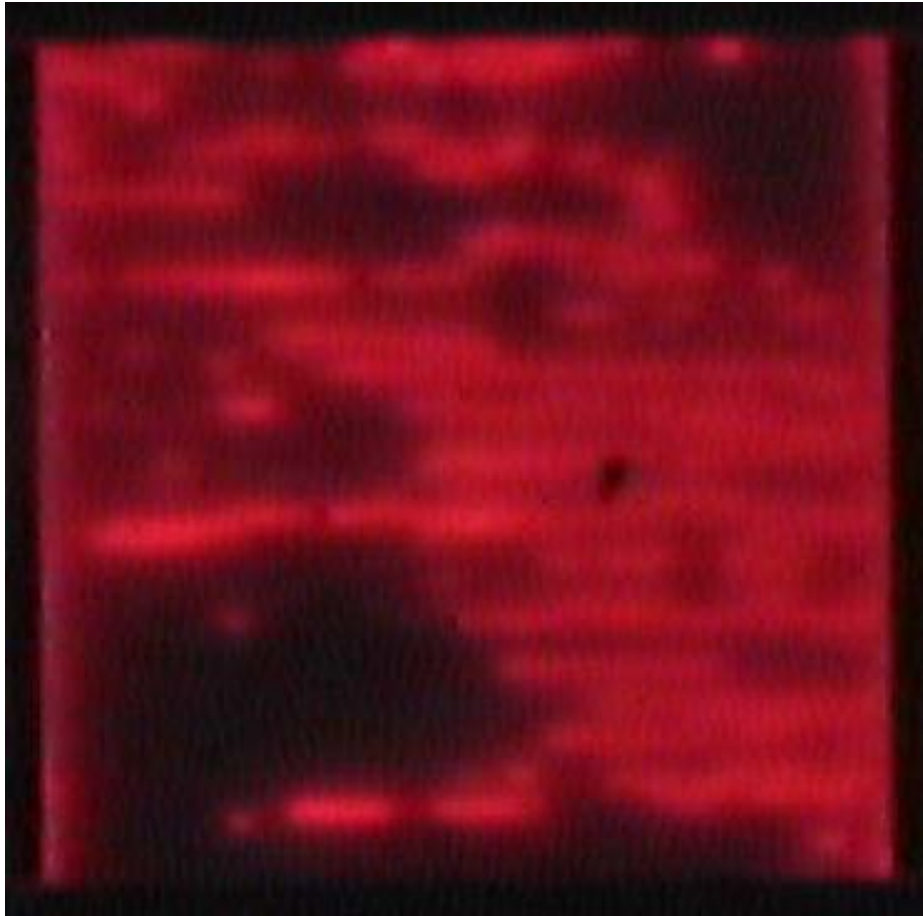


Top Junction

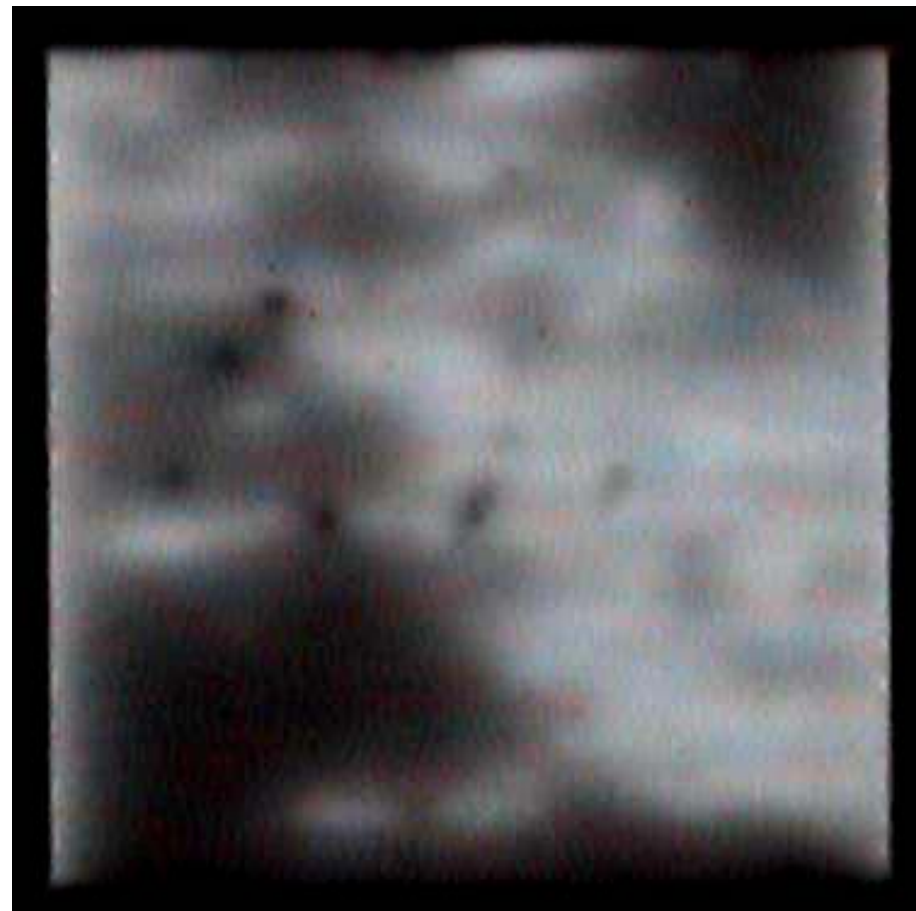


Middle Junction

Multijunction EL Signature of Grid Finger Failure



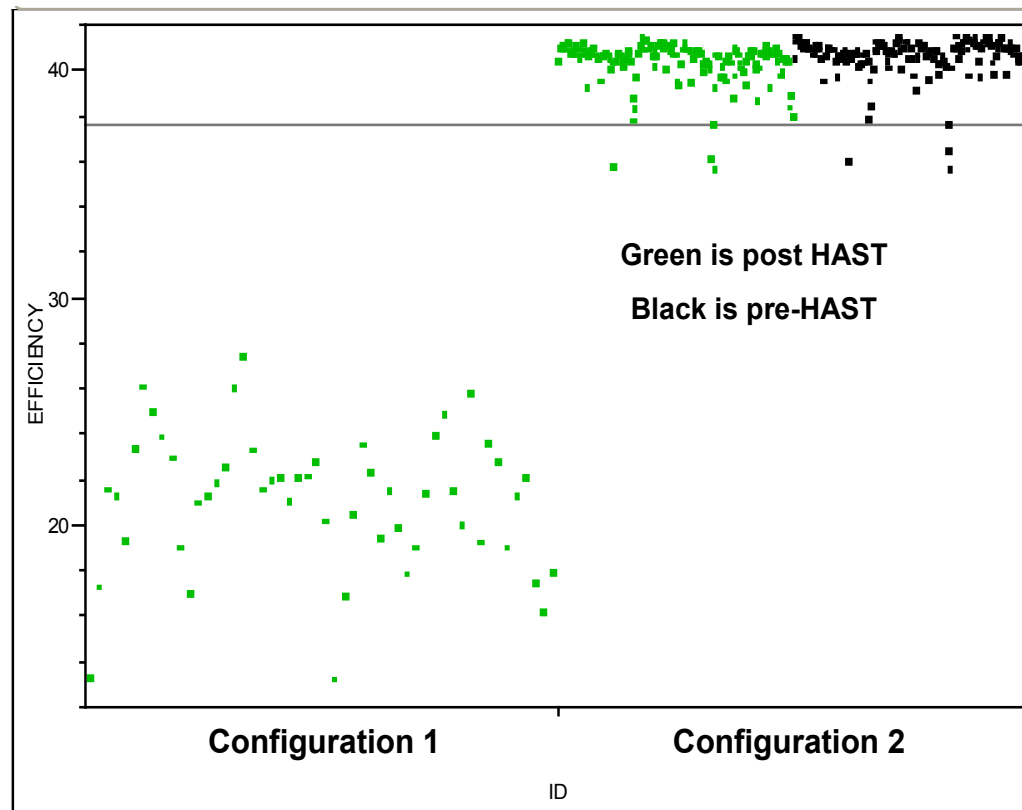
Top Junction



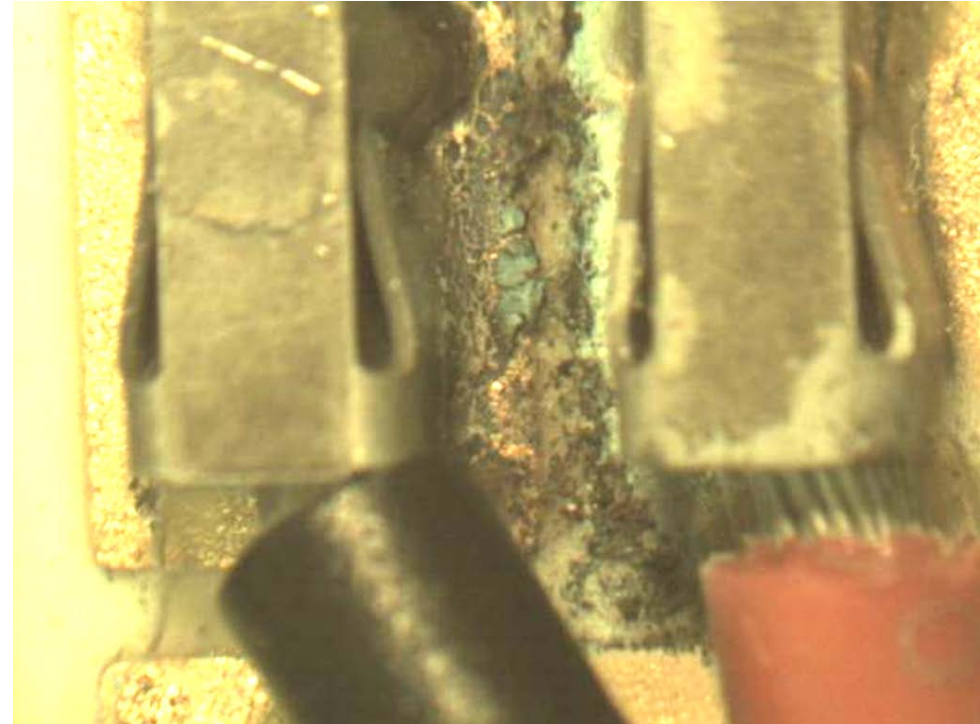
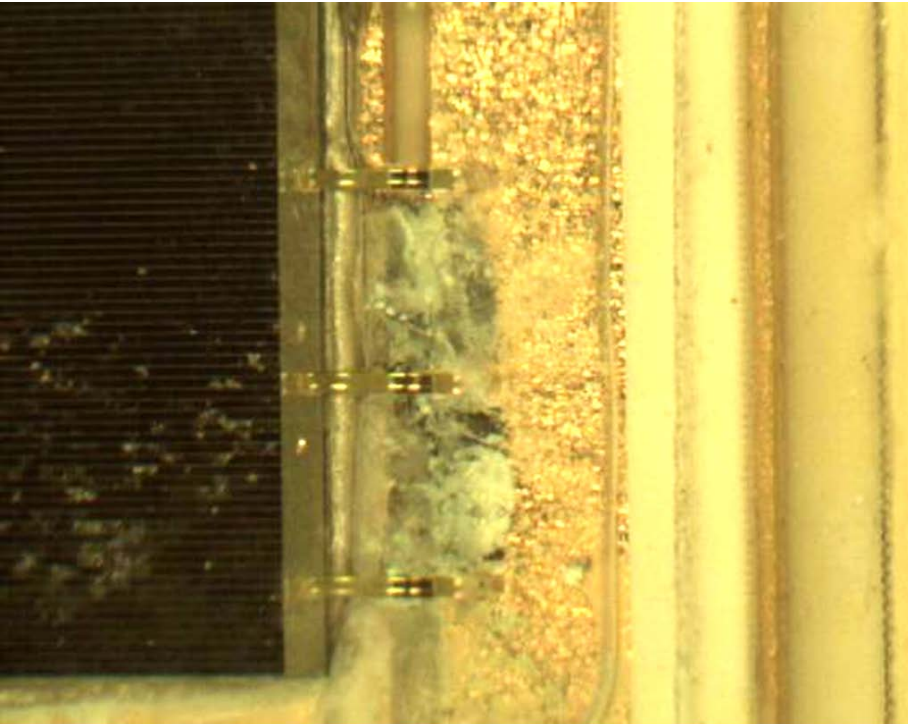
Middle Junction

Bare Cells can now Pass 1k Hrs of 85/85 Exposure

- Based on this experience, Emcore has improved our damp heat resistance at the device level.
- However, passing the 1000 hour IEC damp heat exposure test is no guarantee that bare cells will survive 20 years of exposure to uncontrolled environments.



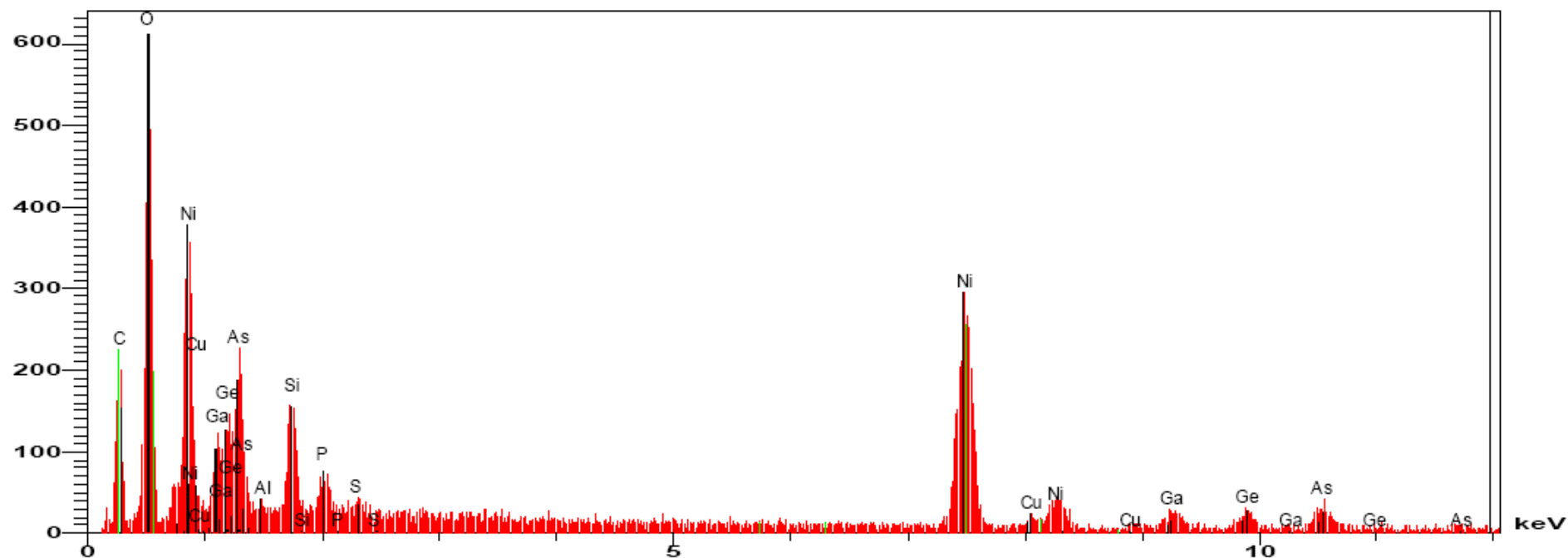
Robust Encapsulation is Critical



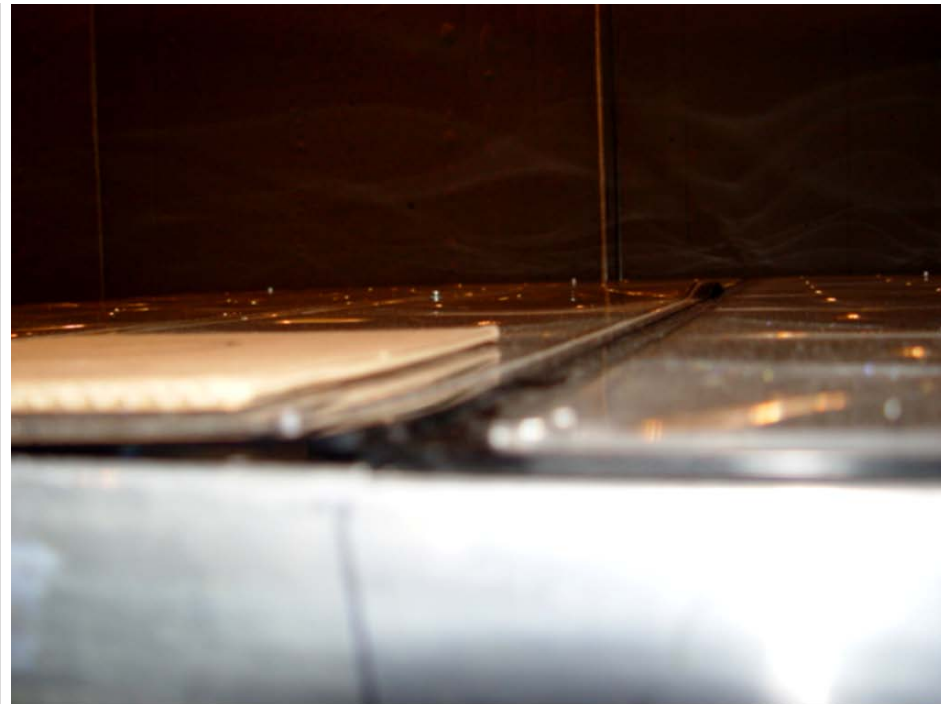
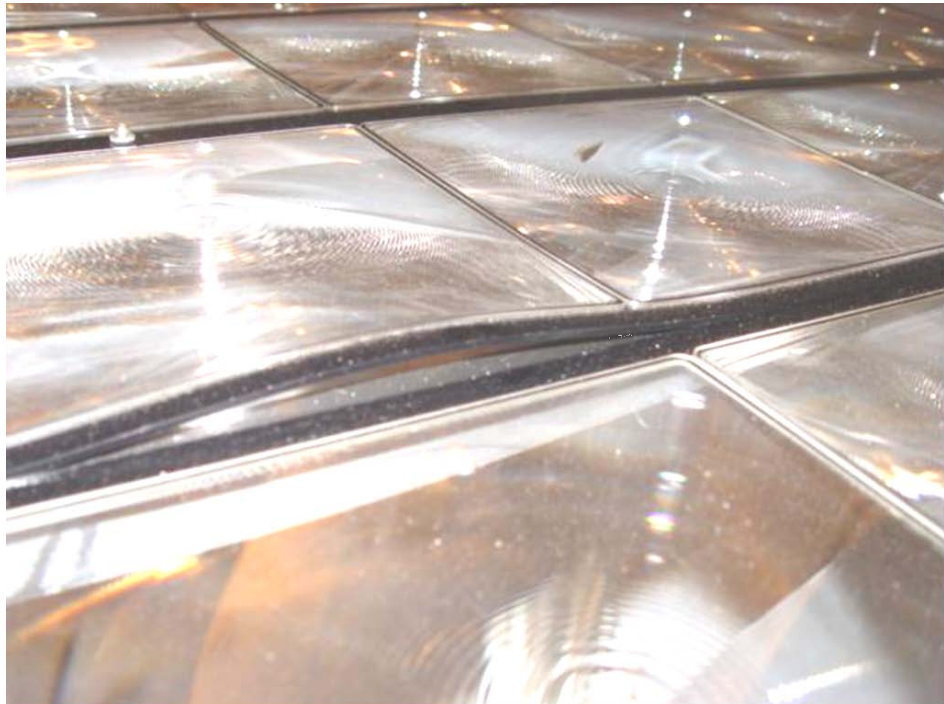
- It appears that this type of failure mode requires both moisture incursion as well as bias.
- For this reason we now add light bias to all our damp heat product reliability testing.
- Moisture incursion also makes it difficult to pass the IEC wet insulation test.

EDX Spectrum from the Blue Goo

L10-A Clip [s0492] 20kV



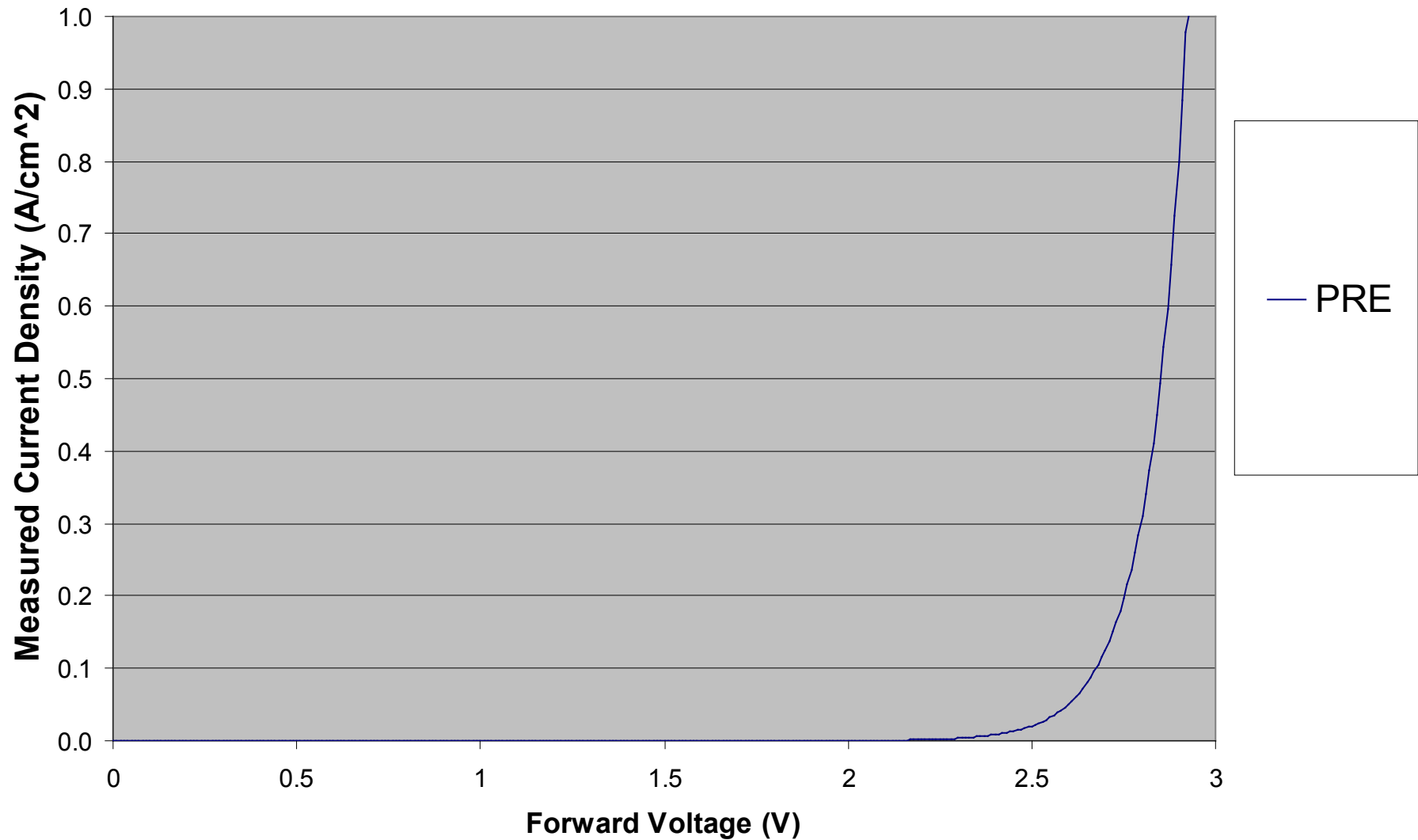
- We have also seen Acrylic lenses deform during damp heat testing.
- Besides the obvious impact to the optical performance of the module, in damp climates this further reduces the chances of passing the wet insulation test when the receiver in the bottom of the module finds itself under water from time to time.



ESD

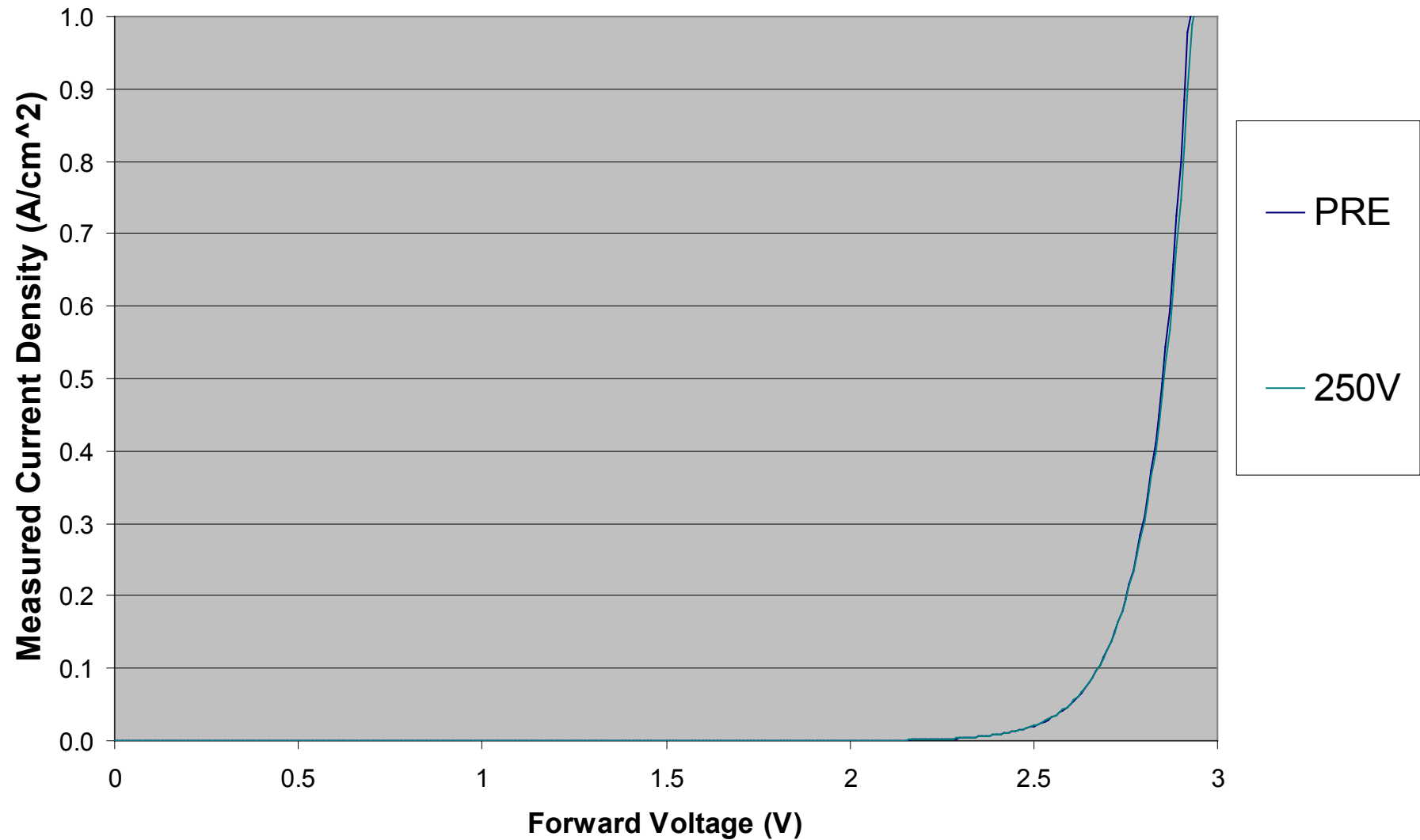
- Through not currently a requirement for IEC qualification of CPV modules, an understanding of the ESD damage threshold of the solar cell is important for establishing adequate ESD mitigation protocols.
- To establish the ESD damage threshold for CPV solar cells we have borrowed from the well established methods used throughout the semiconductor industry (e.g. Mil-STD-883 and JSTD-22a114).
- The following slides illustrate the technique through a series of non-illuminated (dark) current vs voltage characteristics (DIV) for a solar cell that has been subjected to increasingly medieval levels of ESD stress from a Human Body Model (HBM) simulator.
- The reason these data are presented here is mostly as background for the following section on thermal runaway, but ESD may also be implicated in a reported low level infant mortality rate for multijunction solar cells in CPV applications.

HBM ESD Stress Test DIV Curves



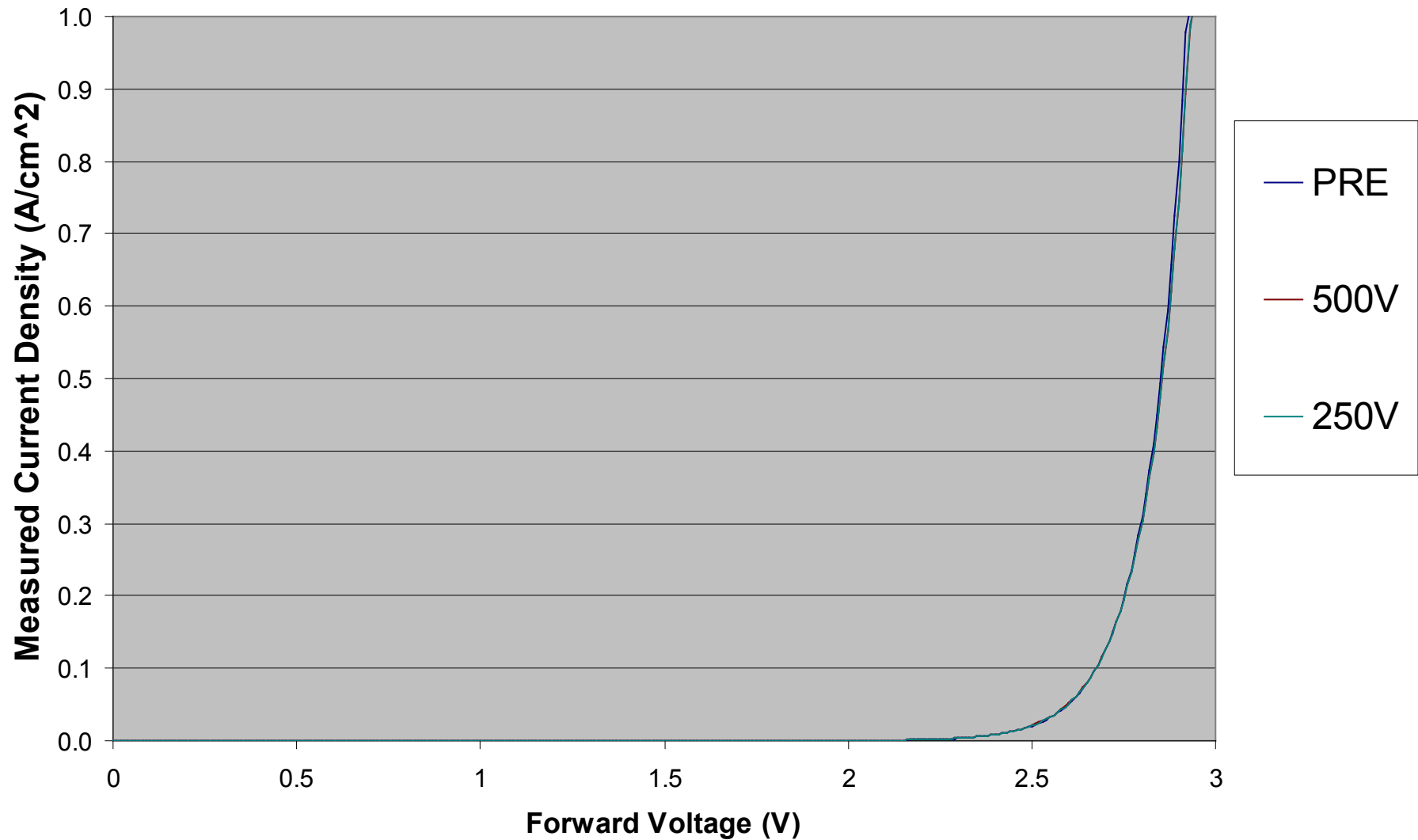
250 V

HBM ESD Stress Test DIV Curves



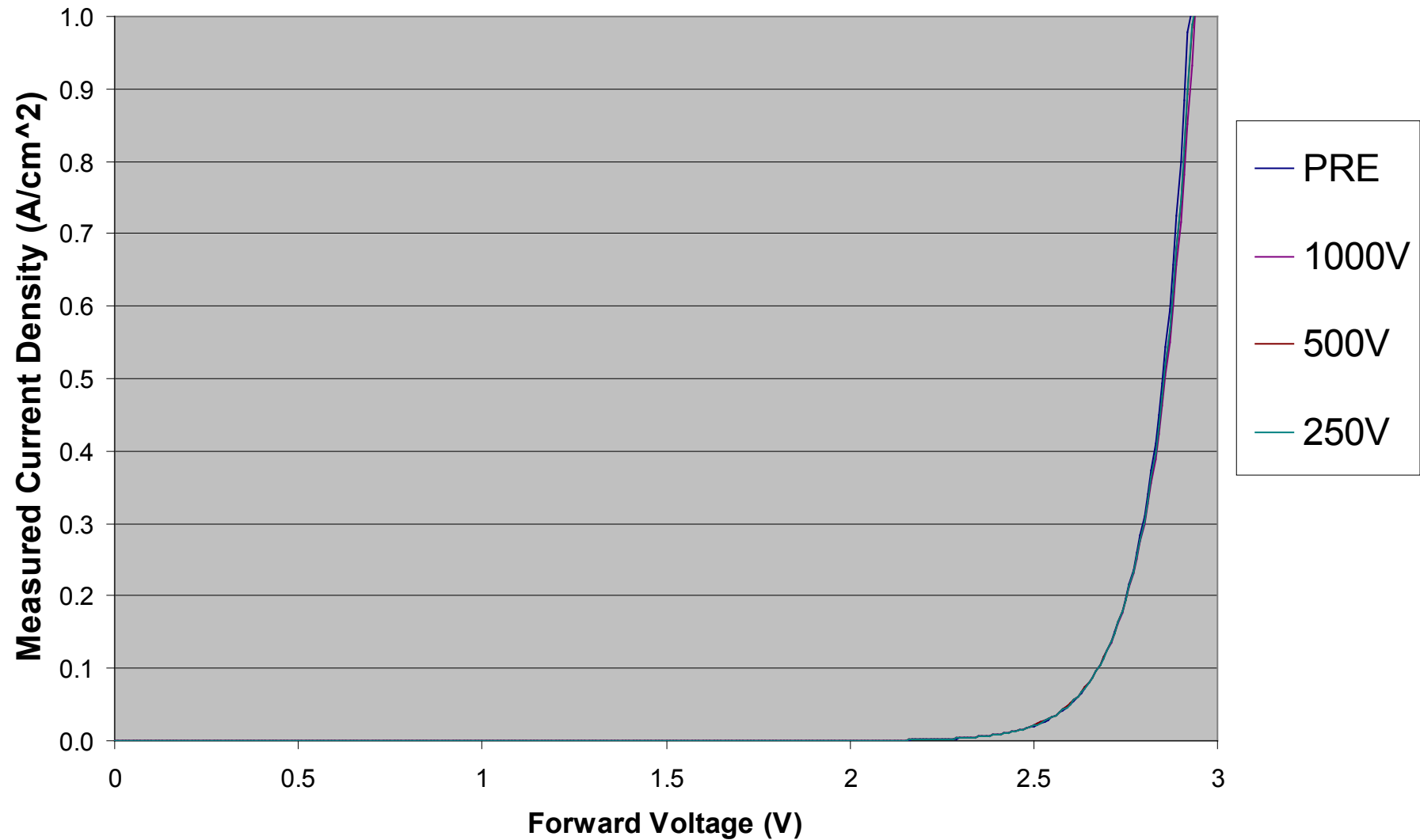
500 V

HBM ESD Stress Test DIV Curves



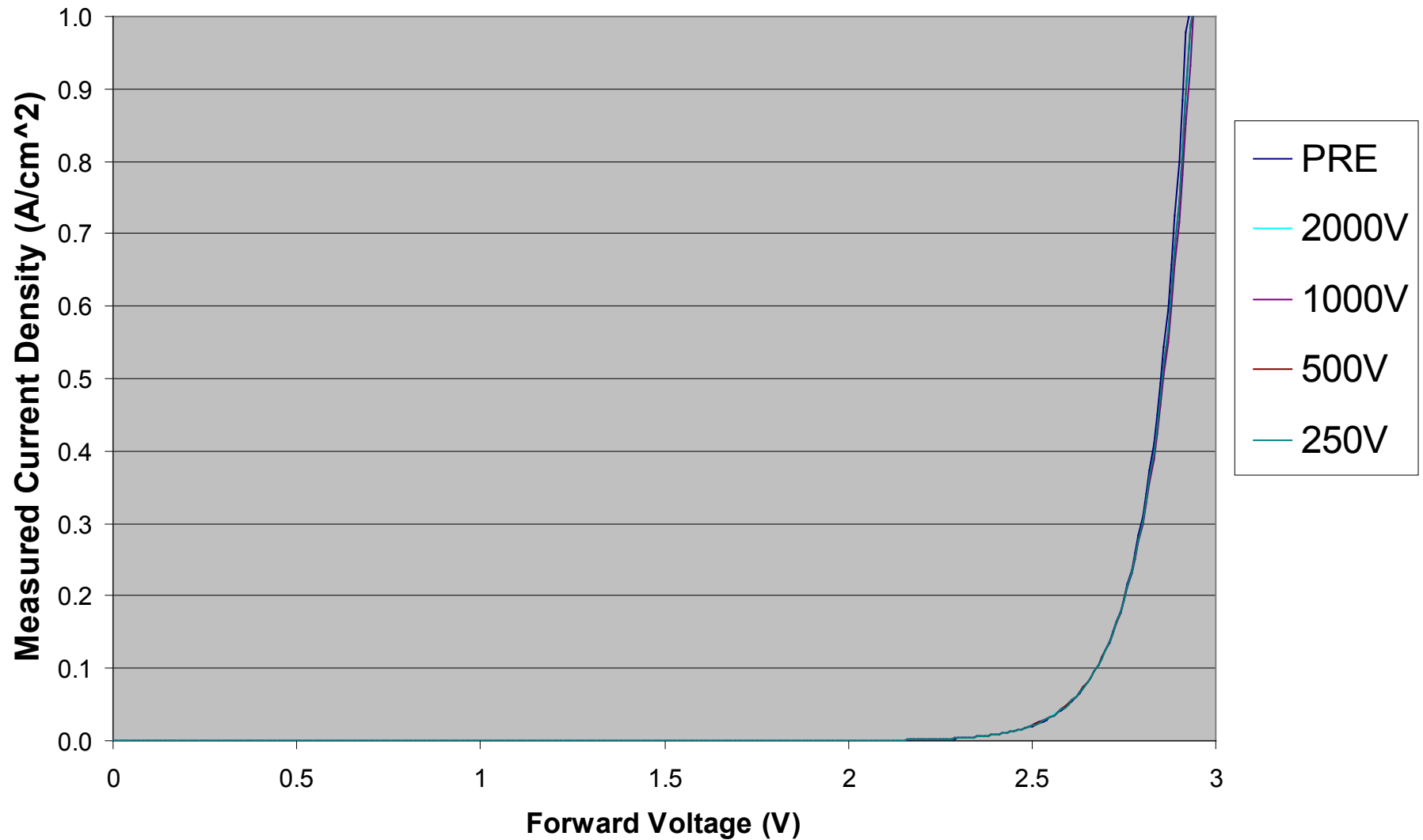
1 kV

HBM ESD Stress Test DIV Curves

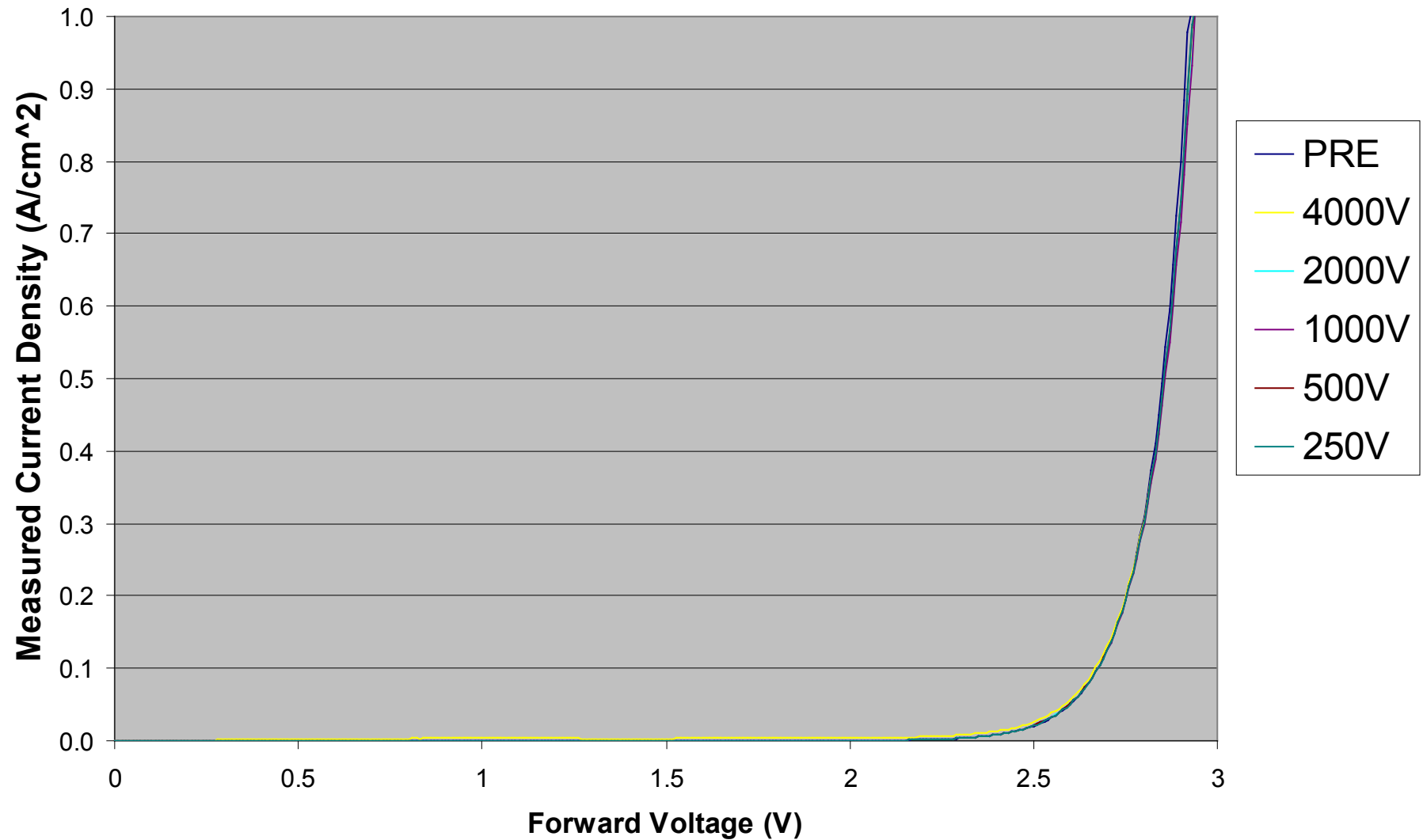


2 KV

HBM ESD Stress Test DIV Curves

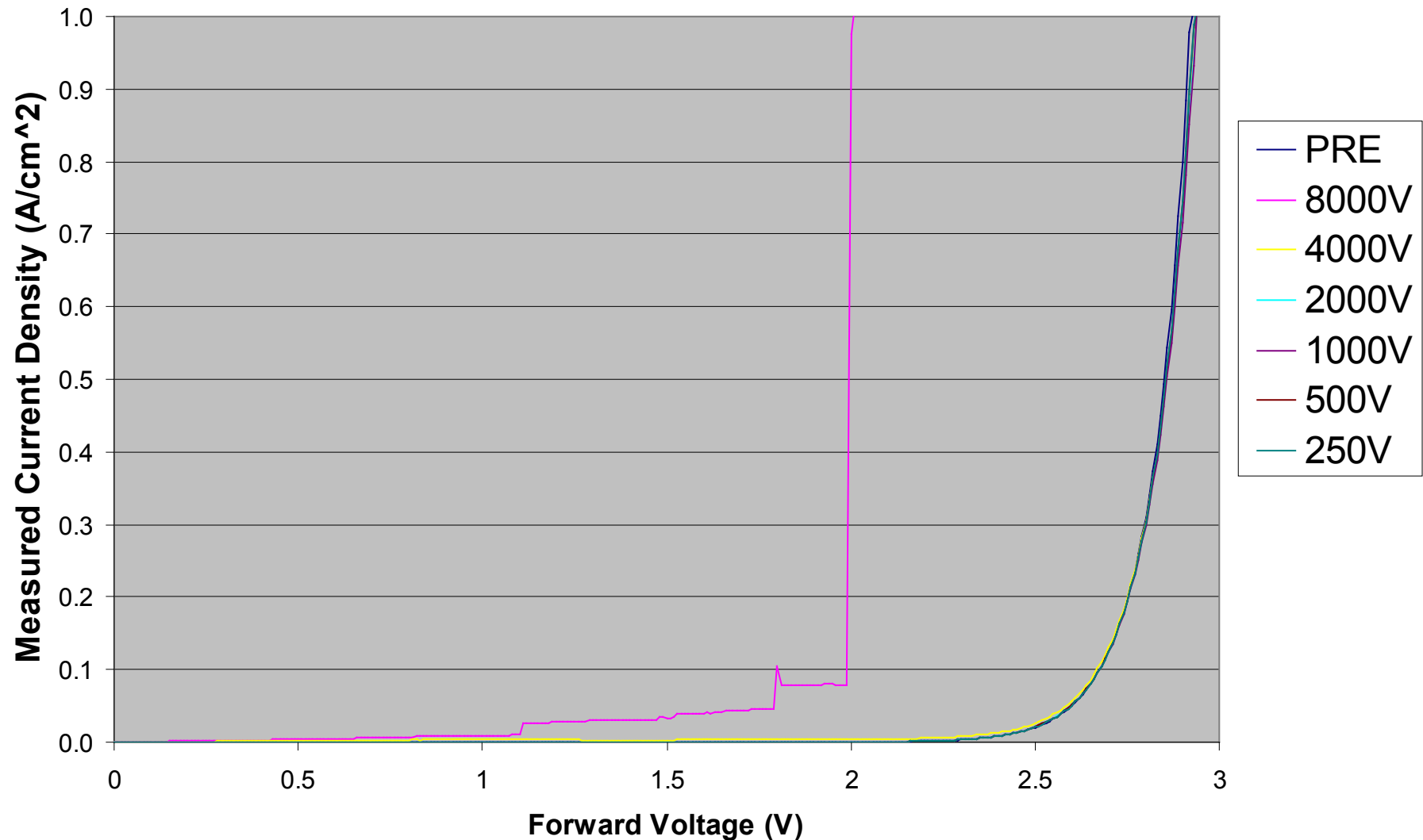


HBM ESD Stress Test DIV Curves



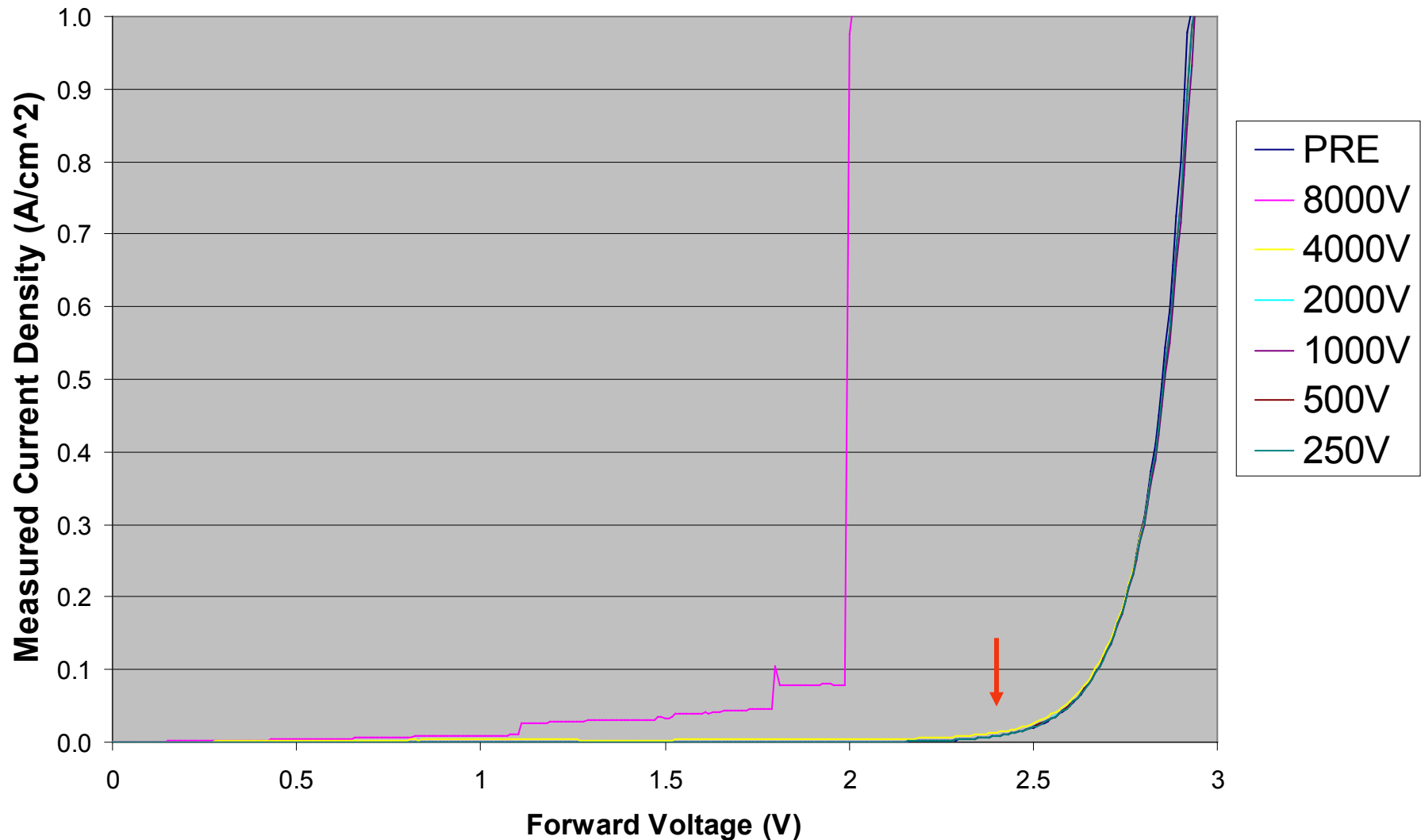
DIV Curves on a Linear Scale

HBM ESD Stress Test DIV Curves

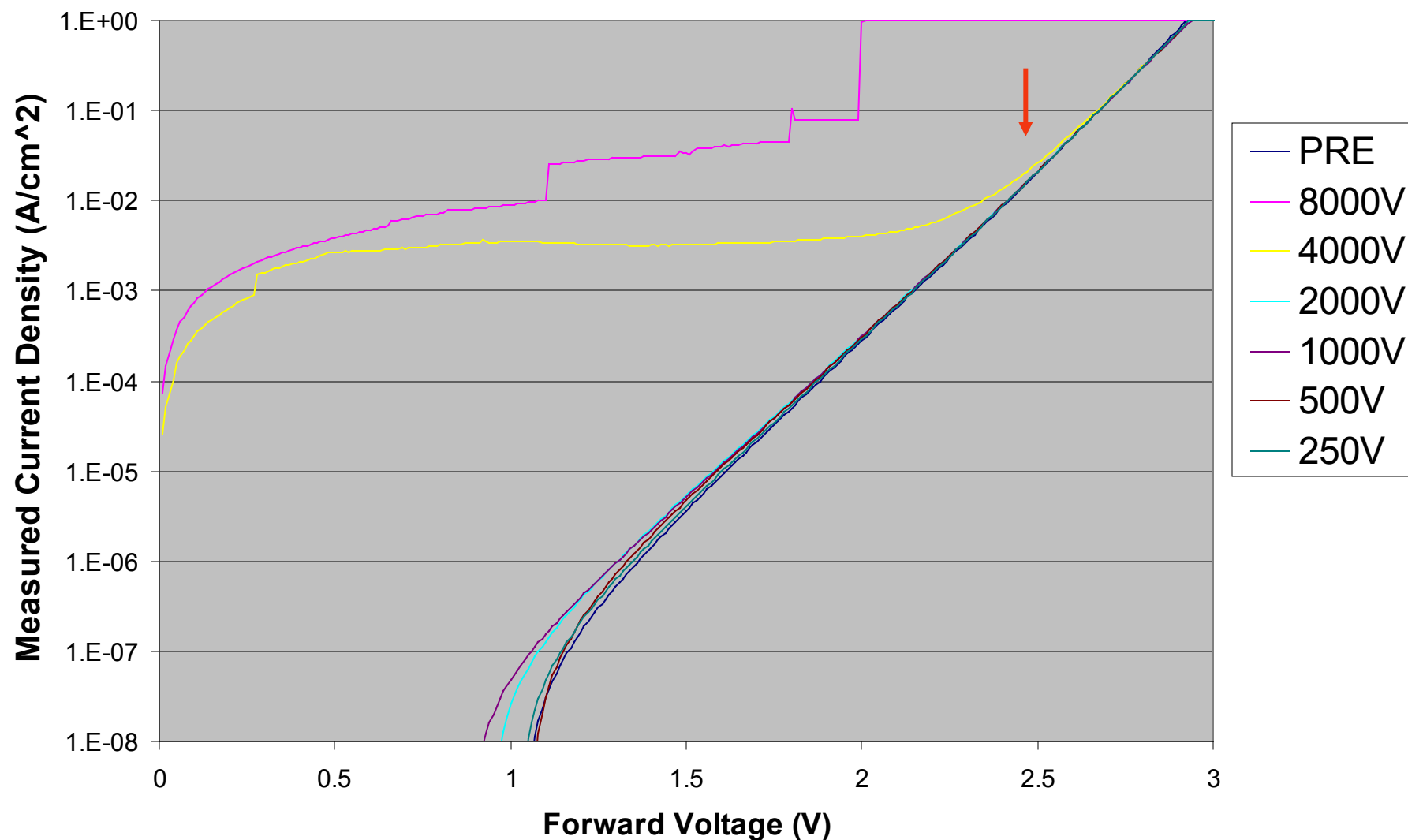


Typical In-process Pass/Fail Requirement

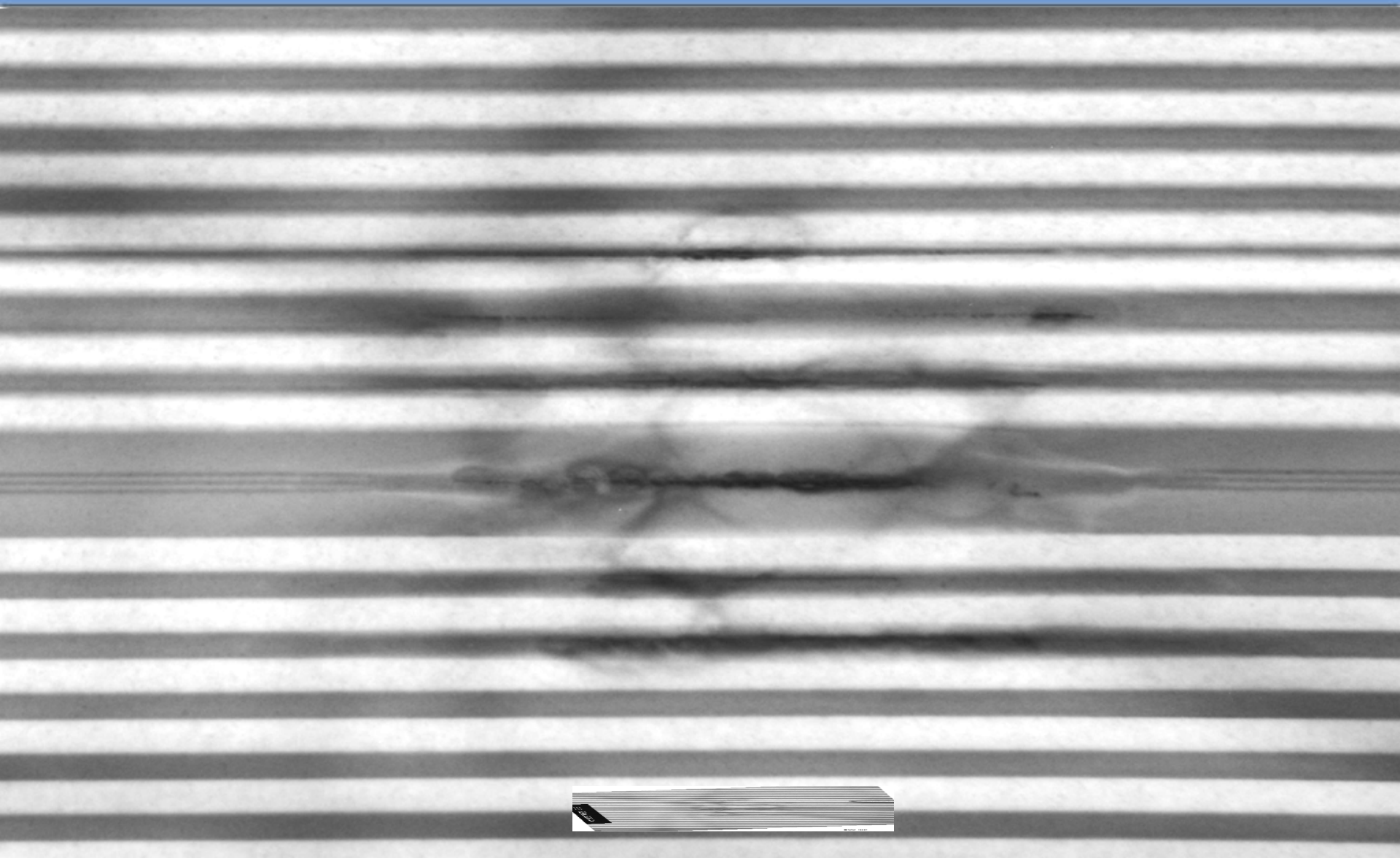
HBM ESD Stress Test DIV Curves



HBM ESD Stress Test DIV Curves

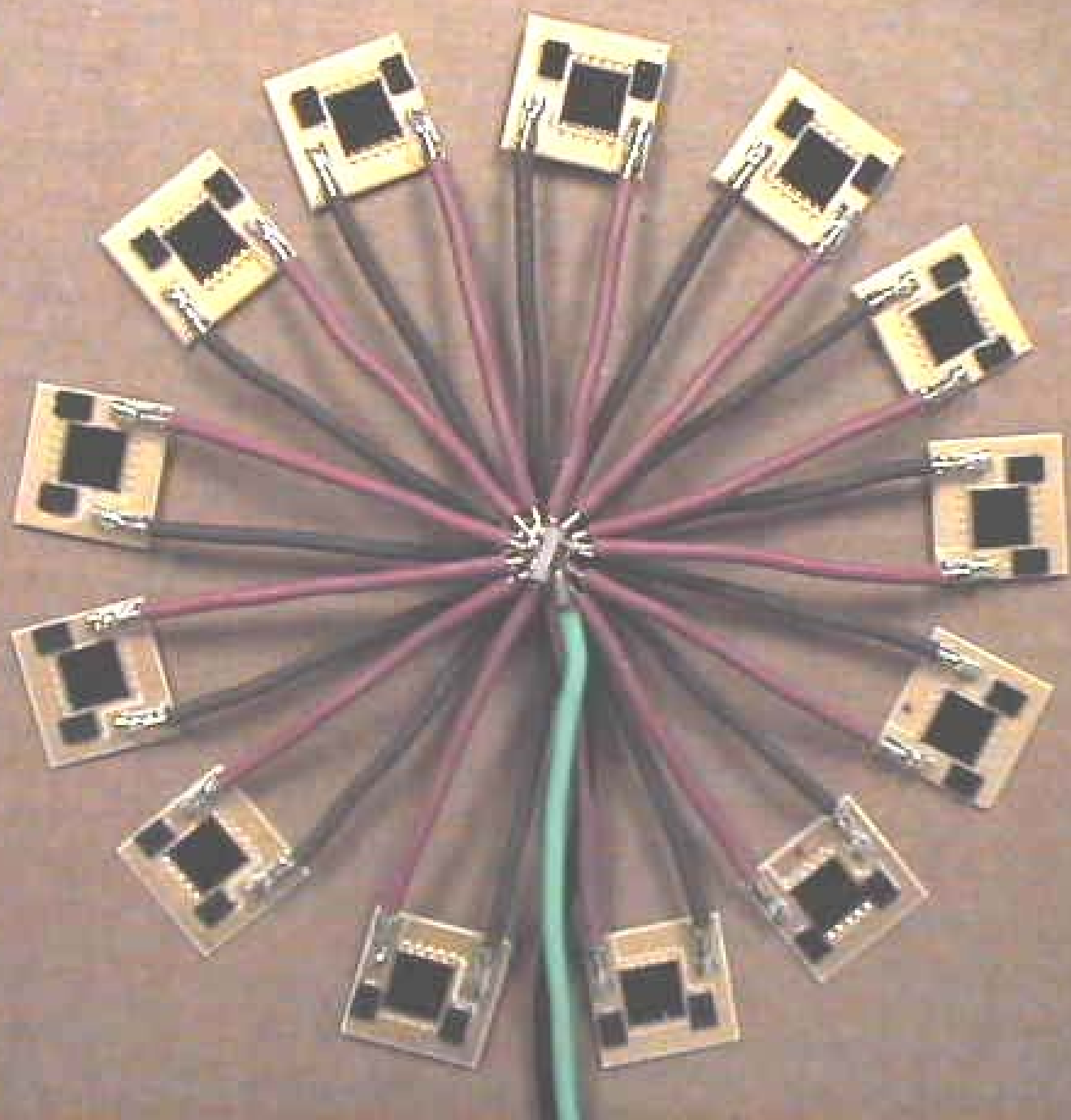


Cross Section TEM of ESD Damage (Laser Diode Structure)

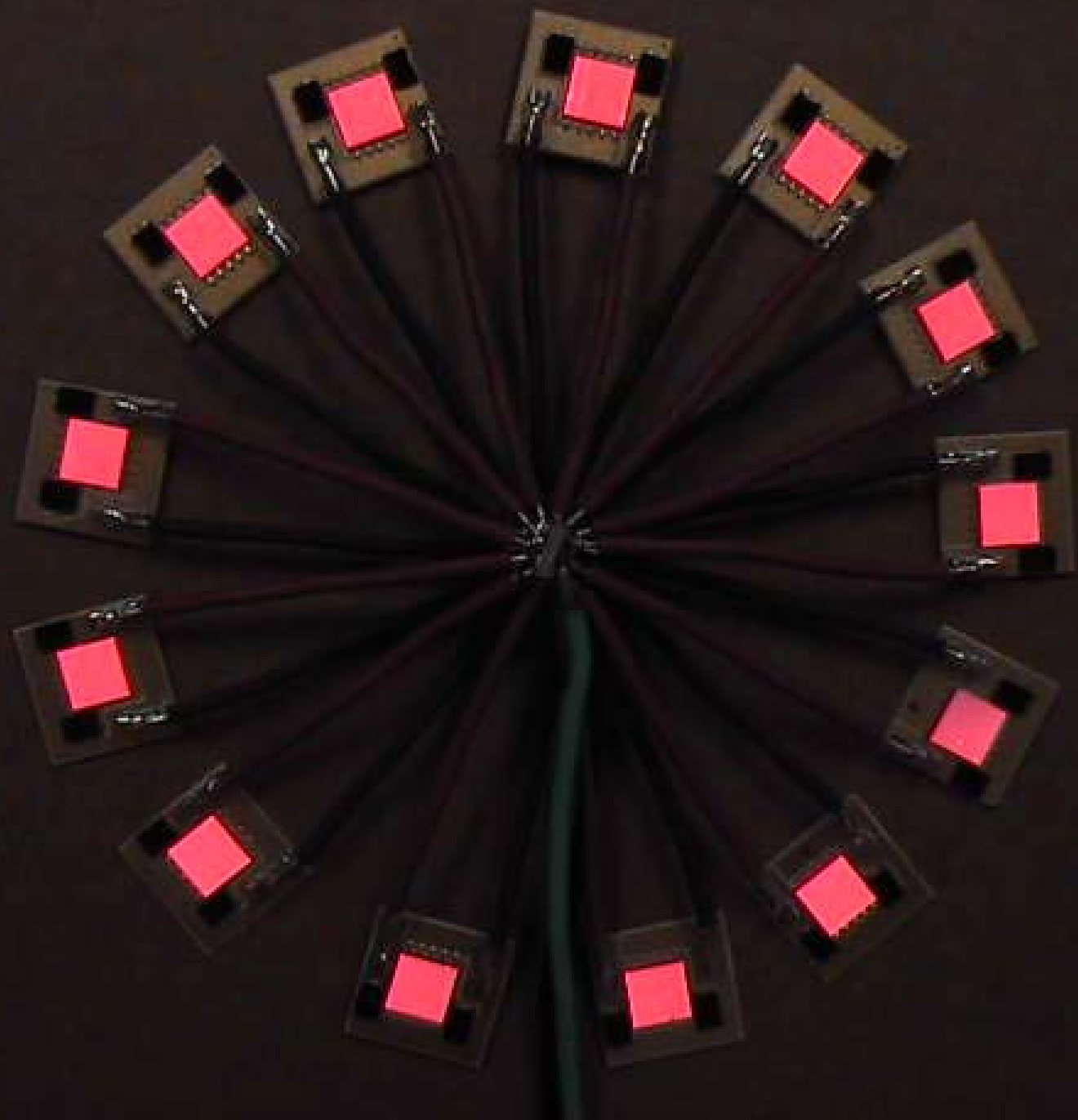


Thermal Runaway

- The following slide sequence shows a baker's dozen of Rxs wired in parallel.
- A fixed voltage at 3 A total regulated current is applied in the forward direction.
- Each device sees the same voltage, but draws a slightly different current due to natural variations in the forward IV characteristics of the cells.
- The assembly is then allowed to heat up.
- As this happens, eventually one of the devices will heat a bit more than the others.
- This, in turn, causes a shift towards lower voltage of the IV characteristic of the hotter device.
- Which leads to an increase in current flow through that device.
- Which leads to it getting even hotter due to joule heating.
- Which causes the IV curve to shift even further.
- Etc., etc.
- Eventually, a single device in the array will draw the lion's share of the current.
- If this is allowed to continue, that device will eventually overheat and fail.



























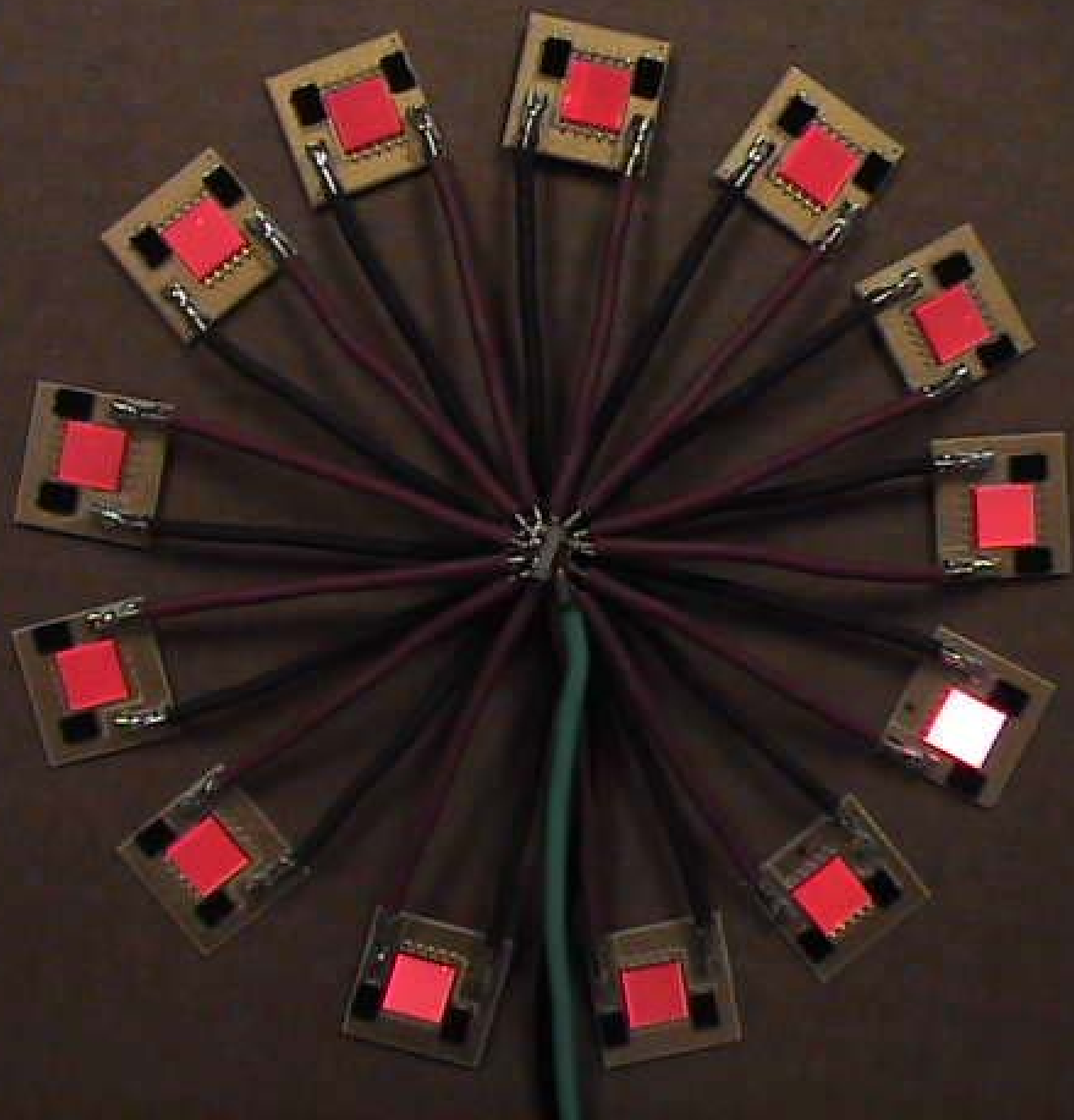


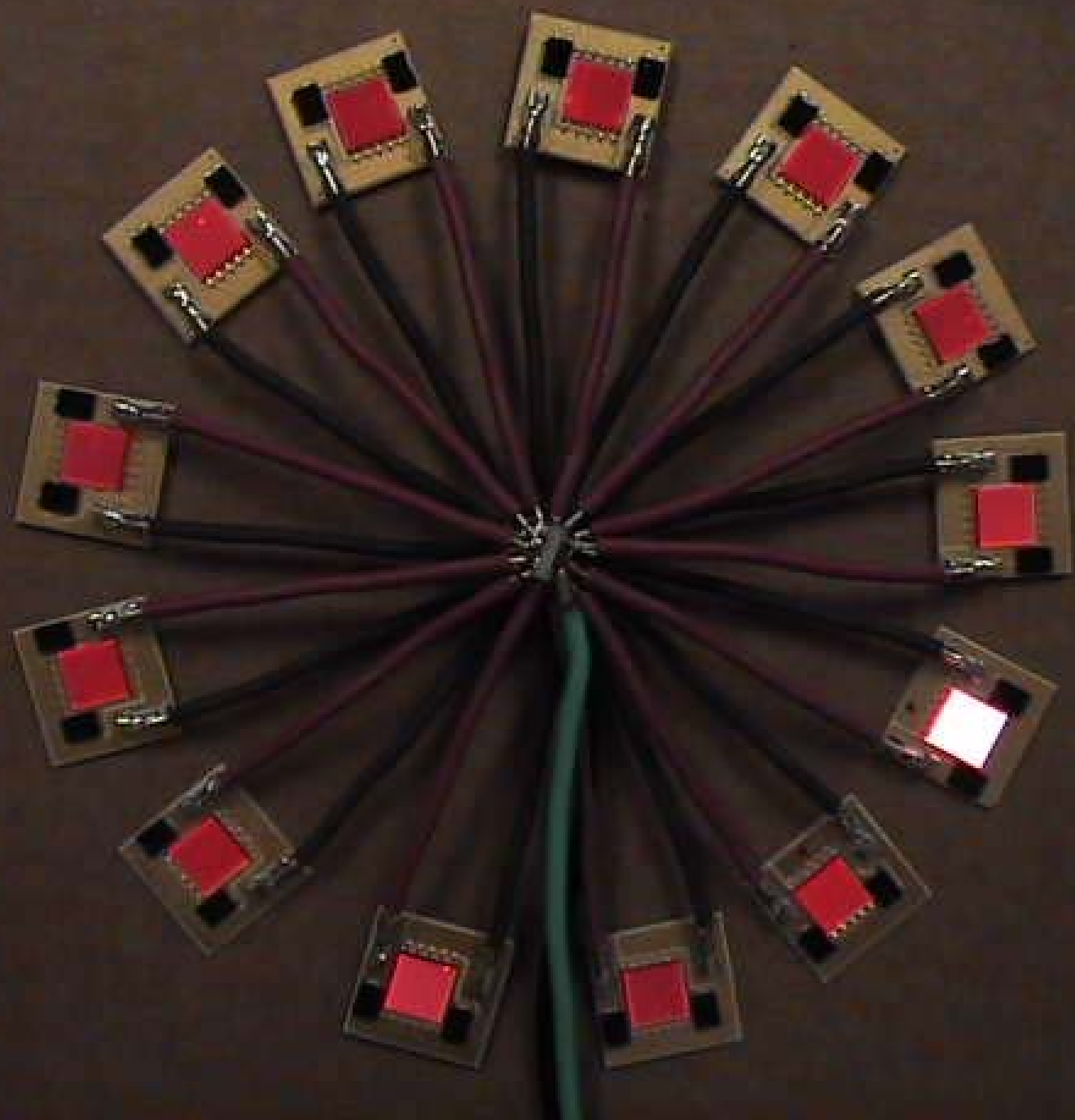


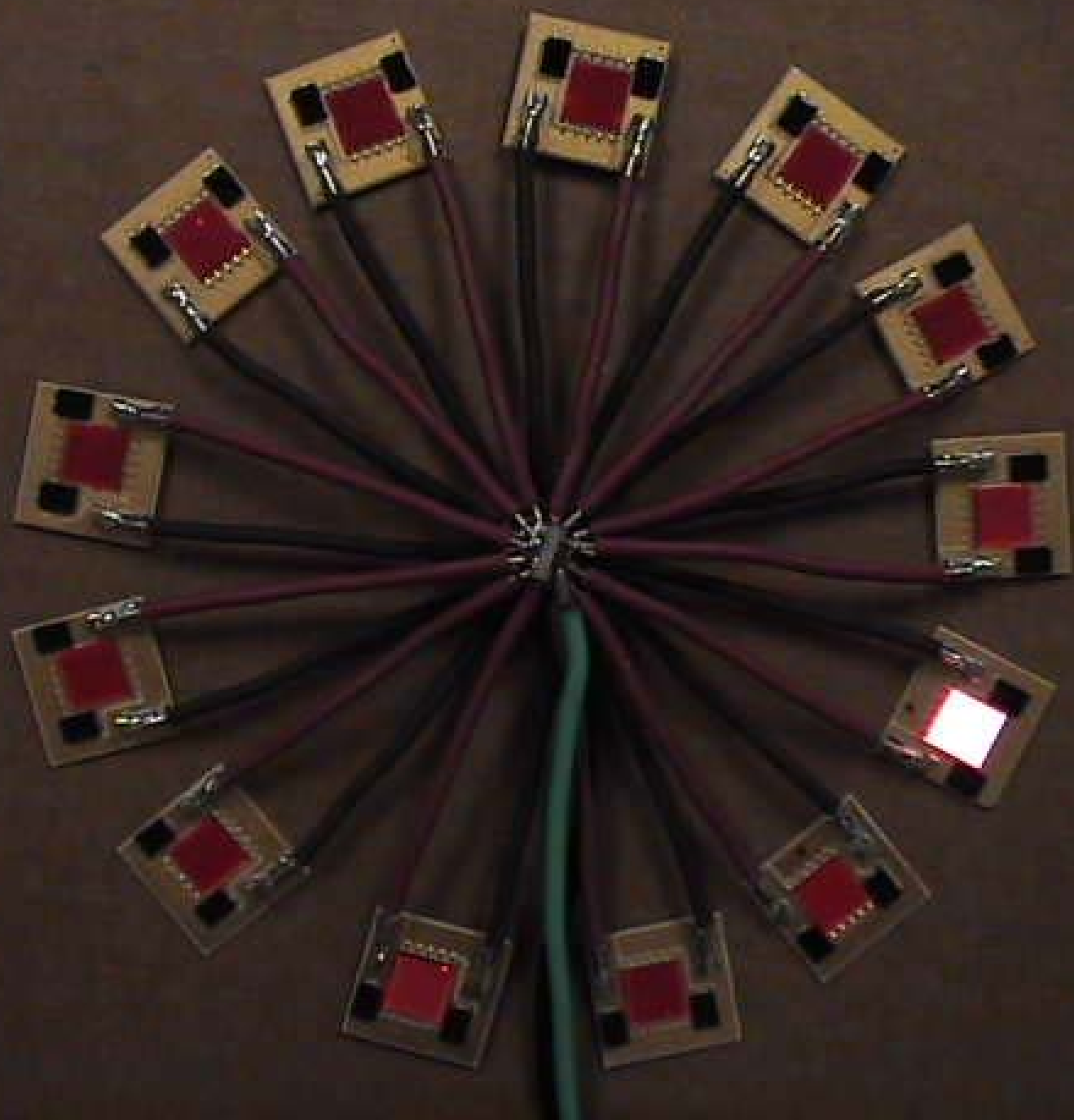




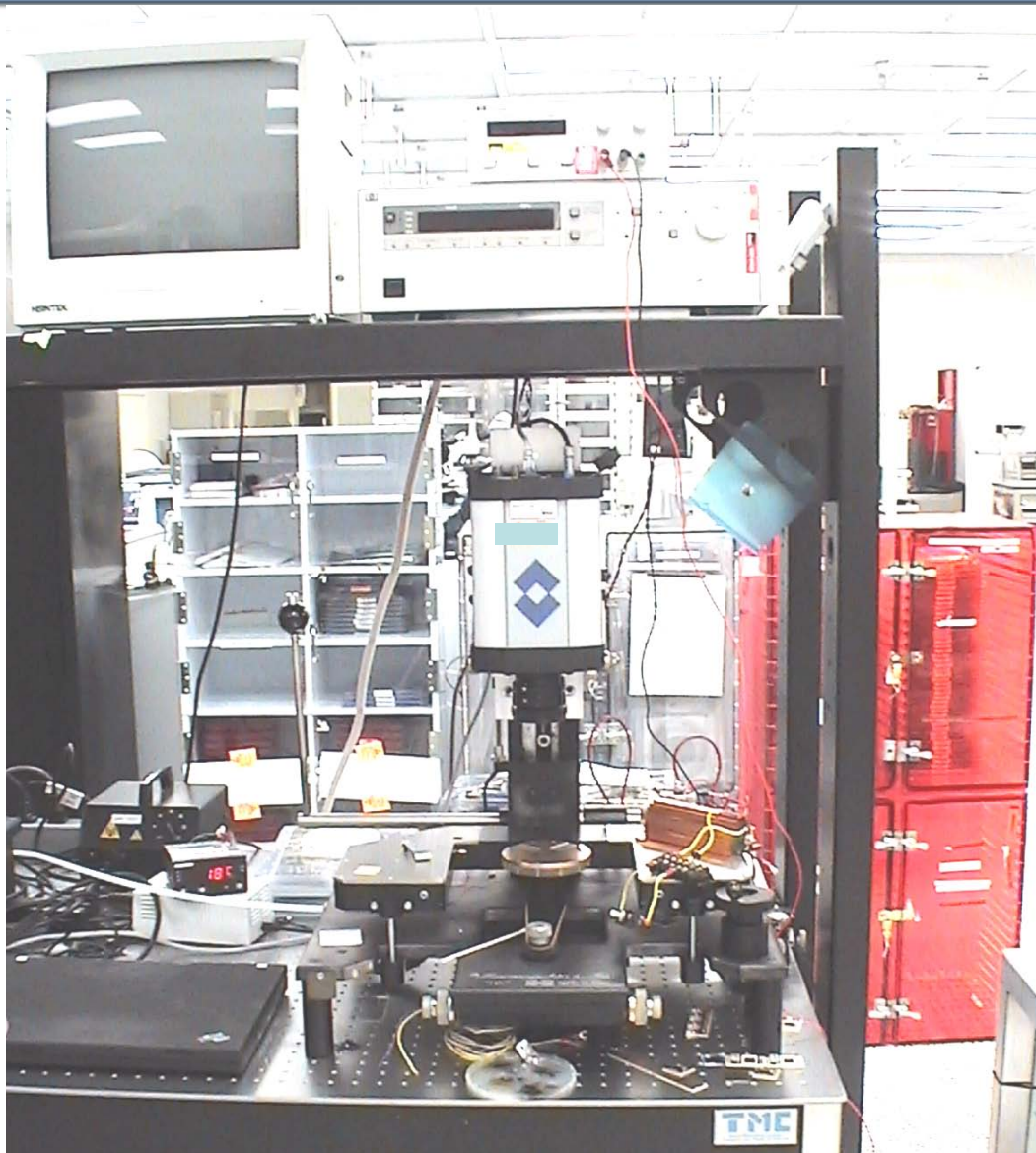








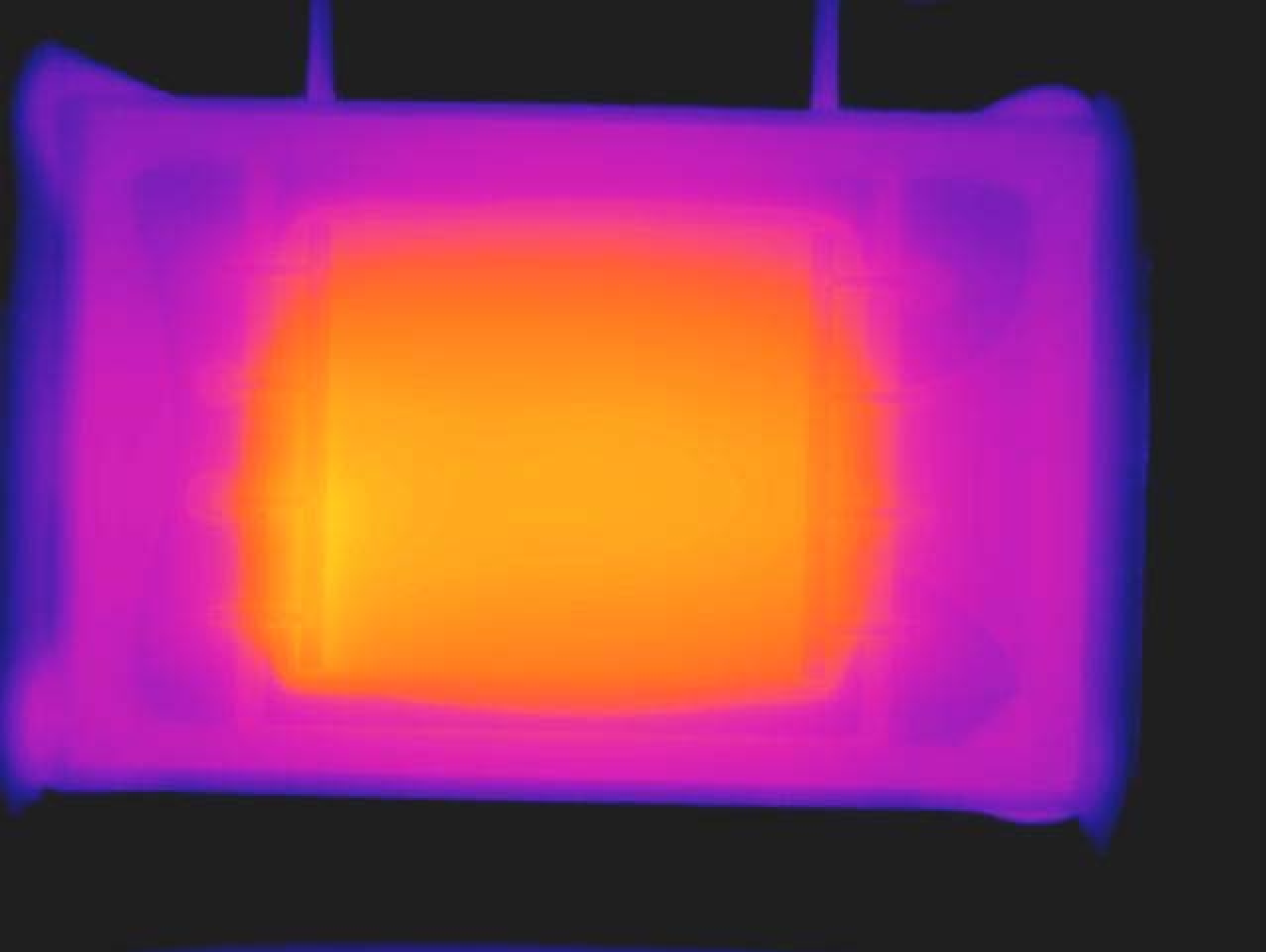
Thermal Imaging Setup

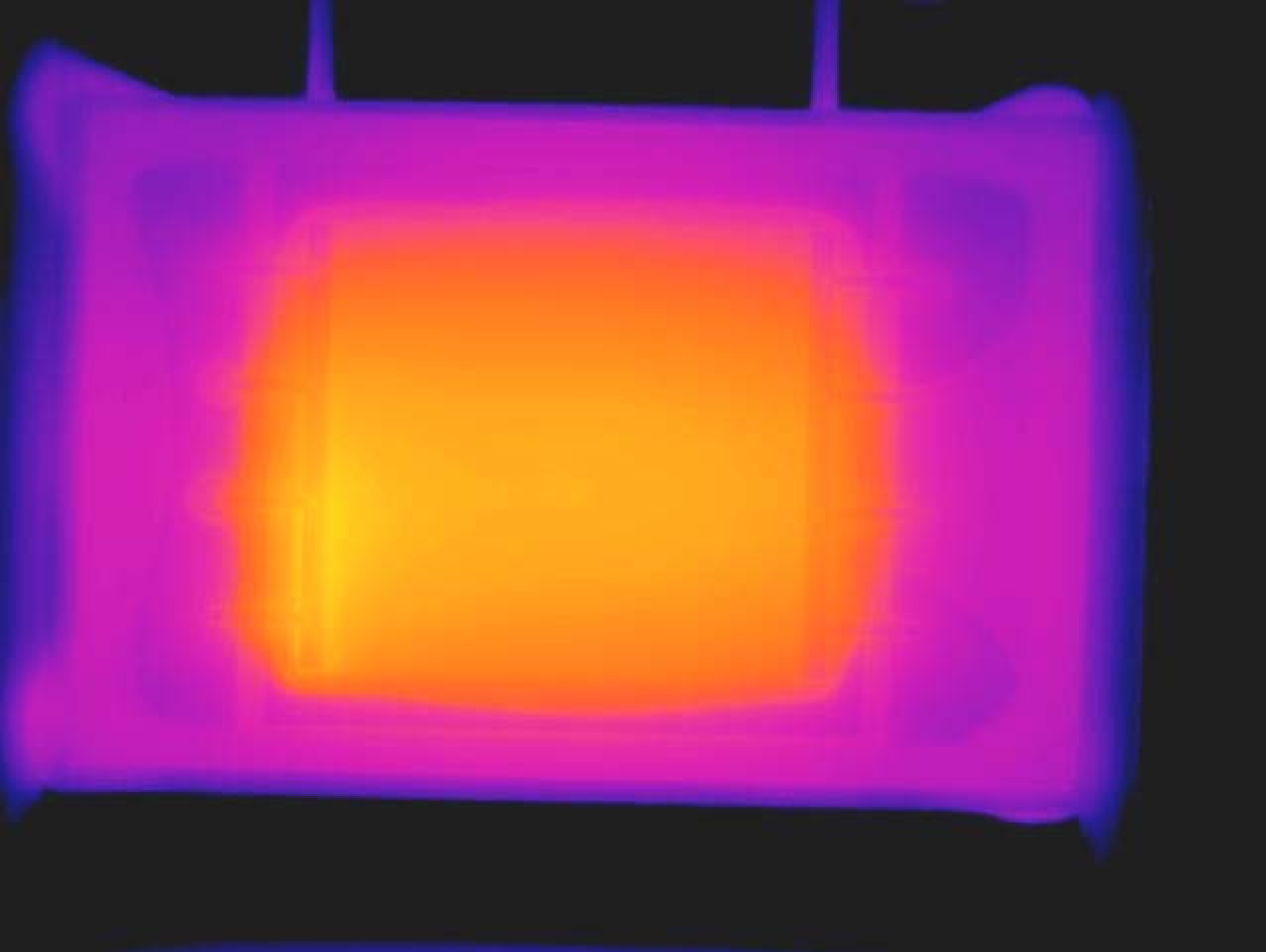


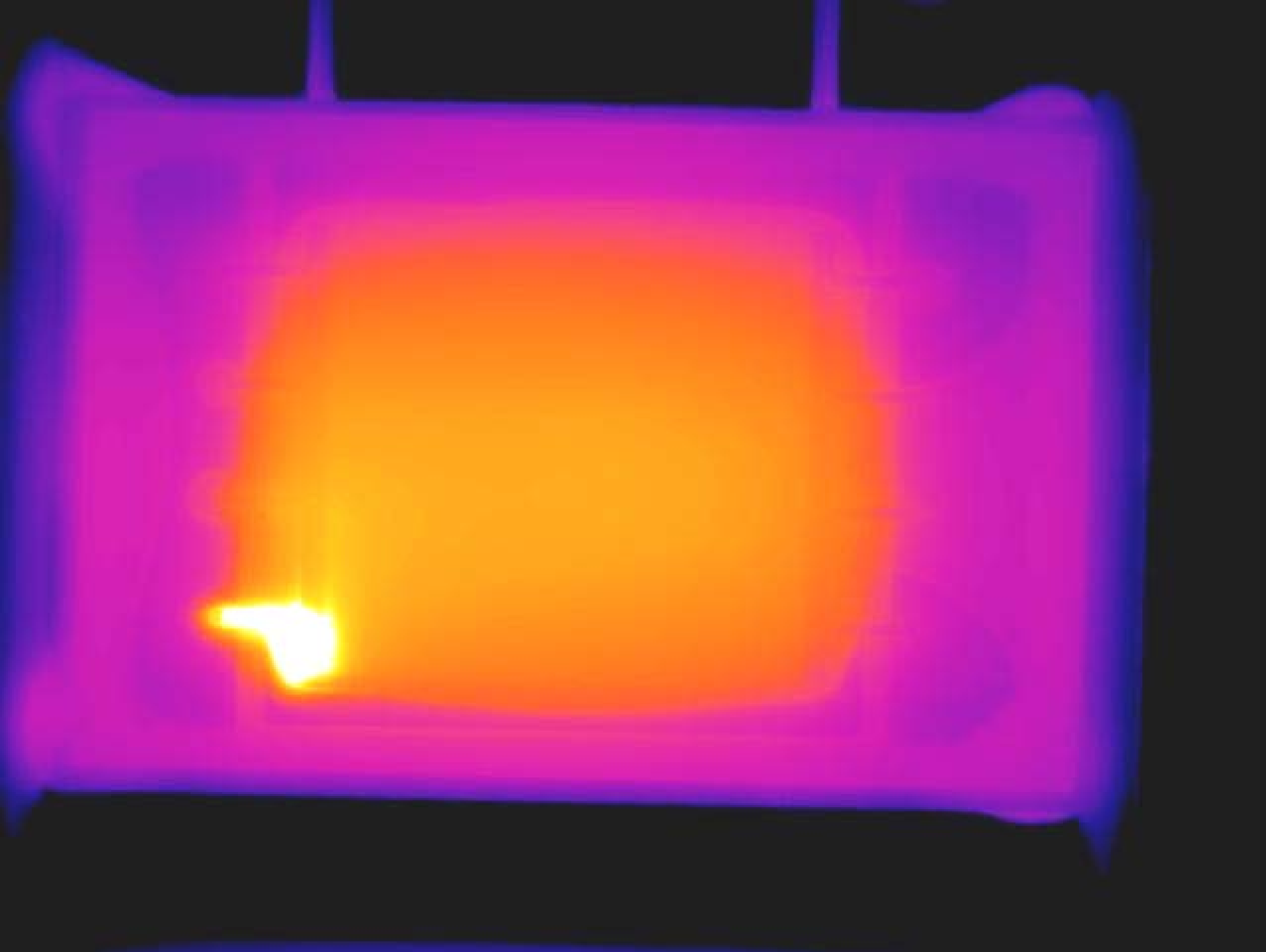
- The previous slide shows a pair of photographs of the FLIR Thermography set up used to capture the images in the following sequence.
- What you will see are thermal images of a single receiver that is stressed with progressively higher levels of forward current.
- The sequence runs from low bias to destruction of the cell by thermal runaway.
- The thermal scale runs from black = room temperature to white = hot, hot, hot (>350°C where the camera saturates).

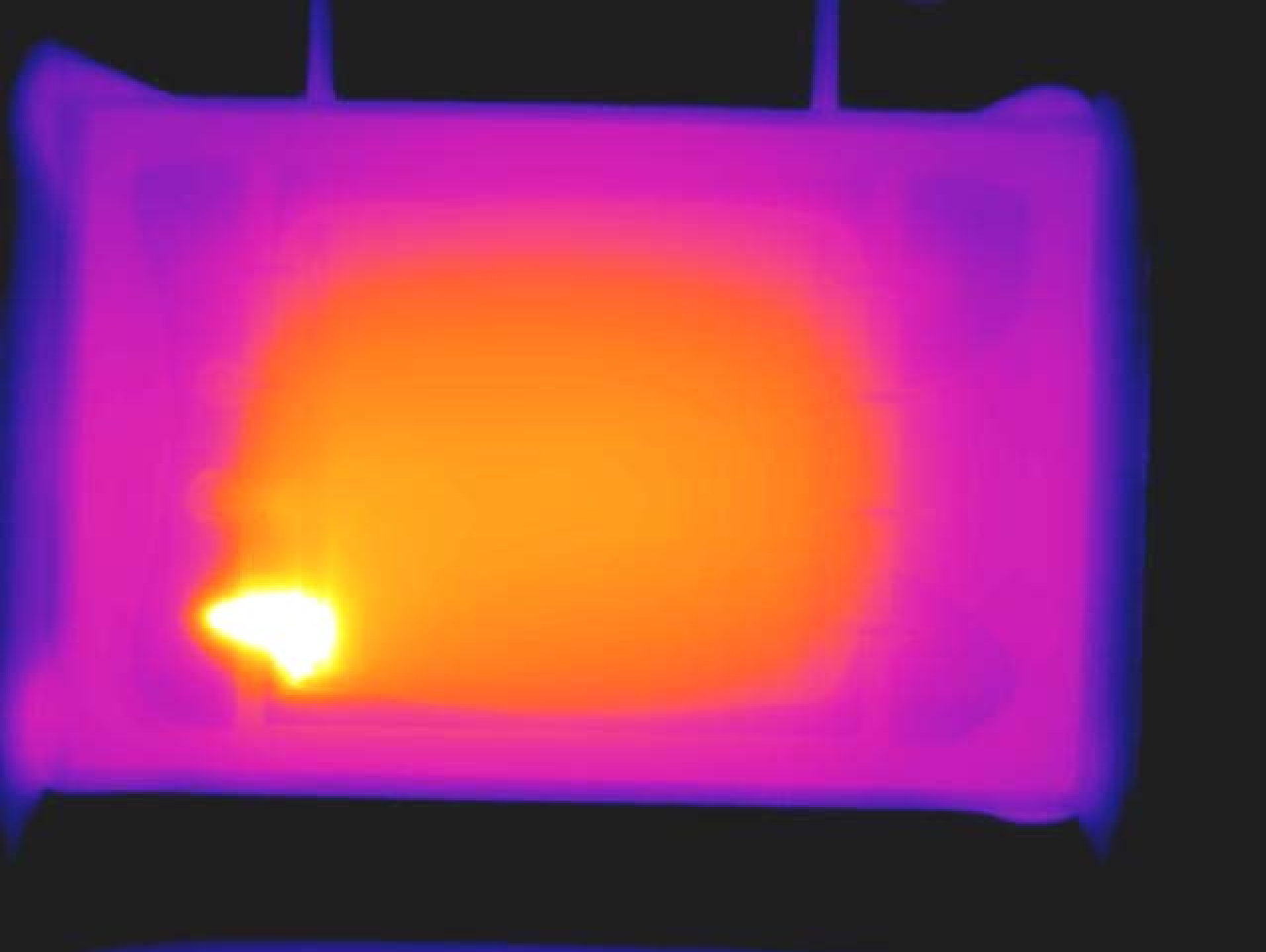


- These images were not corrected for emissivity variation between the various surface materials in the receiver.

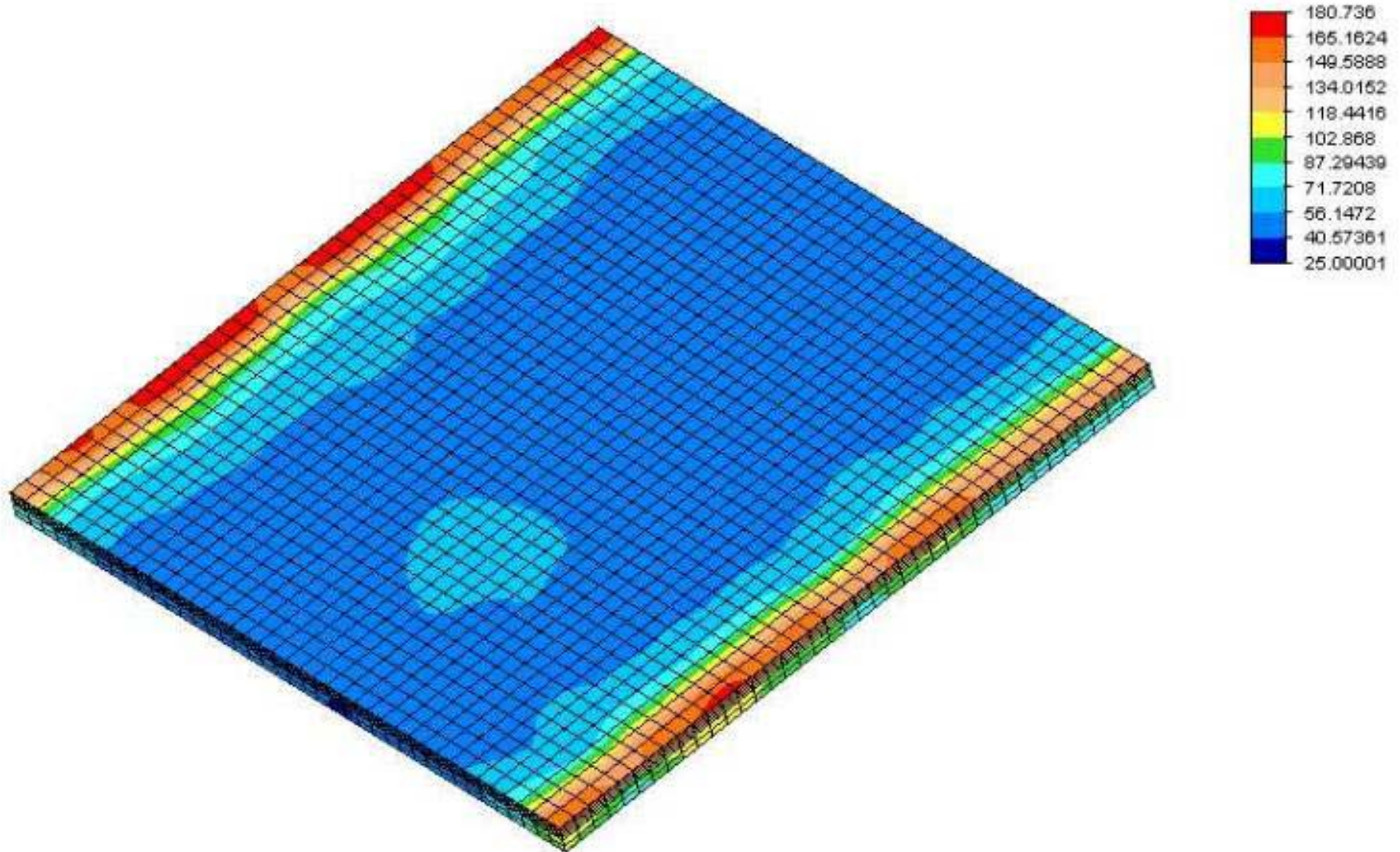






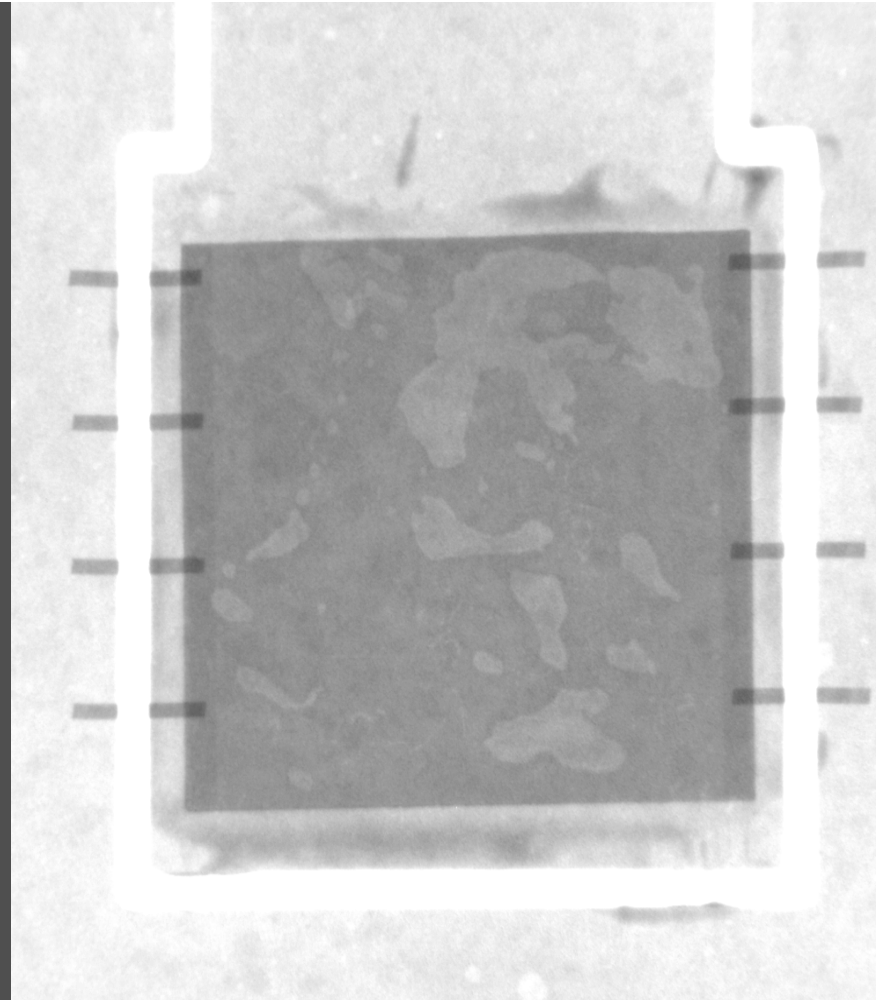
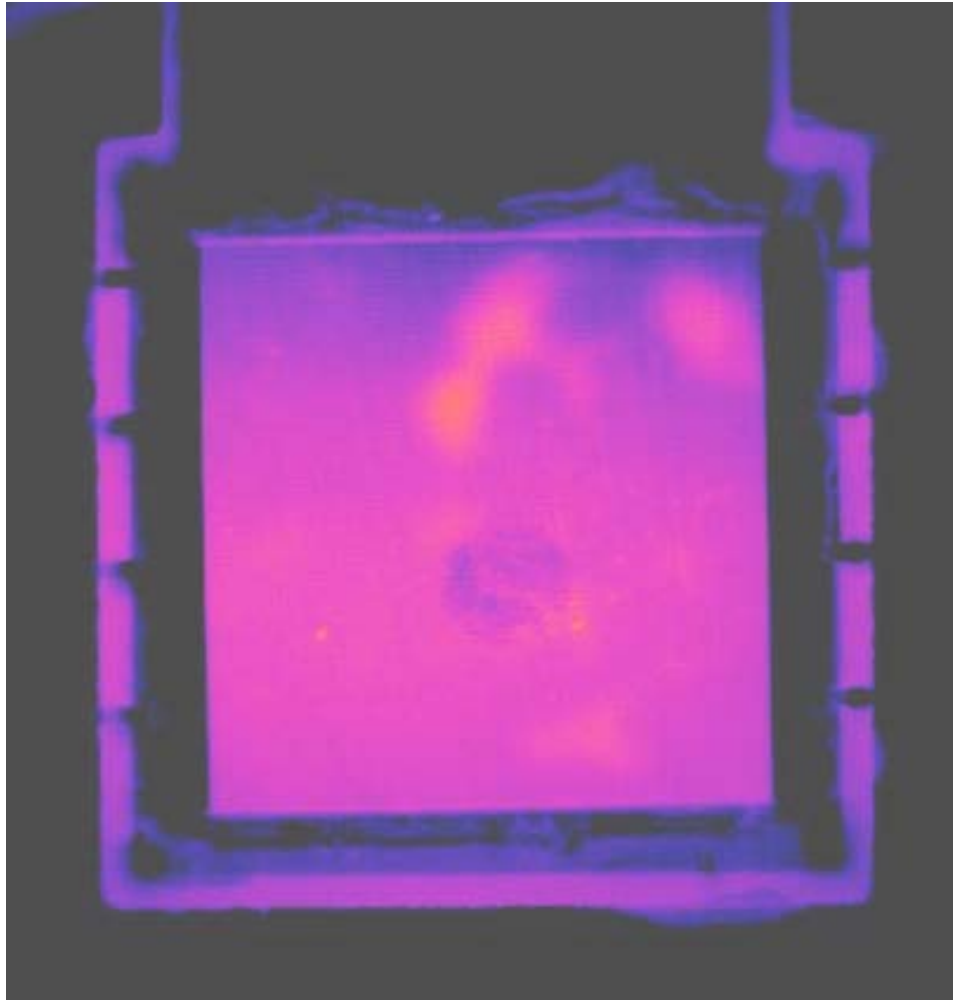


FEA Model (Current and Heat are Synonymous)

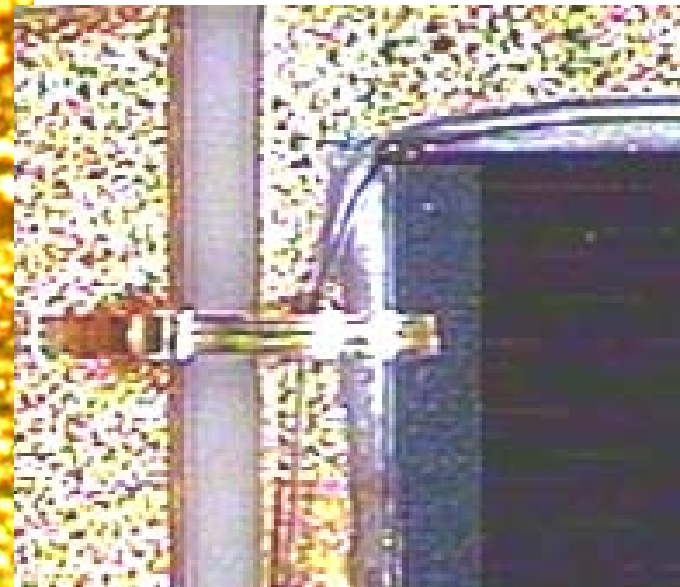
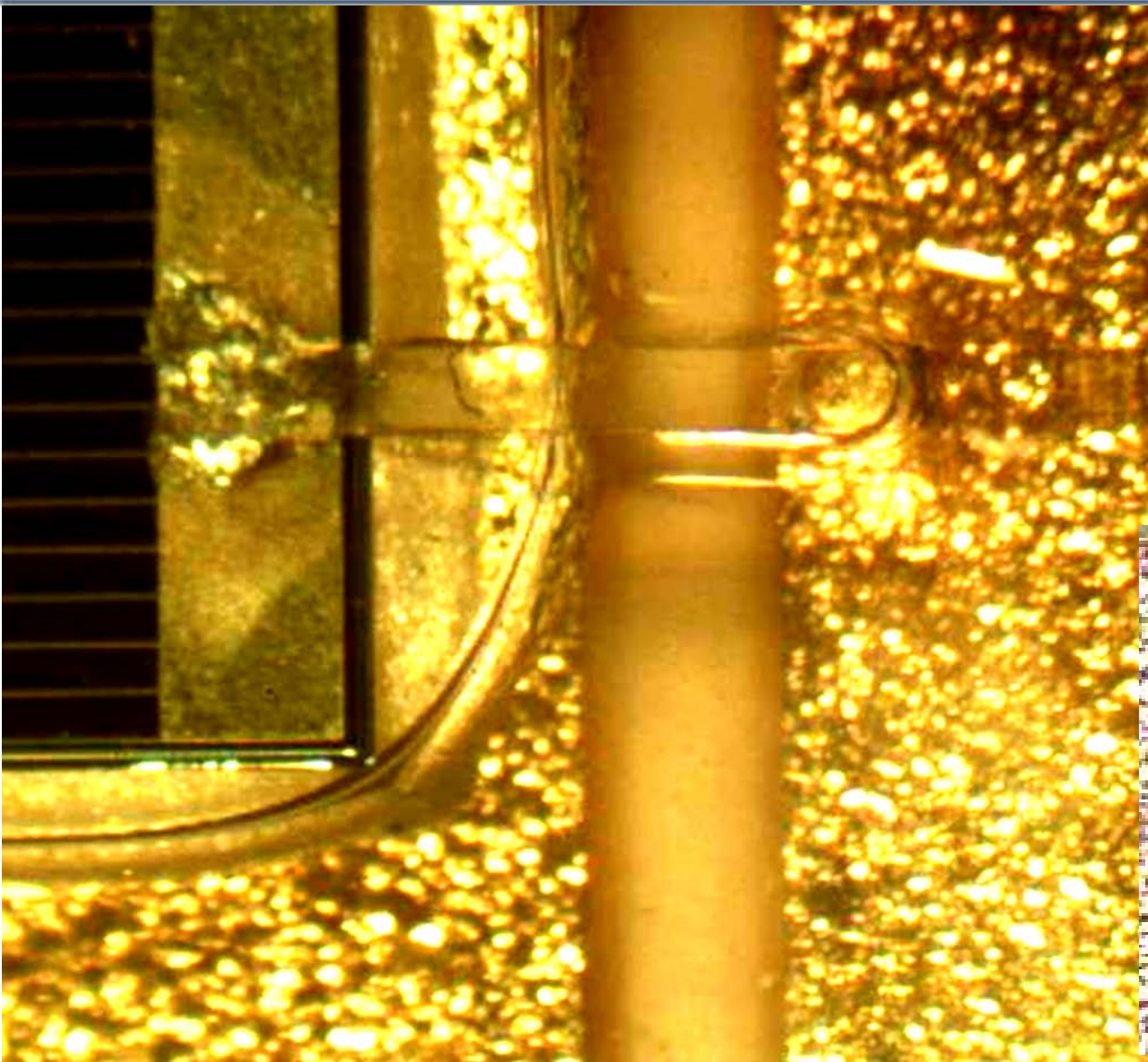


- **Thermal Impedance Variations**
 - Voids and other non-uniformities in the die attach
 - One corner of a rectangular cell is always higher than the other three
- **Current crowding in forward bias**
 - Under buss-bars
 - Near ribbon bonds
- **Localized shunt current paths**
 - Intrinsic crystalline defects
 - Edge shunts
 - EOS/ESD

Die Attach Voids



Fused Ribbon Bonds



Highly Energetic Events



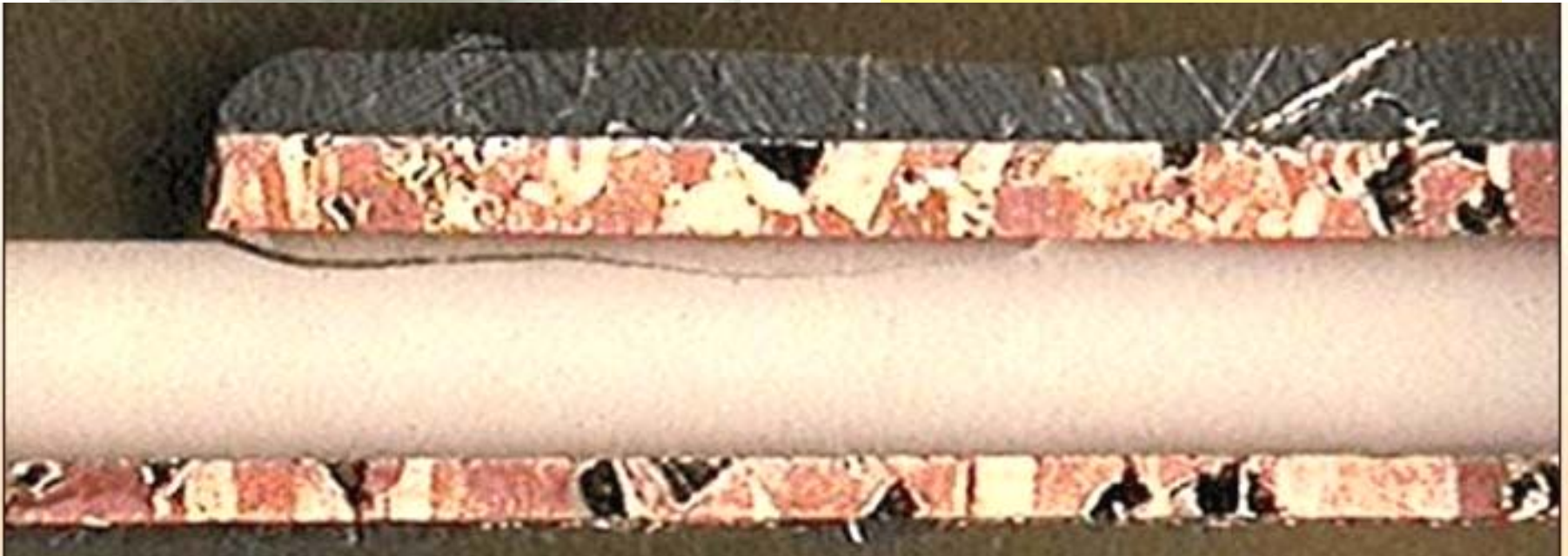
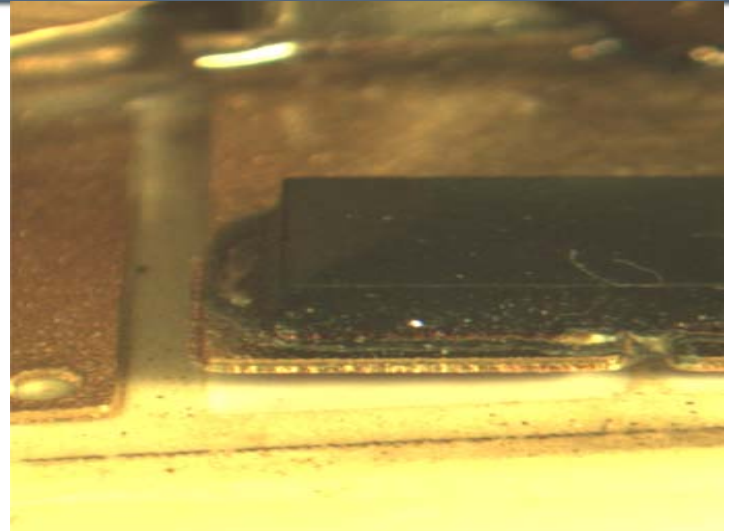
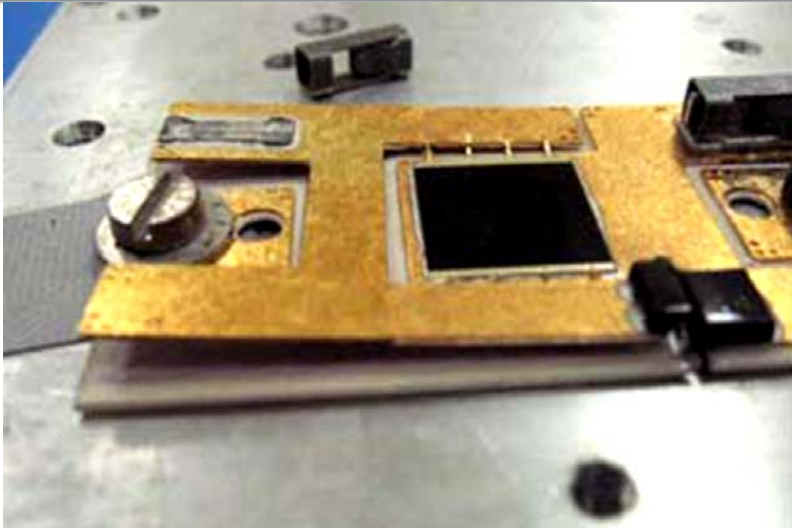
Power Thermal Cycling

- IEC 62108 section 10.6 calls for a periodic forward bias current of $1.25 \times I_{sc}$ through the cell (to simulate the optical thermal load in the application) while the device under test is cycled between -40 to 110°C CELL temperature.
- If one misses the fine points of this test and simply applies the current bias without monitoring (and controlling on) cell temperature some unexpected results may obtain.
 - Thermal Runaway.
 - Very high cell temperatures.
 - Unrealistic temperature gradients.
 - Receiver substrate failures.

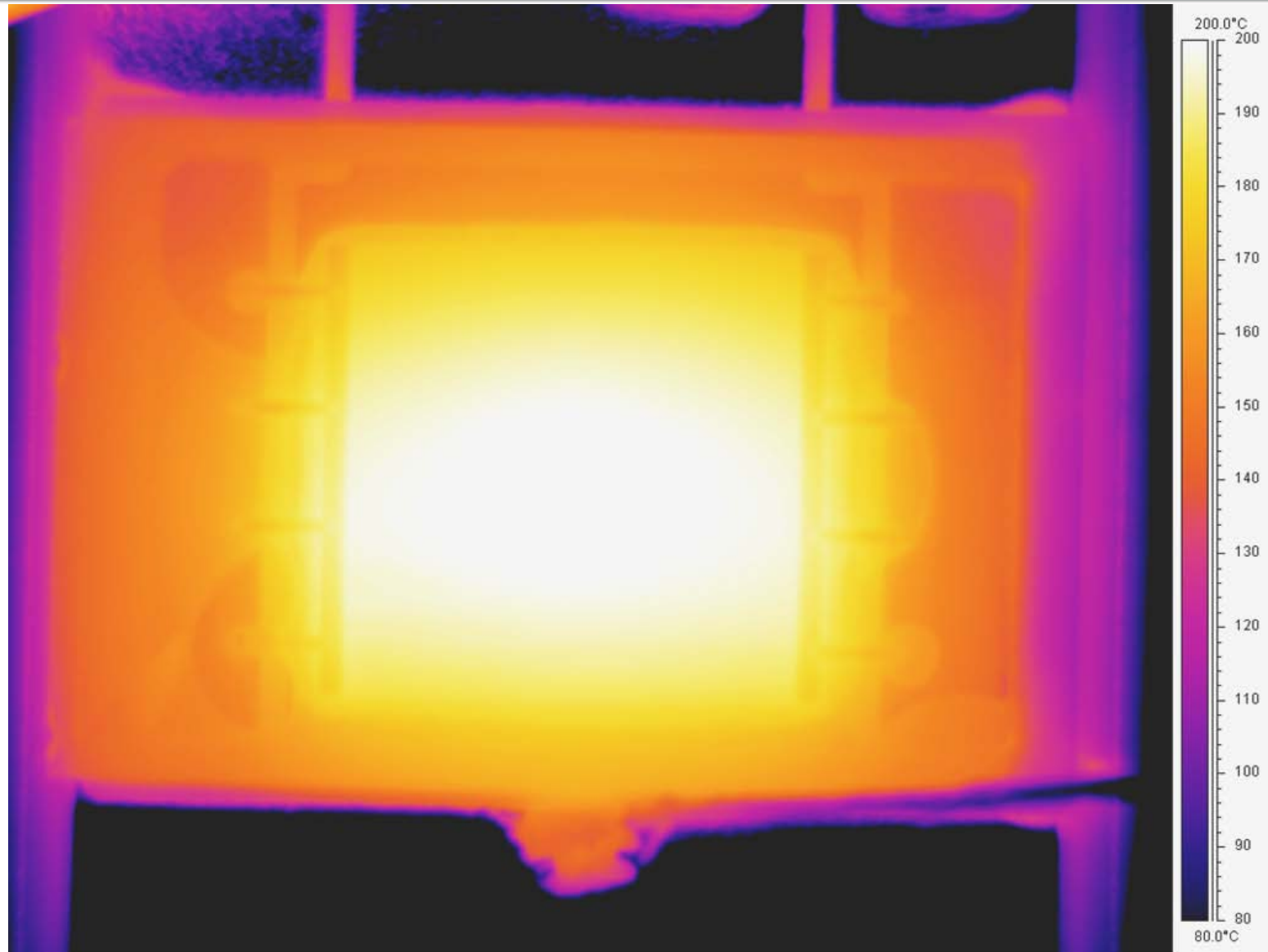
Powered Thermal Cycling



Ceramic Conchoidal Failures in PTC

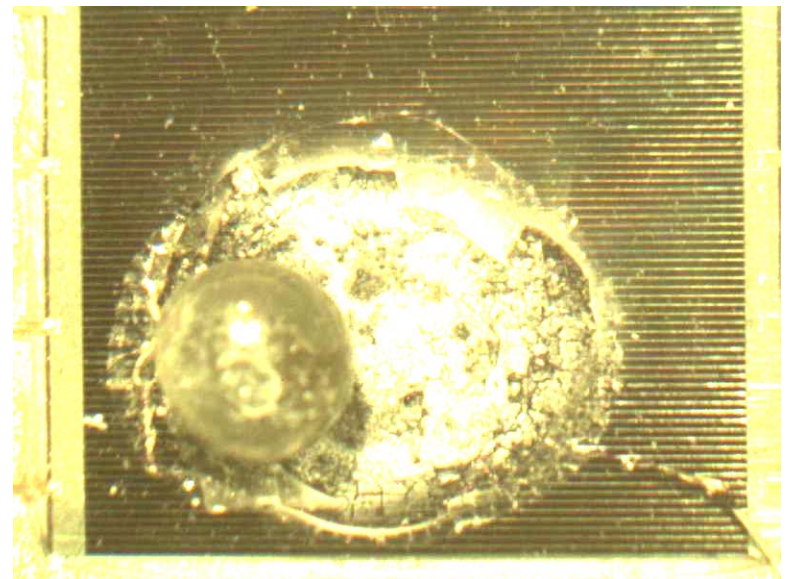
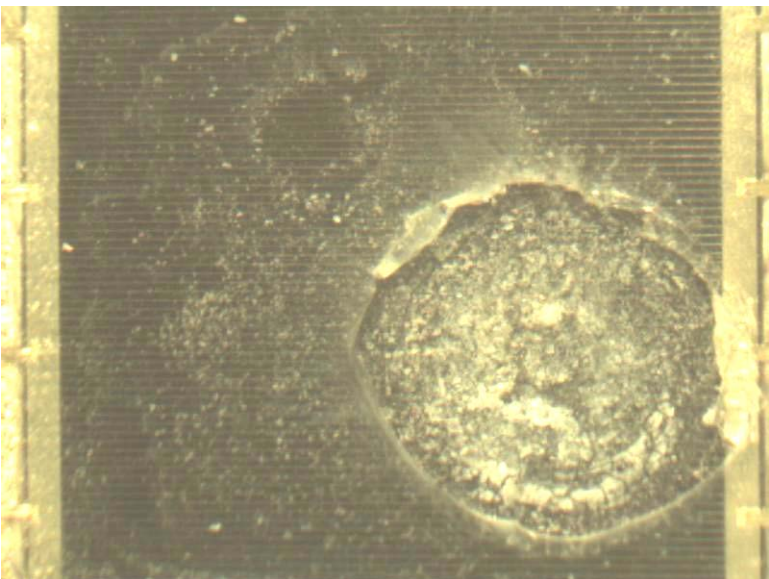
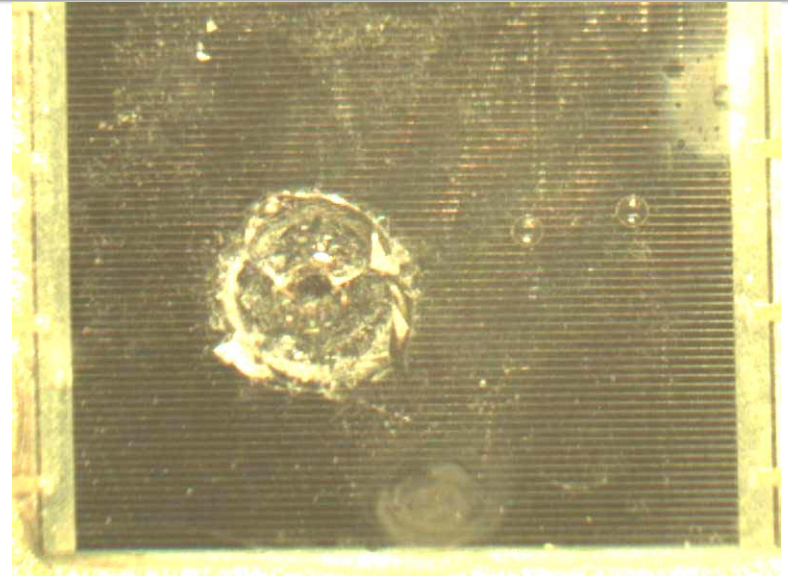
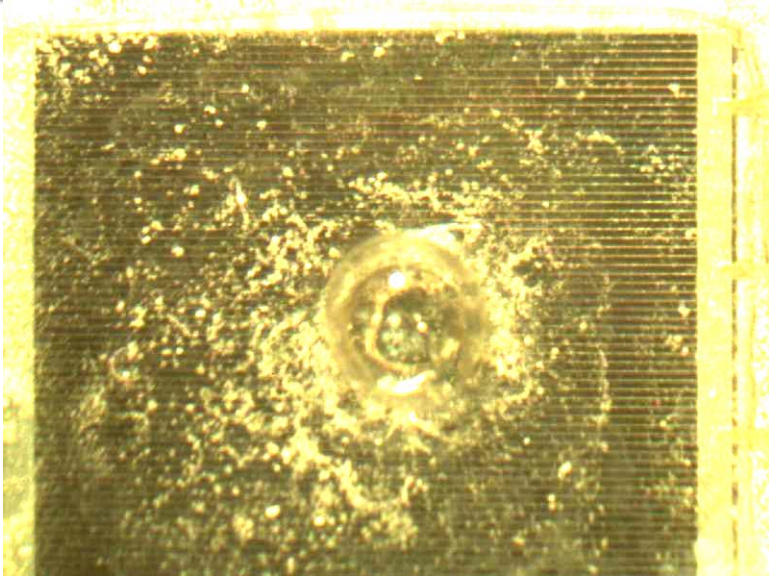


At $1.25 \times I_{SC}$ the temperature of this cell is at least 120°C above ambient (heat sink).

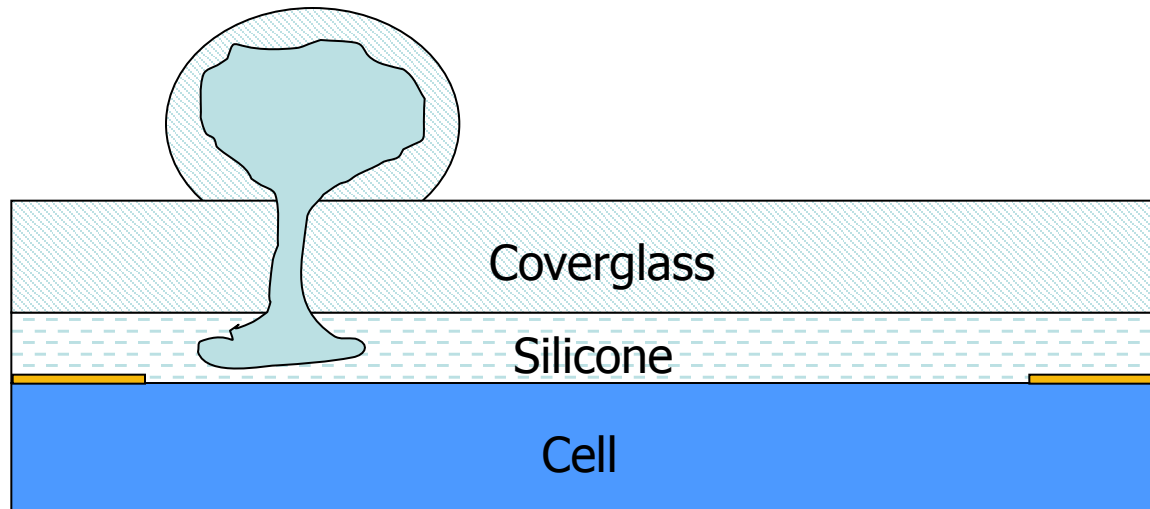


Coverglass Melting

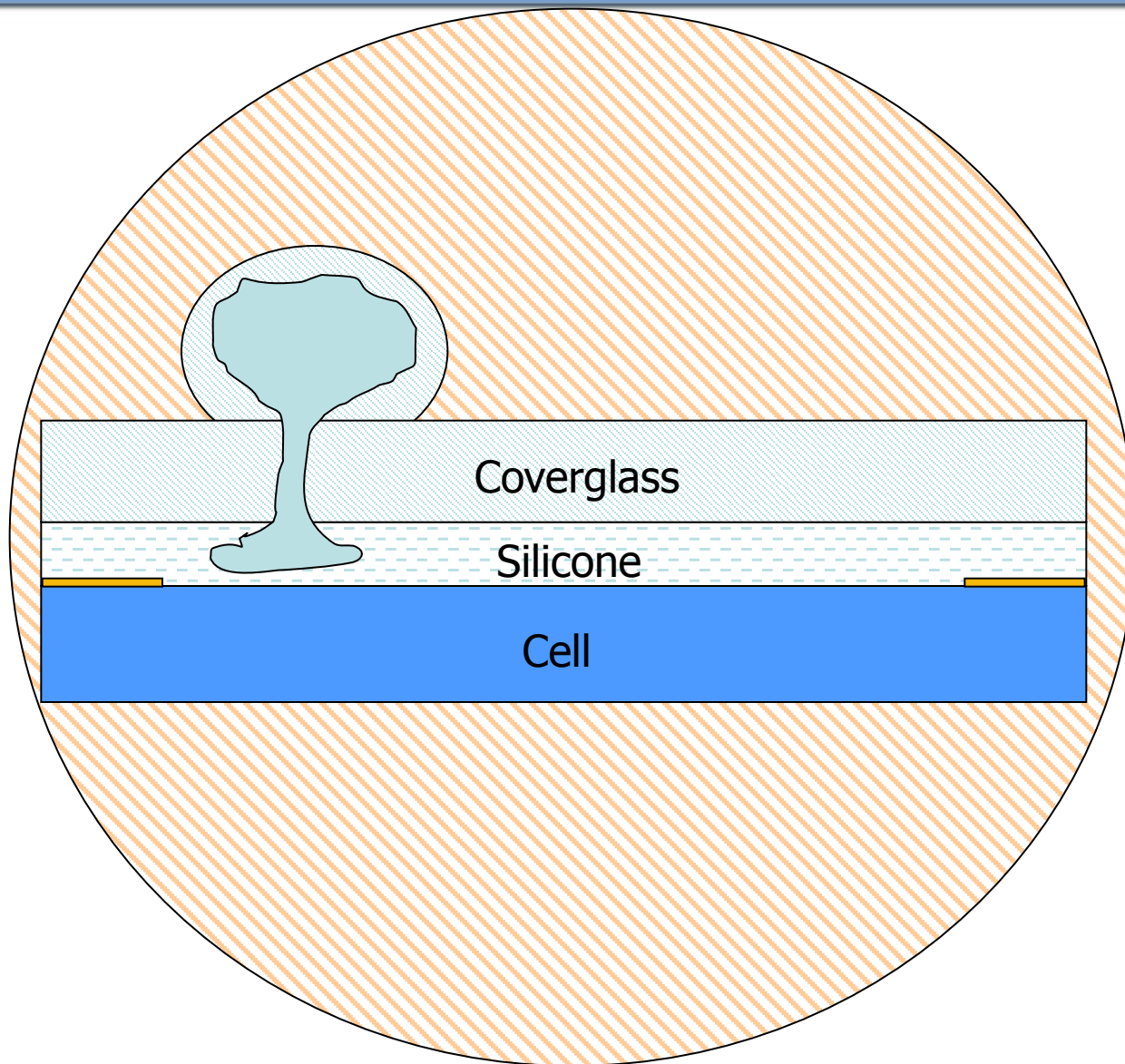
Coverglass Failures



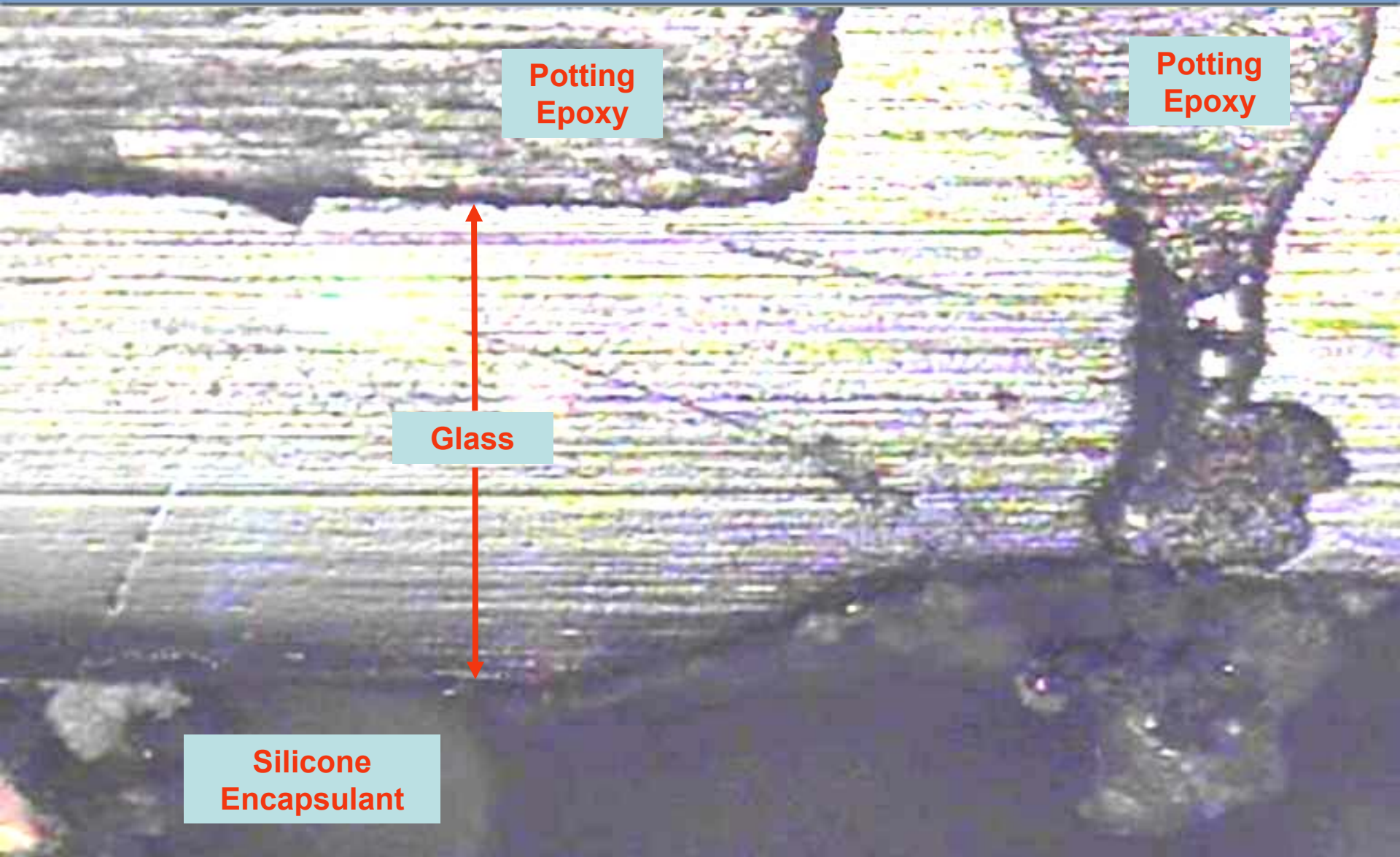
Cartoon Cross Section of Melted Coverglass



Cartoon Cross Section of Melted Coverglass

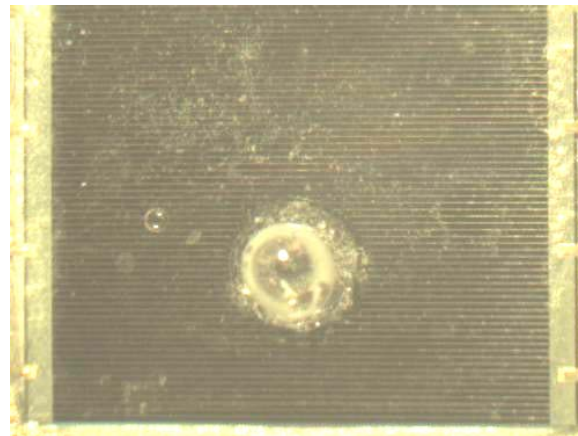
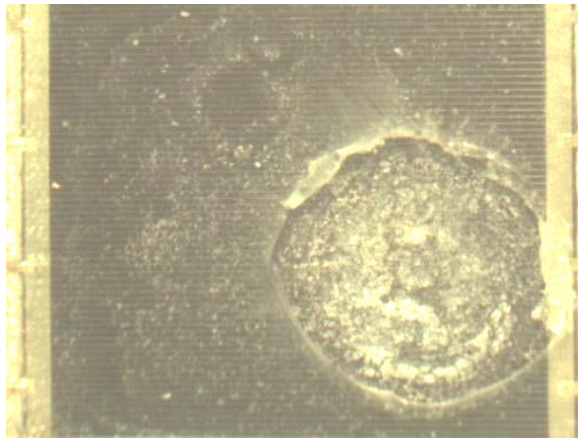


Mechanically Polished Cross-section

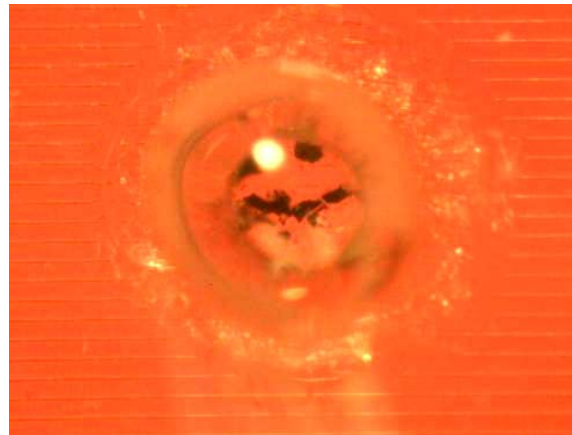
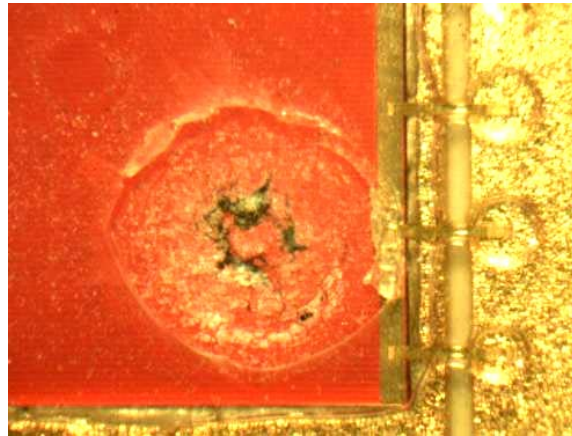


Closer Examination of Failures

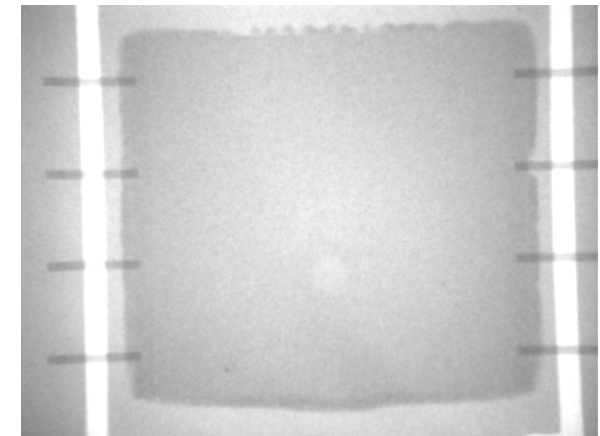
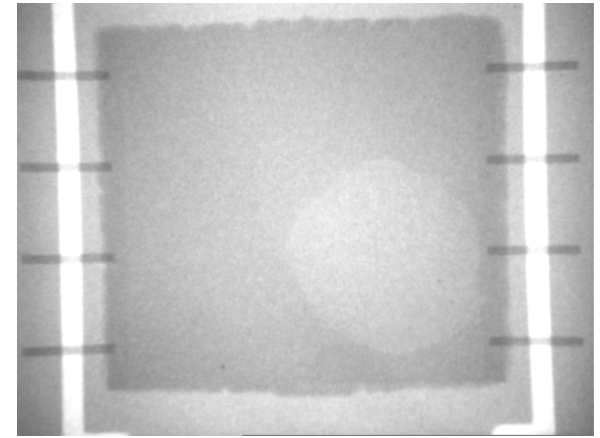
Visual



TC EL



Xray



No apparent damage to cell

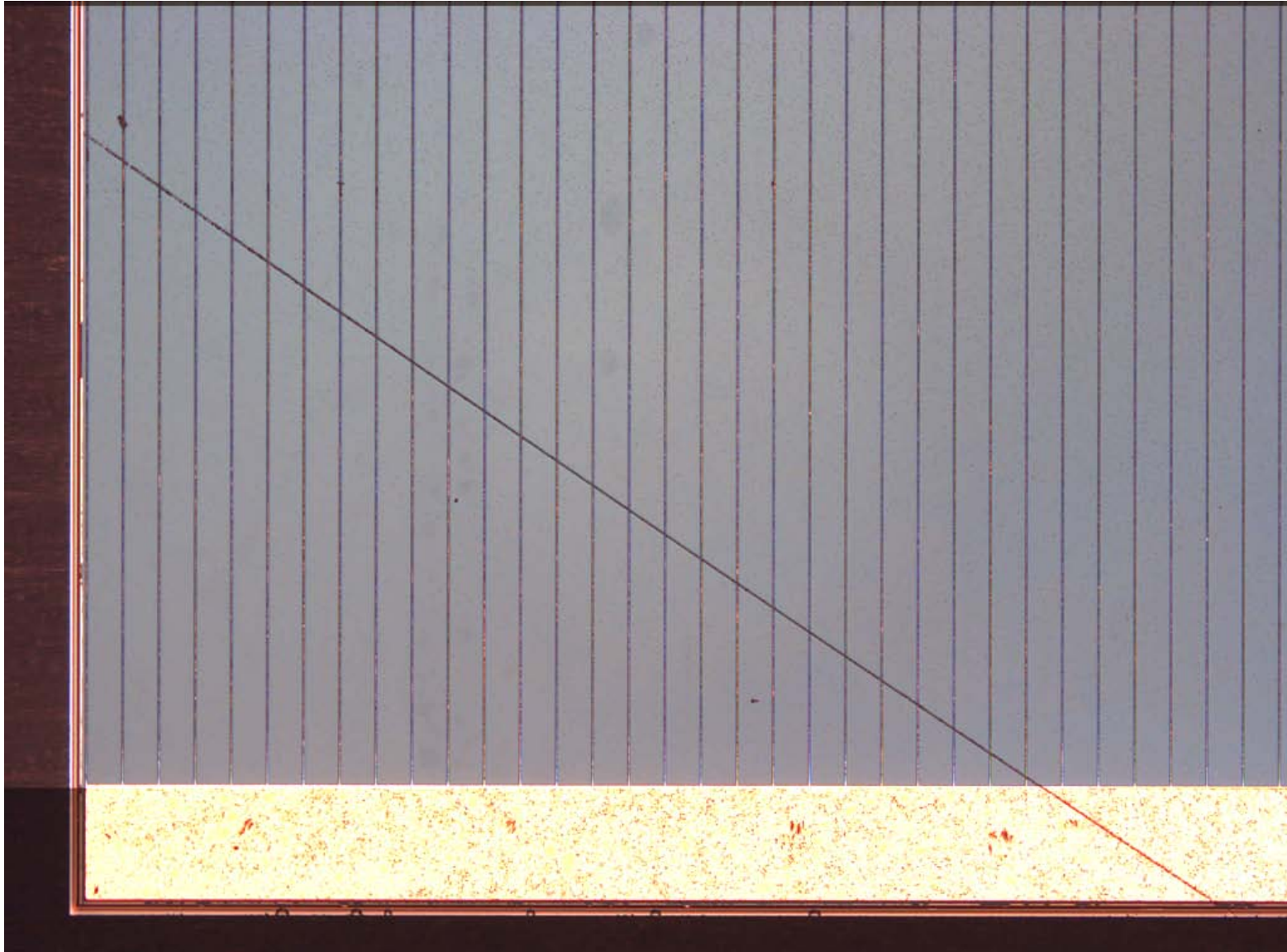
Xray contrast due to glass

- **Silicone beneath coverglass too thick**
 - Thinner silicone (1 – 2 mils) under coverglass has not exhibited the failure mode.
 - Silicone is not a good thermal conductor, but why is it absorbing?
- **Particulates trapped in silicone during fabrication**
 - Tools shedding metal particles.
 - Dust or lint particles.
- **Coverglass quality**
 - Inclusions.
 - Incorrect glass formulation.
- **Various “Greenhouse” effects**
 - Coverglass reflects IR emitted by cell.
 - Structure concentrates and preferentially absorbs energy re-radiated at the middle cell band-edge wavelength.
- **Misalignment of lens relative to cell**
 - Higher concentration (2000X?) if light pushed into corner of SOE.
 - Doesn't explain failures near center of cell, or provide root cause.
- **Thermal impedance**
 - Better heat sinking reduces incidence of failure.

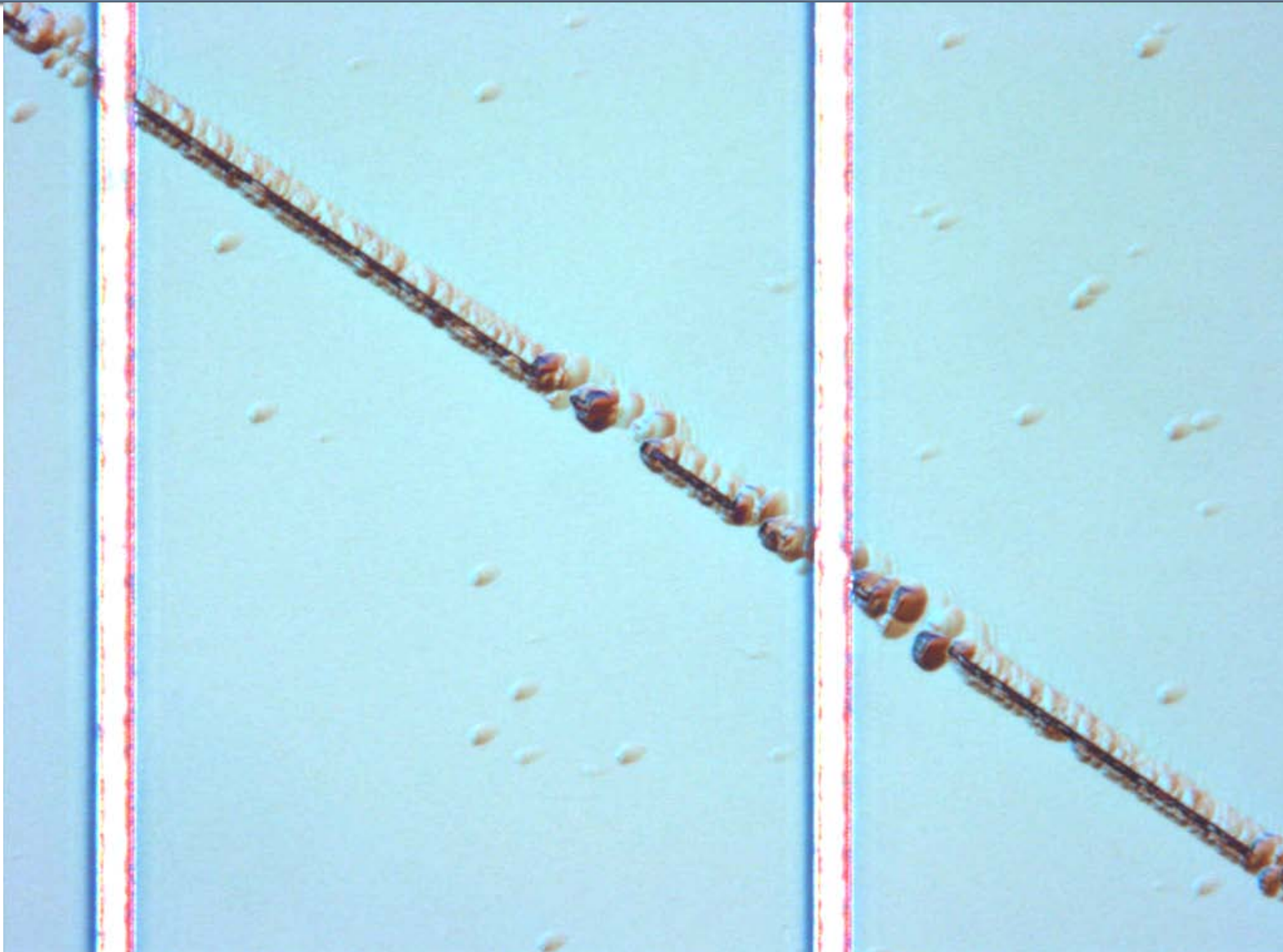
Other Things to (or not to) Worry About

- **Visual Defects**
- **Current Density?**
- **Forward Bias Induced Effects**

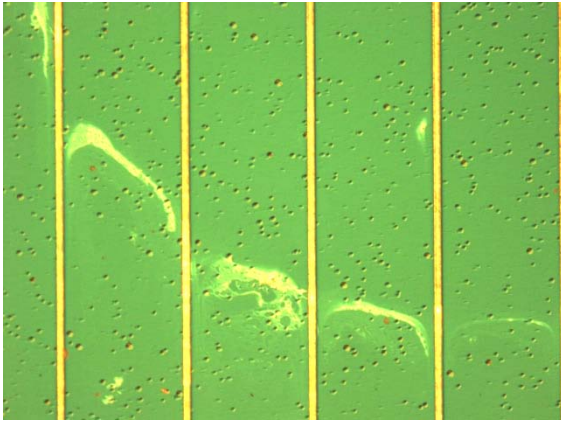
Scratch? Crack? Other?



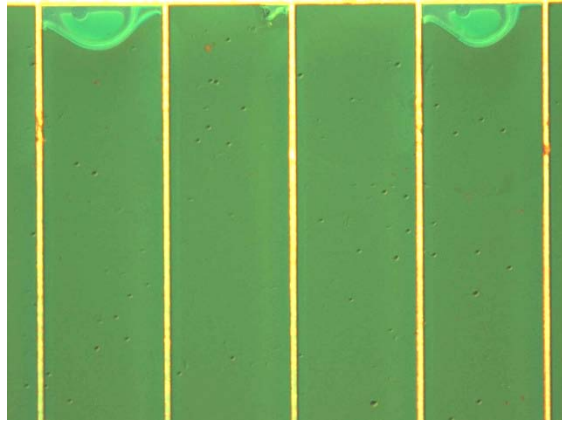
Slip Plane Dislocation



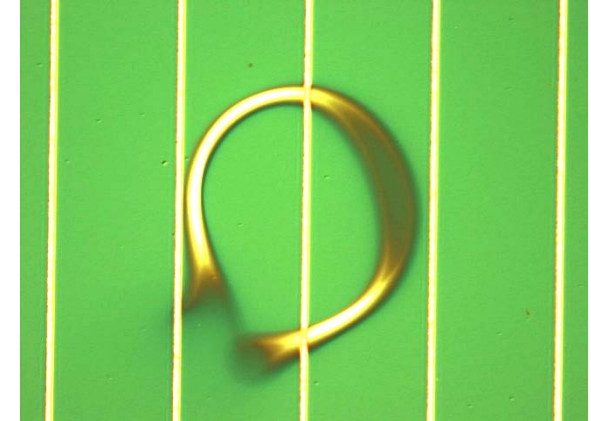
- If you look closely enough, you will find all manner of “features” on the surface of CPV solar cells!



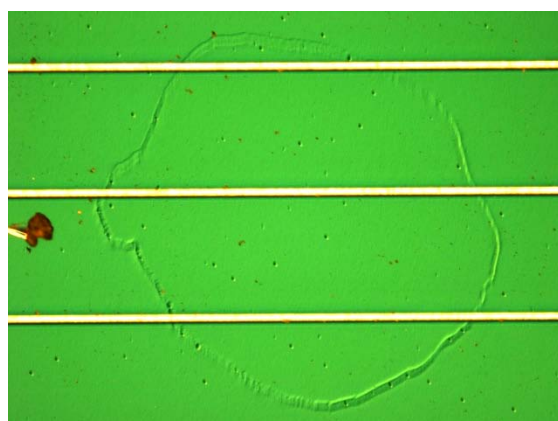
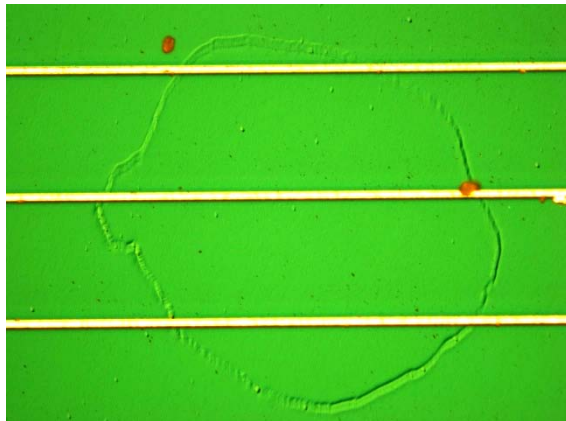
“Stacking Faults”



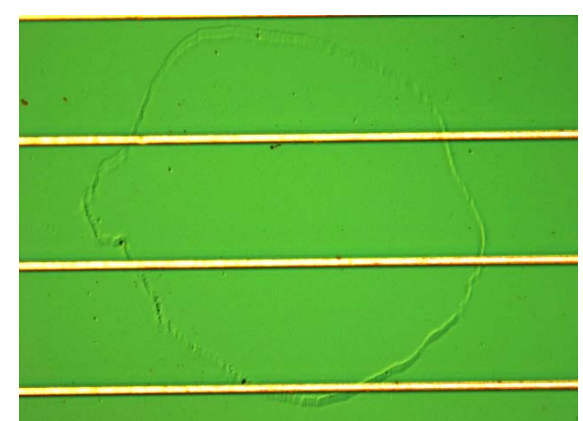
Etch Artifacts



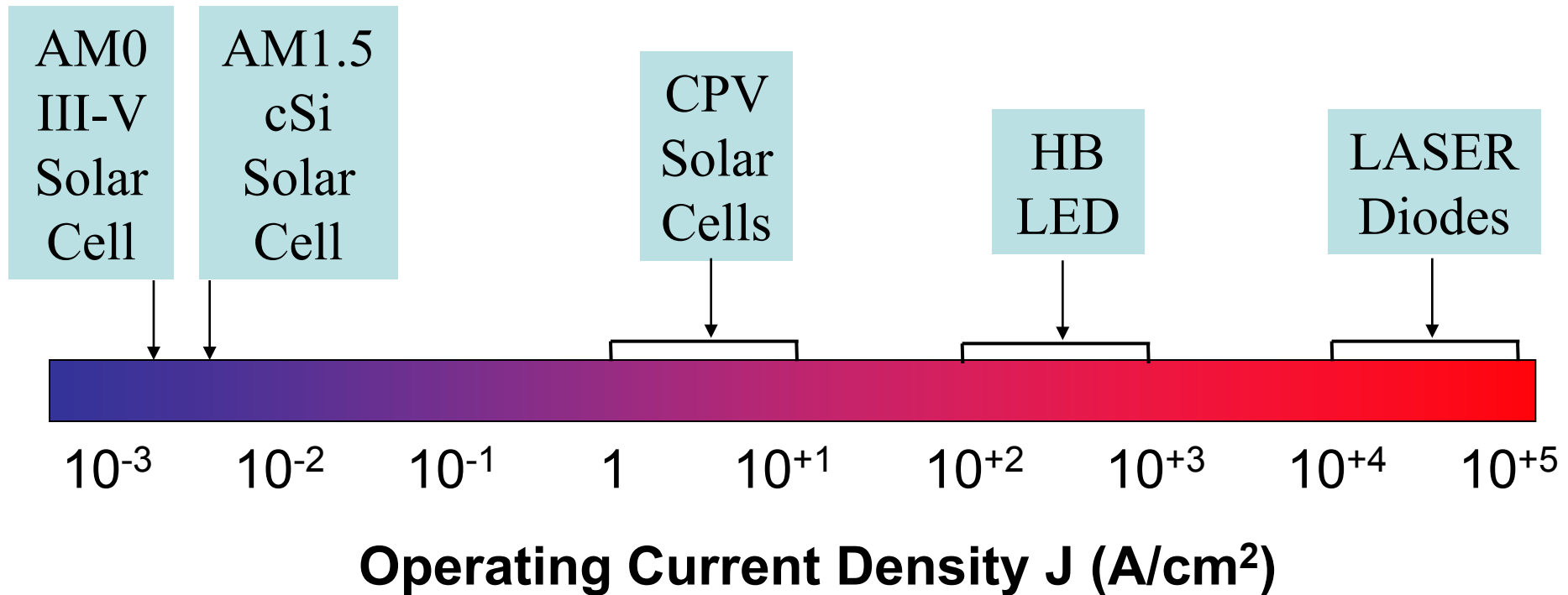
Very Tiny Gold Wedding Rings?



Handling/Litho Repeaters



Current Density in Optoelectronics Devices



Summary

Still Going



- The photo in the next slide a pair of panels that were decommissioned from an ARCO PV plant In California and then reinstalled on a roof in Northern New Mexico ca. 1995.
- Many people in the room probably know a lot more about the pedigree and jaded history of these panels than I do, but these are the essential facts:
 - The panels were originally taken out of service after the encapsulation yellowed and reduced the output power by about 15%.
 - At the time they were reinstalled a misguided drywall screw shattered the tempered face glass on the upper panel.
 - Since then the both panels have been in continuous service powering a 12V DC service in an artist's studio.
 - Both have yellowed considerably more than when reinstalled but even the shattered panel is still generating power.
- I don't have hard numbers, but the main point is that at the time these panels were built, I am guessing that there were not many predictions that they would fail prematurely due to yellowing of the encapsulate and even fewer that they would still be generating power after thirty + years in service and a shattered coverglass.

- **Rel Prediction is a tough business.**
- **CPV modules and systems are complex and opportunities for failure abound.**
- **The IEC 62108 suite of CPV module/system qualification tests provide an excellent baseline for beginning-of-life performance but little insight into long-term reliability.**
 - Accelerated Life Tests at high concentration levels are difficult to implement.
- **Hermeticity at the receiver subassembly level is critical.**

- I would like to sincerely thank all the contributors to this presentation, but especially the following current or former employees of Emcore:
 - Steve Seel
 - Hans Schoon
 - Jim Foressi
 - Dan Aiken
- And the following staff members at NREL:
 - Sarah Kurtz
 - Peter Hacke
 - Nick Bosco
 - Michael Kempe