Four Junction Solar Cell with 40% Target Efficiency Fabricated by Wafer Bonding and Layer Transfer

Subcontract XAT-4-33624-10

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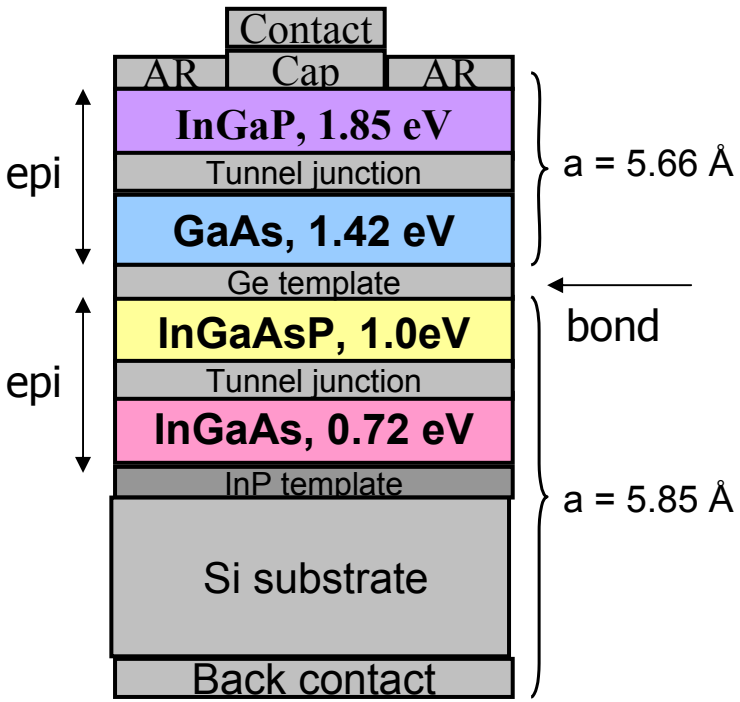
Relevance/Objective

Research objectives:

1. Develop 4 junction solar cell for high performance photovoltaic receivers
2. Develop wafer bonding and layer transfer methods for integration of lattice-mismatched multijunction solar cells

Summary of Activities



4J Cell

- 2J InGaP/GaAs/Si cell on Ge/Si or GaAs/Si template
- integration of top and bottom cells by direct bond interconnect
- 2J 'bottom' InGaAsP/InGaAs cell on InP/Si template

Summary of Activities

- Technical approach:
  - Develop 'top' 2J InGaP/GaAs/Si cell (Caltech, Spectrolab)
  - Develop 'bottom' InGaAsP/InGaAs/Si cell (Caltech, Emcore, Aonex)
  - Perform integration of top and bottom cells (Caltech)
- Participants: Caltech, Spectrolab, Aonex, Emcore
- Methods:
  - wafer bonding and layer transfer to fabricate epitaxial templates for InGaP/GaAs growth and InGaAsP/InGaAs growth
  - MOCVD growth of InGaP/GaAs and InGaAsP/InGaAs
  - direct bond interconnection of top cell and bottom cell
- Outcomes:
  - Ge/Si and InP/Si template layer process development
  - GaAs/InP direct bond interconnect development
  - GaInP/GaAs/Ge/Si cell development
  - InGaAs/InP/Si development

Budget History

Project Task(s)	Total Value
Phase 1 (8/04-8/05)	$205,000
Phase 2 (8/05-8/06)	$174,000
Phase 3 (8/06-8/07)	$146,000
Grand Total	$525,000

Accomplishments

Accomplishments to Date:

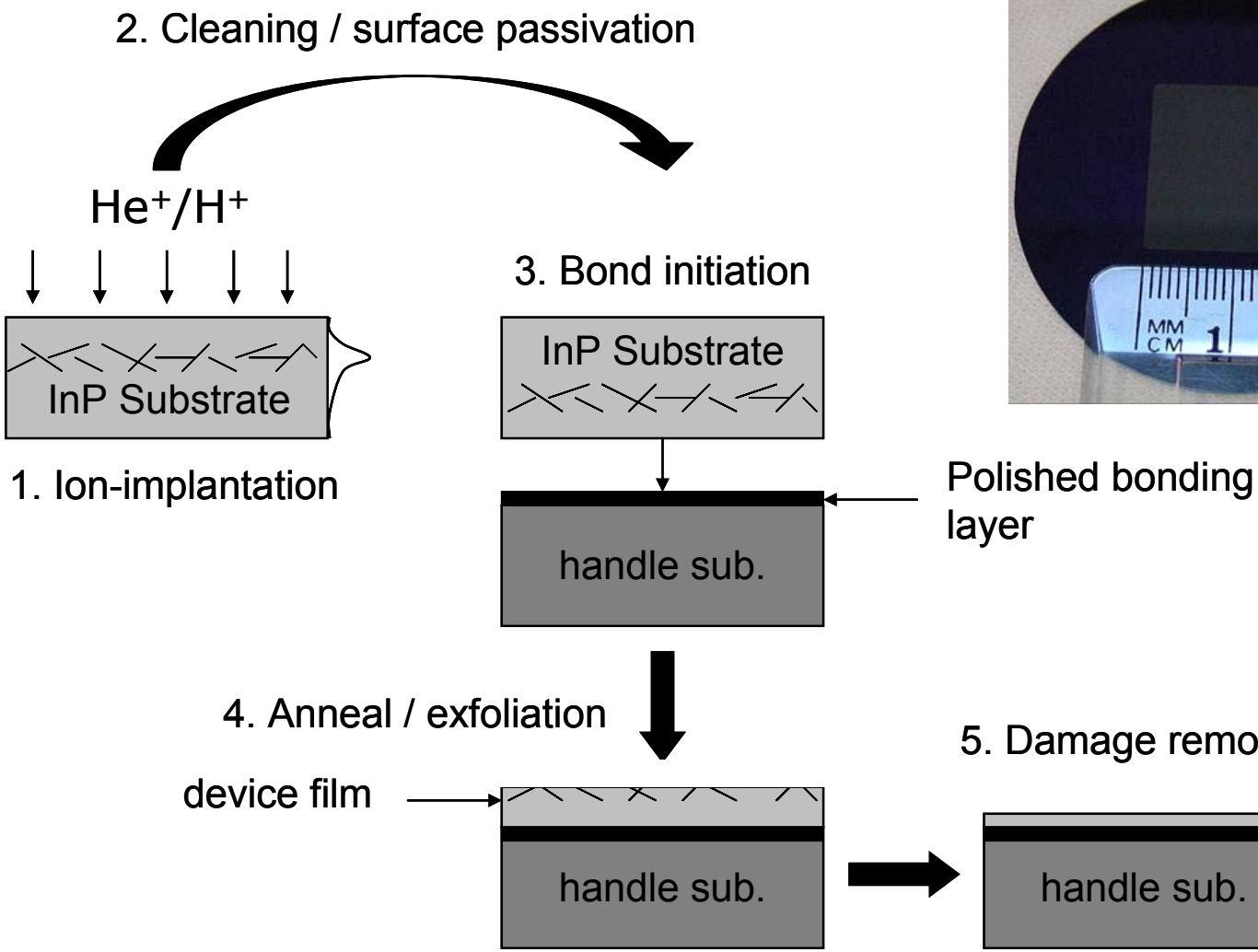
1. 'top' 2J cell demonstrated
   - Ge/Si template is dislocation-free
   - MOCVD-grown InGaP/GaAs cells on Ge/Si are crack-free
   - Surface quality on Ge template is the gating issue for cell quality

2. bottom InGaAs/InP/Si cell with superior performance to InGaAs/InP demonstrated
   - Insertion of SiO_2 layer enables light trapping in InGaAs/InP template cell

3. Optimized InP/Si template layer process developed

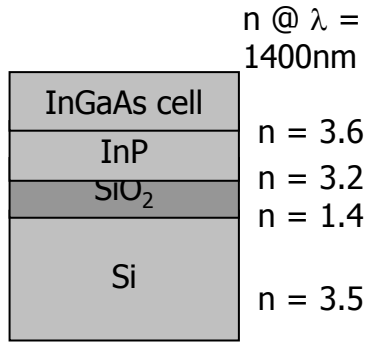
4. Almost-optimized Ge/Si template layer process developed
   - Combined wet-etch/CMP process important for epi-ready surface quality

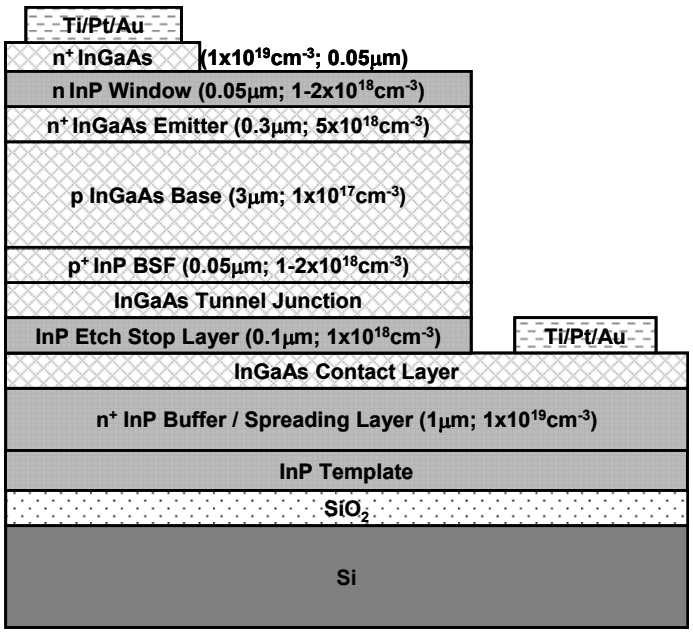
InP/Si Epi-template Fabrication

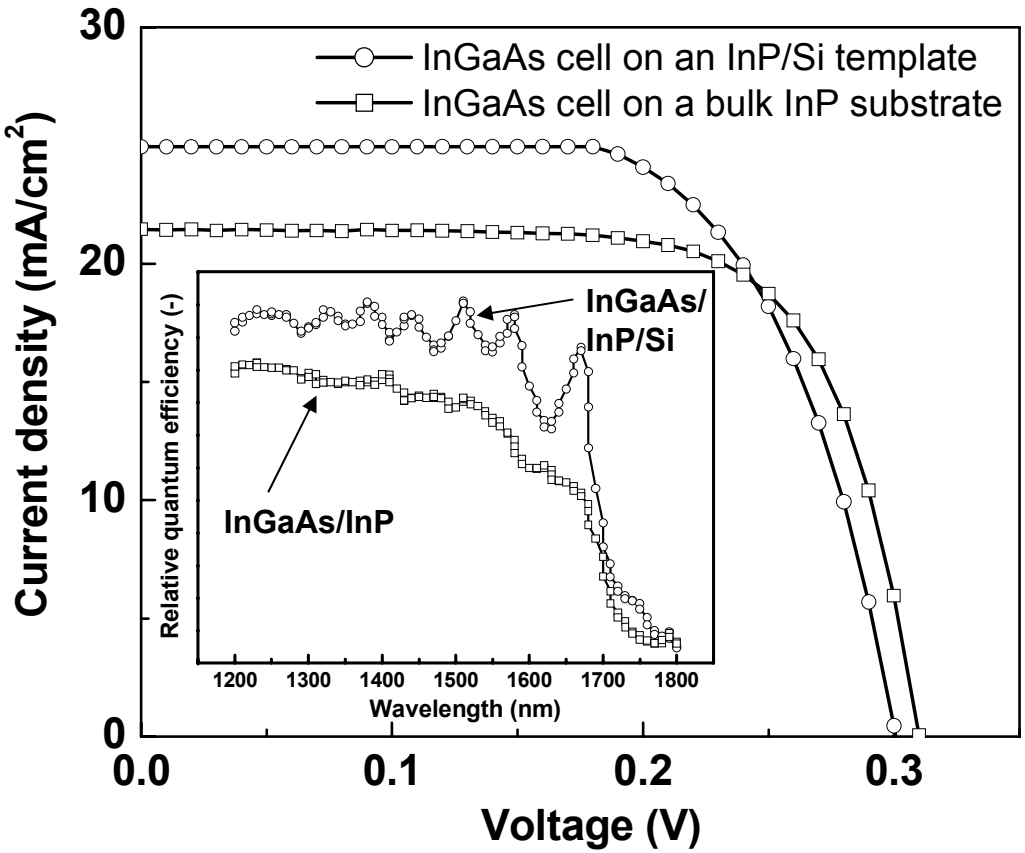


Accomplishments

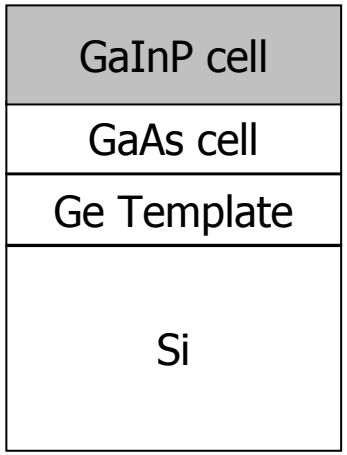
InGaAs/InP/Si Cell with Enhanced Photocurrent Collection Relative to InGaAs/InP





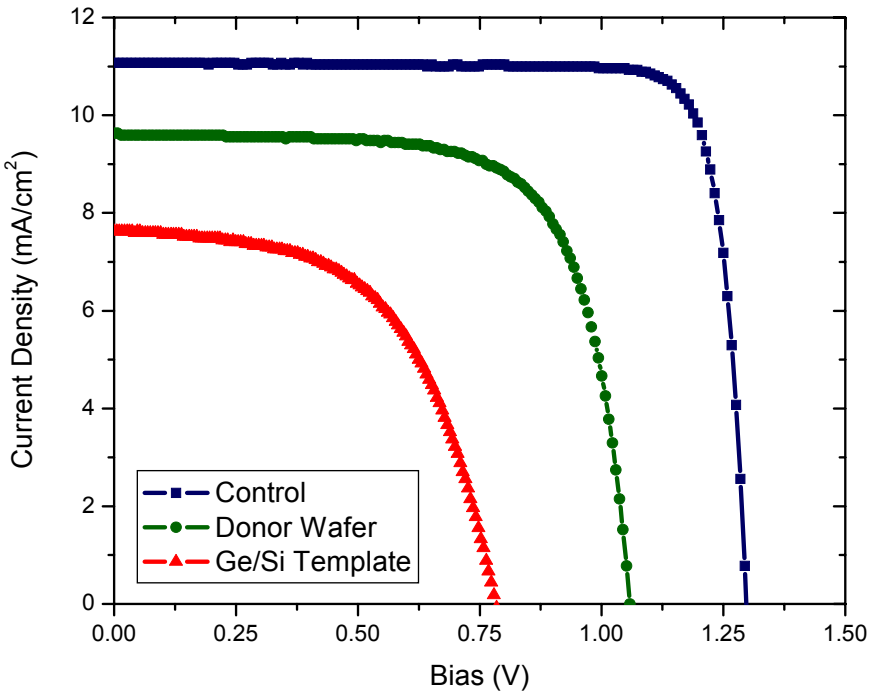


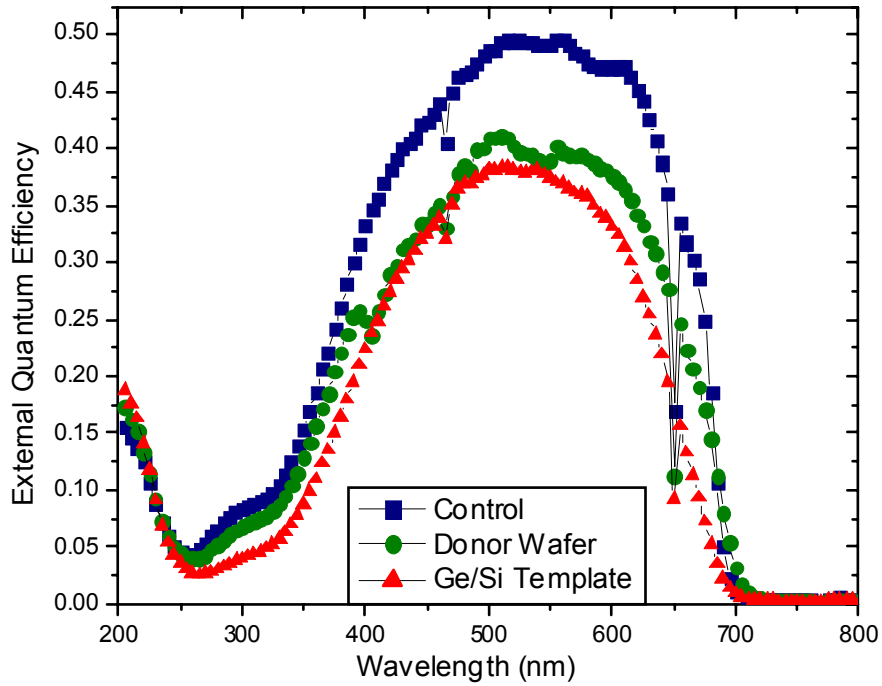
Accomplishments



GaInP Cell Performance in GaInP/GaAs/Ge/Si 2J Cell

(wet etch only Ge template preparation)





Schedule of Major Events/Milestones

Accomplished

In Progress

Phase 1

Task 1: Template Engineering
- Fabrication of InP/Si Templates
- Fabrication of Ge/Si Templates

Task 2: Subcell Design and Fabrication
- Growth of double heterostructures
- Development of GaInPAs/GaInAs/InP 2J cells
- Development of AlGaInP/GaAs 2J cells

Phase 2

Task 3:Template Improvement
- Fabrication of Improved InP/Si Templates
- Fabrication of Ge/Si Templates

Task 4: Improved Subcell Design and Fabrication
- Demonstrate GaInPAs/GaInAs 2J cells on bonded wafer
- Demonstrate AlGaInP/GaAs 2J cells on bonded wafer
- Development of AlGaInP/GaAs 2J cells

Phase 3

Task 5: 4J Integration Issues for Templates
- Address Template Integration Suitability
- Develop Direct Bond Interconnect

Task 6: 4J Bonded Cell Integration
- Fabricate Integration-ready GaInPAs/GaInAs 2J cells
- Fabricate Integration-ready AlGaInP/GaAs 2J cells

Future Directions

- Subcontract has established the basic viability of bonding as integration approach for lattice-mismatched multijunction cells.

- Near future (6 months will focus on completion of wafer-bonded subcells and demonstrated of a 3J cell with Ge and InP templated layers and a direct bond interconnect.

- Follow-on research proposed for new solicitation will carry forward the knowledge and experience gain to fabricate direct bonded multijunction cells using other thin wafer approaches (ELO, substrate removal).