Voltage Deficit in Thin-Film Polycrystalline Solar Cells

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ABSTRACT

The highest reported efficiency for thin-film CIGS solar cells is 3% larger than the highest seen with CdTe cells. The lower CdTe efficiency is the result of a much larger voltage deficit between CdTe cells and crystalline cells of similar band gap. The explanation for the difference is that CIGS has a natural energy barrier, which repels holes from grain boundaries, but CdTe does not. Significant efficiency increases in CdTe cells will therefore likely require new structures with full absorber depletion and electron reflection at the back contact.

1. Objectives

The general objectives of the research program are to elucidate key aspects of CIGS and CdTe device physics, quantify observed performance losses, and contribute to improvements in device performance. The specific objective of the work reported here is to explain why the voltage deficits seen in the best CIGS and CdTe cells are dramatically different.

2. Technical Approach

This report synthesizes the numerical-simulation results from Refs. 1 and 2 with the current-voltage data reported for the highest efficiency thin-film and single-crystal solar cells to analyze the CIGS and CdTe voltage deficits.

3. Results and Accomplishments

3.1 Introduction

The highest reported conversion efficiencies of thin-film CIGS and CdTe solar cells are 19.5%[3] and 16.5%[4], respectively. (Band-gap considerations alone would predict a 3% difference in the opposite direction.) The current-voltage (J-V) curves for the highest efficiency CIGS and CdTe cells are shown in Fig. 1. For comparison, current-voltage curves derived from those of high-efficiency single-crystal Si and GaAs cells are also shown. The reported curves for the Si[5] and GaAs[6] cells were adjusted slightly (30-40 mV in voltage, about 1 mA/cm in current density) to match the band gaps of the CIGS and CdTe cells.

The salient feature of Fig. 1 is the 230 mV voltage deficit for CdTe compared to the 30 mV deficit for CIGS. Reduction of the CdTe deficit to that of CIGS would increase CeTe cell efficiency by about 5% to approximately 22%. The obvious questions are why does such a large difference exist between the CdTe and the CIGS voltage deficit and what might be done to significantly reduce the CdTe deficit.

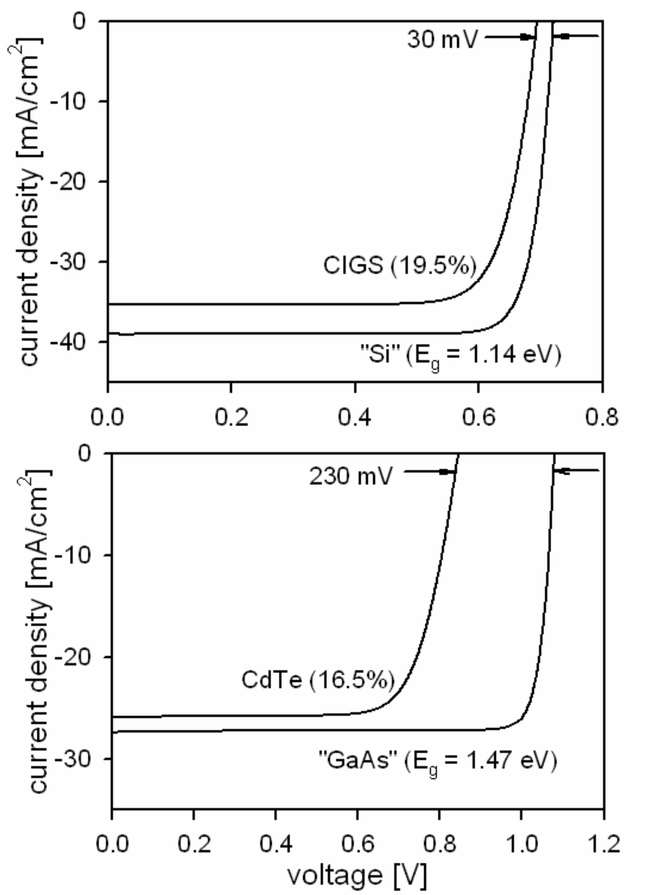

Fig. 1. J-V comparison of record-efficiency CIGS cell with high-efficiency Si adjusted slightly for band gap. Similar comparison of CdTe with GaAs.

3.2 CIGS Cells

It is quite remarkable that the CIGS voltage deficit shown above is as small as it is. For a neutral grain boundary (GB) with crystallite size the order of 1 μm, a GB recombination velocity less than 10^4 cm/s would be required for the observed voltages and efficiencies. Such a small value seems unlikely in an uneven structure unless there is a mechanism to keep the majority carrier holes away from the GBs. One mechanism often suggested is that the GBs are positively charged. However, this mechanism in itself does not yield high the voltages observed. In fact, a positive GB will allow additional forward-current recombination and result in smaller voltage than for the equivalent neutral GB.[1]

The likely explanation for the benign nature of CIGS GBs is a lower the valence band near the GB without an equivalent reduction in the conduction band.[1] This scenario is consistent with theoretical analysis of CIGS surfaces and interfaces, where a copper deficit results in an expanded band gap with a lower valence band.[7] The necessary valence-band lowering, as calculated in Ref. 1, is 0.2 eV or greater, and the hole shielding is effective even when modest GB charge exists along with the gap expansion.

3.3 CdTe Cells

The best CdTe cells are limited in voltage because of both a low hole density and low lifetime for photogenerated carriers.[2] The J-V curve shown in Fig. 1 is consistent with generally accepted values of hole density (~!0^{14} cm^{-2}) and lifetime (~1 ns).[2] Both of these problems are presumably related to defects associated with CdTe GBs.

One strategy to increase CdTe voltage significantly is to substantially reduce the GB defects, increasing both hole density and carrier lifetime, and essentially making thin-film CdTe similar to crystalline GaAs. The predicted "n-p" result is shown in Fig. 2. Attempts to move in this direction, however, have not been successful to date. Additionally, interfacial recombination at the CdS/CdTe heterojunction may become the voltage-limiting factor if the bulk CdTe properties are significantly improved.[2]

An alternative "n-i-p" strategy, also shown in Fig. 2, is a fully-depleted CdTe configuration. In this case, a conduction-band back barrier (electron reflector) of 0.2 or greater would be critical to reduce voltage-limiting recombination at the back surface.[2] The CdTe lifetime, however, need not be particularly high. A potential difficulty is that any recombination at the reflector interface may compromise the gain from blocking electrons from the contact interface.

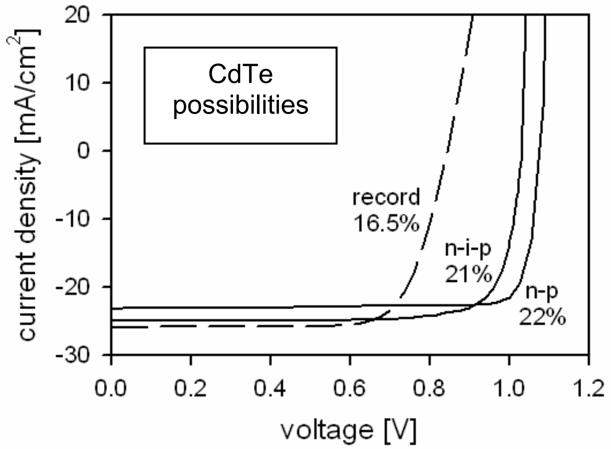

Fig. 2. Two strategies to increase CdTe efficiency.

4. Conclusions

Polycrystalline CIGS appears to have the fortuitous feature of a valence-band energy barrier that prevents holes from reaching GB defects. CdTe does not have this feature, and its voltage deficit to date has been quite large. It is suggested that the most effective strategy to achieve high voltage and efficiency is to fully deplete the CdTe absorber by thinning and/or smaller hole density and to build in an effective electron reflector at the back contact.

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