Damp Heat Effects on CIGSS and CdTe Cells

Larry Olsen, Sambhu Kundu, Mark Gross, and Alan Joly
Pacific Northwest National Laboratory, Larry.Olsen@pnl.gov
Richland, WA 99352

ABSTRACT

This paper reviews studies of the effects of moisture on thin-film CIGSS and CdTe solar cells and discusses recent studies with photoluminescence. Current voltage characteristics of bare and encapsulated cells were acquired periodically for devices undergoing stress in a 60ºC/90%RH environment for 1000 hours. Both types of cell degrade rapidly when subjected to damp heat testing. I-V analyses indicate junction and absorber properties are affected by moisture ingress. Photoluminescence studies confirm that the minority carrier lifetime decreases due to moisture ingress. The efficiency of CIGSS mini-modules encapsulated with a PNNL multi-layer, transparent barrier coating decreased only slightly after 1000 hours of stress. Similar results were obtained for encapsulated CdTe cells.

1. Objectives

In order for thin film photovoltaic manufacturers to meet lifetime, stability and cost goals of DOE for photovoltaic power production, approaches to depositing low cost, effective encapsulation of thin-film PV modules must be developed. The objectives of the work presented in this paper are to determine the effect of moisture ingress in CIGSS and CdTe modules and to determine approaches to effectively encapsulating these devices.

2. Technical Approach

Efforts have concentrated on two types of cells, CIGSS cells made by Shell Solar Industries (SSI) which have a substrate structure (Fig. 1) and CdTe devices made by Colorado State University (CSU) that have a superstrate configuration (Fig.2)[1]. Transparent multi-layered polymer/alumina coatings (referred to as PML coatings) were applied to CIGSS cells and mini-modules, while two types of coatings have been investigated for encapsulating CdTe cells, namely, both PML and opaque coatings. The opaque coatings consisted of a polymer/Al-film structure. The PML coatings consist of a relatively thick polymer layer (P-layer) followed by a thin alumina film, and then followed by pairs of polymer/alumina films (diads) [2].

Investigations have consisted of : (1) characterizing the effect of environmental stress due to 60ºC/90%RH on bare and encapsulated devices; (2) determine the effects of stress on junction properties; and finally, (3) utilize photoluminescence studies to characterize the effect of moisture on minority carrier properties.

3. Results and Accomplishments

3.1 Properties of Bare and Encapsulated CIGSS Cells

SSI provided monolithically integrated thin-film CIGSS circuits, each of which consist of ten cells connected in series on a 10 cm x 10 cm glass substrate. Each cell is approximately 0.69 cm x 8.3 cm. A border region of approximately 0.8 cm was depleted by SSI for the purpose of these studies to allow a smooth coating at the edge of the circuit. Prior to coating CIGSS circuits, the surfaces were cleaned to remove any loose debris that might cause defects in coatings which in turn can cause pathways for moisture ingress. These problems would not exist in a production process. Due to the rough surface of CIGSS films, it was determined that the first polymer layer (P-layer) needed to be several microns in order to minimize defect formation in barrier coatings.

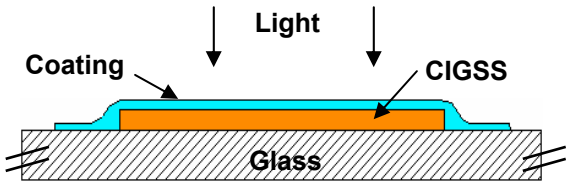

Fig. 1. Substrate configuration for coated CIGSS cell.

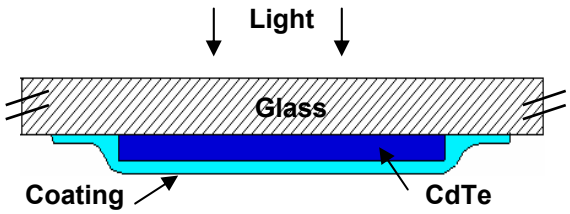

Fig. 2. Superstrate configuration for coated CdTe cell.

Results for coated mini-modules with two thicknesses for the P-layer and an uncoated module are shown in Fig.3. The efficiency of an uncoated circuit degrades very rapidly, becoming less than 1% within 400 hours. Moisture ingress affects all cell parameters. It is clear that a five dyad coating with a P-layer of several microns provides very good encapsulation for SSI circuits. If the P-layer is too thin, water spots will appear, particularly along a cut made as a step in the monolithic integration process.

Damp heat stress affects all basic cell properties. Table 1 gives average values of single device parameters for dark I-V characteristics of an uncoated SSI mini-module before and after damp-heat testing. Values of parameters were determined for voltages in the 0.2 to 0.5 Volt range. The A-value remaining nearly unchanged before and after stress suggests that the dominate recombination center in the depletion region is unchanged. On the other hand, the J_o-value increases by more than two orders of magnitude as a result of stress, which suggests that the number of defects responsible for recombination increases accordingly.

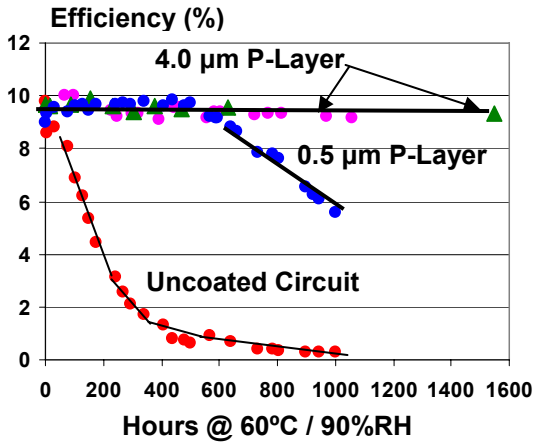

Fig. 3. Efficiency versus time for three encapsulated min-modules and one uncoated CIGSS circuit.

Table 1 -- I-V Parameters For SSI CIGSS Circuit

Beginning of Life	R_s = 1.8 ohms J_0 = 1.5E-8 A/cm^2 A = 1.80
After 1000 hrs in Damp Heat	R_s = 3.6 ohms J_0 = 5E-6 A/cm^2 A = 1.88

3.2 Properties of Bare and Encapsulated CdTe Cells

A collaborative investigation of barrier coatings for CdTe cells is being carried out with Dr. Sampath at Colorado State University. The CSU CdTe cells are fabricated with a superstrate configuration. Data for cell efficiencies vs time are given in Fig. 4 for bare CSU devices and encapsulated CSU cells subjected to an environment of 60ºC/90%RH. One cell was encapsulated with a five dyad coating and the other with the aluminum based coating. The decline in efficiency is due almost entirely to a decrease in the fill factor, or specifically increased series resistance. From other studies it is clear that the degradation is due to the effect of the temperature of 60ºC. Since the bare cells degrade very rapidly in the 60ºC/90%RH environment, one can conclude

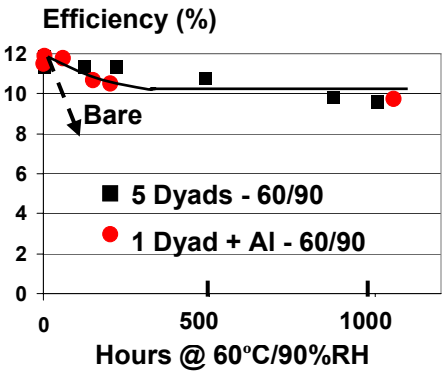

Fig. 4 Efficiency versus time for bare and coated CdTe cells.

that both types of barrier coating are effectively preventing moisture ingress under these conditions.

3.3 Photoluminescence Studies

Time resolved photoluminescence (TPL) is being used to study the effect of moisture on minority carrier properties. The effective lifetime for the CdTe absorber in a CSU cell before being stressed was determined from the data presented in Fig. 5 to be ~ 475 psec. After 1440 hours at 60ºC/90%RH, the lifetime decreased to 335 psec. Thus it is clear that the damp heat caused a degradation in the minority carrier lifetime. Similar studies with CIGSS cells are underway.

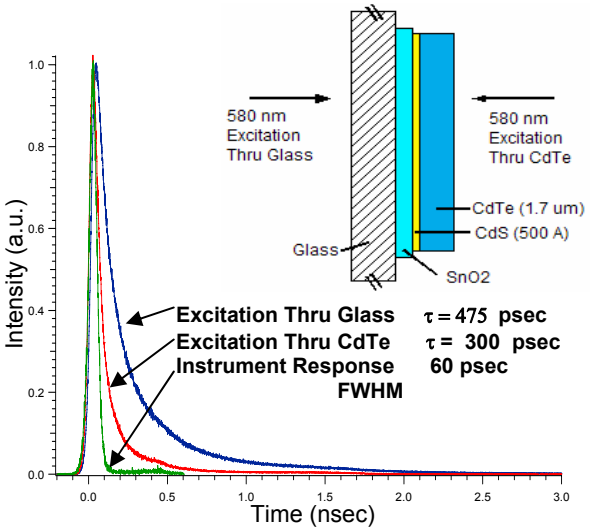

Fig. 5 Time resolved PL for unstressed sample.

4. Conclusions

Damp heat studies of CIGSS and CdTe cells have been conducted by subjecting cells and min-modules to an environment 60C/90%RH. Two key conclusions can be made: (1) Both CIGSS and CdTe cells degrade rapidly under 60C/90%RH unless they are protected with a barrier coating; (2) Damp heat stress will cause changes in the junction transport properties and minority carrier transport characteristics of the cell absorber.

ACKNOWLEDGEMENTS

This work was supported by NREL subcontract 48027 under DOE contract DAX-4-44239-01.

REFERENCES

1. K.L. Barth, R.A. Enzenroth and W.S. Sampath, "Consistent Processing and Long Term Stability of CdTe Devices," pages 323-326, 31st IEEE PVSC (2005).
2. LC Olsen, SN Sambhu, CC Bonham and M Gross, "Barrier Coatings for CIGSS and CdTe Cells," pages 327-330, 31st IEEE PVSC (2005).