

Thin CIGS Devices and Modules produced using the Simplified Hybrid Process

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ABSTRACT

Research results obtained by Energy Photovoltaics, Inc. ("EPV") during the past year under its CIGS subcontract are reported. Advances in the following areas were achieved: (a) deposition of thin and ultra-thin samples; (b) reduction of substrate temperature for CIGS; (c) improvement of CIGS surface by different treatments; (d) monitoring of the Cu-rich / Cu-poor transition during CIGS growth; and (e) use of textured window layers to increase useful light absorption. The first three advances were implemented in modules.

1. Objectives

This project aims to produce high quality CIGS over large areas by scalable and consistent methods and to solve module-related problems so that high performance, glass-based modules can be prepared. To reduce potential manufacturing costs, we are currently seeking to reduce CIGS thickness from the 2.5 μm range as much as possible and to reduce growth temperatures to limit glass warping.

2. Technical Approach

EPV has already reported the success of the "simplified hybrid (SH) process" in which Cu is supplied by magnetron sputtering and In, Ga and Se are supplied by evaporation. Two CIGS systems are in use, one for recipe development and one for large area deposition. We have recently designed and built accurate source controllers for the smaller system, and with greatly improved process reproducibility we are now engaged in end-point detection and process optimization. In the device area we seek to optimize performance via CIGS surface treatment and via use of novel techniques to improve the window (TCO) layer.¹ We are also active in alternative back contact research and back reflectors for ultra-thin CIGS.

3. Results and Accomplishments

CIGS devices with a range of thicknesses were prepared using the SH process and with the baseline structure SLG/Mo/CIGS/CdS/i-ZnO/n-ZnO. It is found that the device efficiency progressively drops from 13% to 10% as thickness decreases from 1.3 μm to 0.5 μm . At 0.5 μm , the current density decreases significantly because of insufficient light absorption at long wavelengths, but FF and V_{oc} are also reduced presumably because of back surface recombination. These reductions occur despite our attempt to increase the Ga content near the Mo. The variation of efficiency with thickness is shown in Figure 1 for devices with no grid or AR coating.

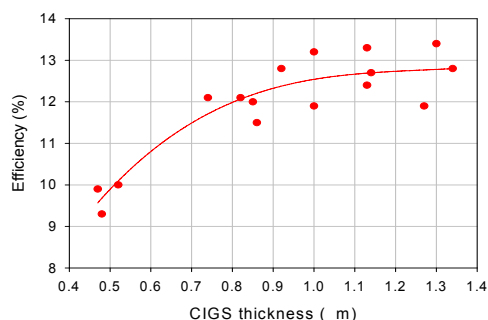


Fig. 1. Thickness dependence of device efficiency.

For efficiency verification, we deposited a Ni/Al grid and AlF_3 AR coating on a good sample (CIGS thickness 1.13 μm) and sent the cells to NREL. The best result was a 14.0% cell, as shown in Figure 2.

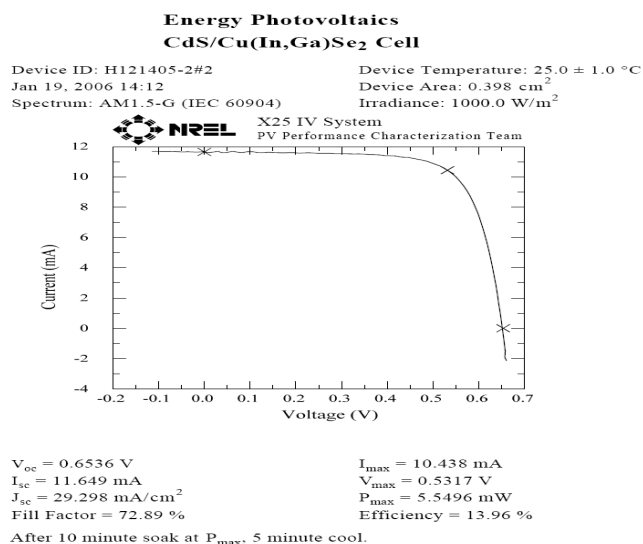


Fig. 2. I-V curve for 14%, 1.13 μm thick CIGS device.

EPV's SH process is designed to pass through a Cu-rich to Cu-poor ($\text{Cu}/\text{In}+\text{Ga} < 1$) transition. During this transition, the film emissivity falls.² We have monitored this transition using a thermocouple attached to the substrate. Figure 3 shows dV/dt versus time for the

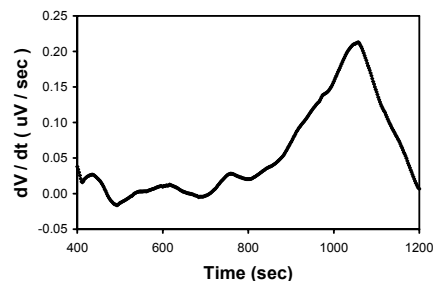


Fig. 3. Time dependence of dV/dt during CIGS growth.

thermocouple voltage V during CIGS deposition. The time at which the sharp rise in dV/dt is observed (at about 800 sec) is assigned to the onset of the Cu-rich to Cu-poor transition.

Previous optimization of the temperature T_s for CIGS growth concluded that $T_s = 535^\circ\text{C}$ was optimal (here T_s is the temperature of the substrate holder, the actual glass temperature is higher). We have repeated this study using the SH process. Table 1 summarizes device performance for CIGS (Ga content 32-35%) grown with three different temperature profiles (constant at 535°C , constant at 495°C , and graded from 495°C to 475°C) and for CIGS with Ga content 26% grown with the graded temperature profile. For the SH process, the optimal temperature is clearly lower than 535°C . (The see-saw effect of Ga content on V_{oc} and J_{sc} is also evident.)

Table 1. Effect of T_s on device performance

Run	$T_s^\circ\text{C}$	V_{oc} (mV)	J_{sc} (mA/cm ²)	FF%	Eff%
1	535	585	29.2	66.6	11.4
2	495	578	30.8	71.2	12.7
3	495*	592	32.8	65.6	12.7
4	495*	557	34.1	62.7	11.9

* T_s graded from 495°C to 475°C

A post-deposition treatment of the CIGS is a standard step in EPV's processing. Table 2 shows device results obtained with the standard treatment (T1) and a new treatment (T2). We believe that the T2 treatment helps to remove Cu_xSe from the CIGS.

Table 2. Device results with different CIGS treatments

Sample	V_{oc} (mV)	FF (%)	J_{sc} (mA/cm ²)	Eff (%)	Treat ment
A	582	68.0	29.2	11.6	T1
B	580	73.9	28.7	12.3	T2

We have previously reported the use of reactive-environment hollow cathode sputtering (RE-HCS) to apply ZnO:B window layers to CIGS. More recently we have prepared textured ZnO:Al on CIGS devices. Figure 4 shows the QE response for CIGS devices having smooth and textured ZnO window layers.

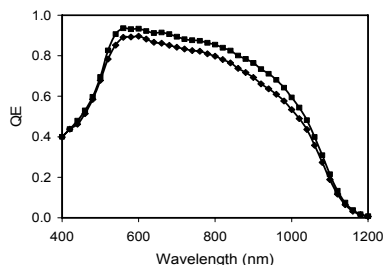


Fig. 4. Improvement of QE by use of textured ZnO.

The enhanced QE increases J_{sc} by about 6%. We have confirmed that the cell reflectivity is reduced.

Modules have been produced with reduced CIGS thicknesses around $1.3 \mu\text{m}$, reduced T_s , and post-

deposition treatment. Table 3 shows the performance of a representative module (#1807, 47 segments, 2332 cm^2 , $J_{sc} = 23.8 \text{ mA/cm}^2$). The degraded performance of the module is ascribed to the following factors: a) deficiencies in the CIGS absorber (quality and homogeneity); b) change in dimension of the SL glass substrate due to high temperature processing (this causes P1-P2 scribe misalignment); and c) power loss due to higher than desired ZnO:Al sheet resistance and ZnO-Mo contact resistance. The dimensional changes were detected using a long-base micrometer caliper. The problems with the CIGS, ZnO, and P1-P2 alignment are understood and soluble.

Table 3. Performance of large area module

V_{oc} (V)	V_{oc}/cell (mV)	I_{sc} * (A)	FF (%)	P (W)	Eff (%)
24.8	528	1.185	54.0	15.9	6.8

* outdoor measurements normalized to one sun

4. Conclusions

We focused during this period on optimizing the simplified hybrid process in the thickness range 0.8 to $1.3 \mu\text{m}$. A device efficiency of 14.0% was achieved at $1.1 \mu\text{m}$, with prospects for further improvement. The Cu-rich to Cu-poor transition was detected via the emissivity change of the growing film; this is to be correlated with CIGS composition. A useful gain in device J_{sc} was realized via use of a textured top TCO.

ACKNOWLEDGEMENTS

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REFERENCES

1. A.E. Delahoy, S. Guo, J. Cambridge, R. Lyndall, J.A. Anna Selvan, A. Patel, A. Foustotchenko, B. Sang, "Reactive-Environment Hollow Cathode Sputtering: Compound Film Production, and Application to Thin Film Photovoltaics," 4th World Conf. on Photovoltaic Energy Conversion, Hawaii, 2006, pp. 327-332.
2. N. Kohara, T. Negami, M. Nishitani and T. Wada, *Jpn. J. Appl. Phys.* **34**, L1141 (1995).

MAJOR FY 2006/2007 PUBLICATIONS

- L. Chen, B. Sang, M. Akhtar, R. Govindarajan, S. Guo, A. Delahoy, M. Contreras, "Development of Large Area, High Efficiency, Thin Film CIGS Modules," 15th Intl. Photovoltaic Science and Engineering Conference, Shanghai, 2005, pp. 85-88.
- S.Y. Guo, W.N. Shafarman, A.E. Delahoy, "TiN and TiO₂:Nb Thin Film Preparation using Hollow Cathode Sputtering with Application to Solar Cells," *J. Vac. Sci. Technol. A* **24(4)**, 1524 (2006).
- A.E. Delahoy, L. Chen, B. Sang, "Uniform, High Efficiency, Hybrid CIGS Processing with Application to Novel Device Structures," Annual Technical Report, March 15, 2005 – March 14, 2006; also, National CIS R&D Team Meeting, Denver, CO, April 6-7 (2006).