High Efficiency, Low-Cost, Multijunction Solar Cells Based on Epitaxial Liftoff and Wafer Bonding

Pre-Incubator

Photovoltaics: Long Term

Rao Tatavarti

MicroLink Devices Inc

rtatavarti@mldevices.com

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Overview

U.S. DEPARTMENT OF ENERGY | Energy Efficiency & Renewable Energy

Timeline

- Project start date: 29 March 2010
- Project end date : 29 March 2011
- Percent complete: 10%

Barriers

- Barriers addressed
  - Material Utilization & Cost
  - Efficiency
  - Manufacturing Processes

Budget

- Total project funding
  - DOE share: $500k
  - Contractor share: $125k
- Funding received in FY09: $0
- Funding for FY10: $100k

Partners

- Interactions/ collaborations: UCLA
- Project lead: Prof. Mark Goorsky

Challenges, Barriers or Problems

- This pre-incubator addresses the challenge of making concentrated photovoltaic (CPV) systems cost-competitive and reliable

- The technical barriers addressed are
  - Manufacturing cost reduction
  - Module cost reduction
  - Reliability improvement

- This program address the SETP mission to make solar power cost-competitive with conventional electricity sources by 2015 by providing low-cost, higher-efficiency solar cells for CPV systems applications

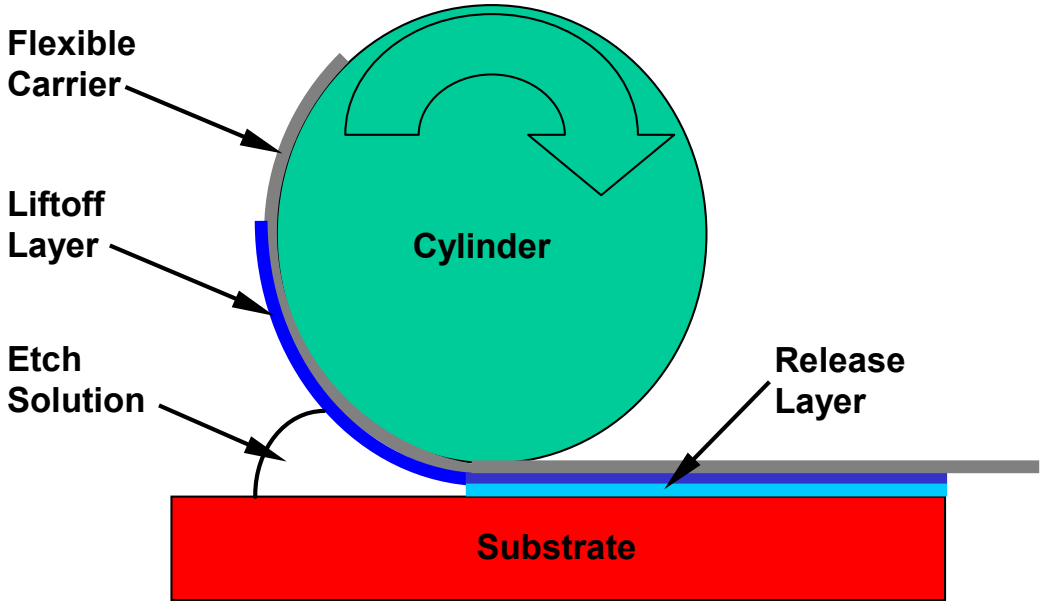
Increased cell efficiency → Reduced solar power cost ($/kWh)

Objectives and Relevance

- The objective of this pre-incubator program is to develop new solar cell manufacturing technology by combining:
  - Epitaxial liftoff technology
  - Wafer bonding
- This approach will address the following technical barriers:
  - Reduction of manufacturing cost of solar cells by lowering the material cost
  - Reduction of module costs of CPV systems by providing higher efficiency solar cells
  - Potential to improve the reliability of CPV systems by using solar cells made from lattice matched materials
- In this talk we will present
  - Our current baseline technology
  - New technology
  - Work performed in the past two months

Technical Approach: ELO Process

- Grow III-V structure on substrate with release layer
- Apply flexible carrier to top of structure
- Remove release layer by chemical process
- Structure lifts off in one piece
- Transfer to temporary carrier for processing

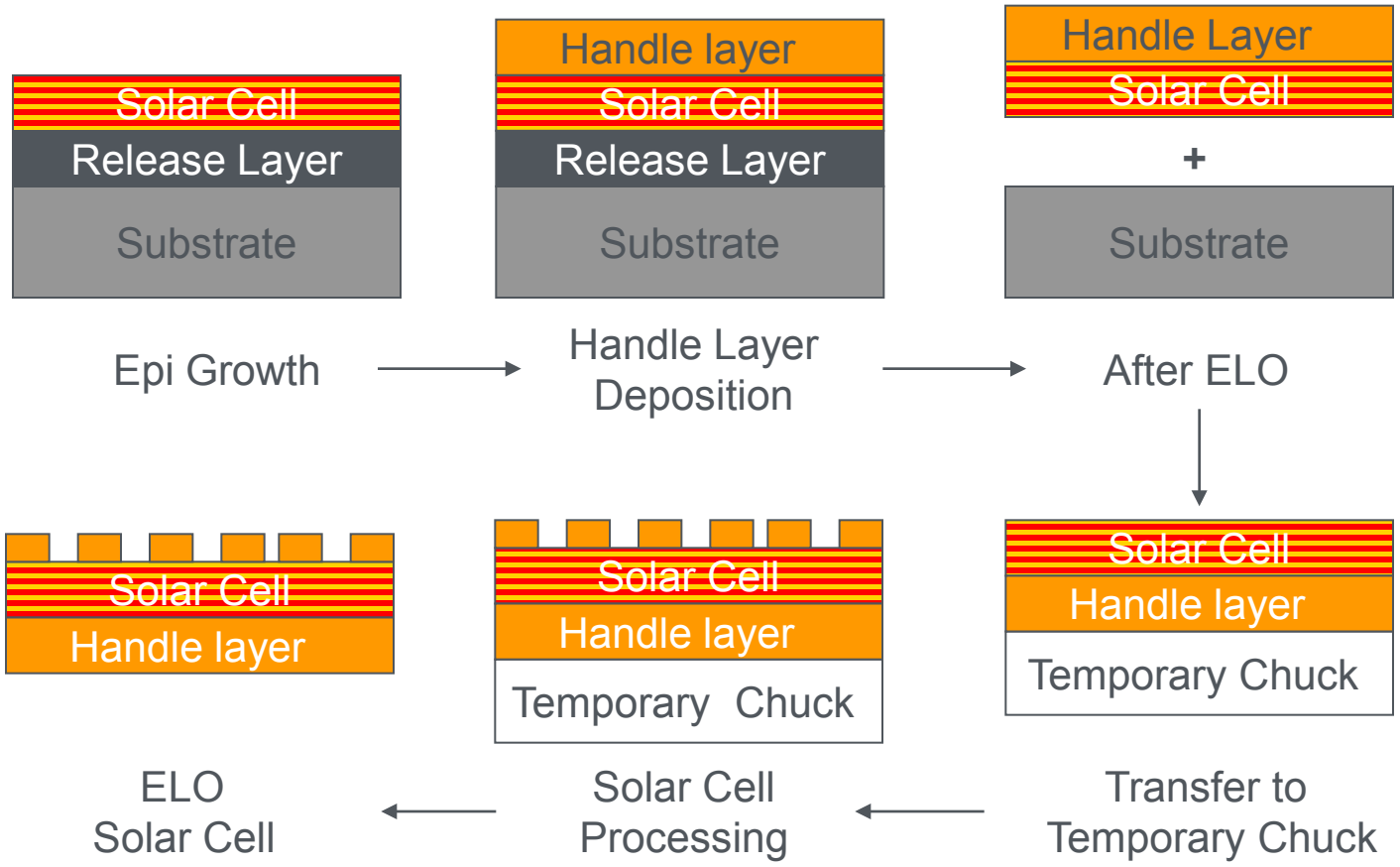


Technical Approach: ELO Benefits

- Substrate can be reused several times to reduce cost
- Consistent with fabrication of complex structures
  - Liftoff does not damage devices
- Very thin liftoff layer - everything below the grown structure removed
  - Low thermal impedance – reduces operating temperature thereby increasing cell efficiency
  - Flexible – use materials in new situations
  - Lightweight – enables unique aeronautic and space applications
- Works for GaAs, InP and other III-V materials

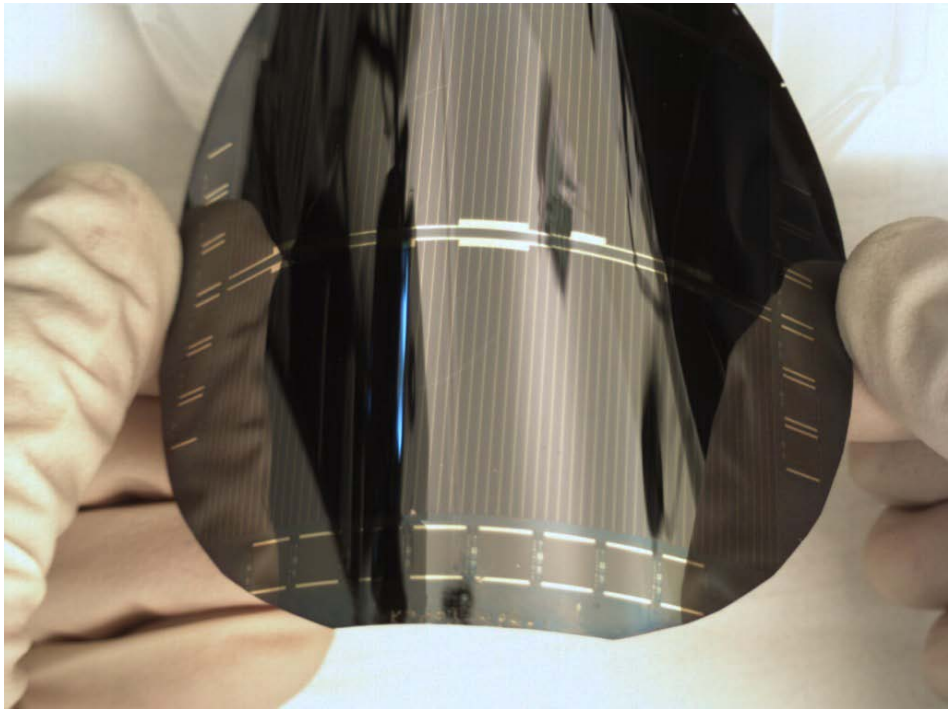
ELO approach addresses manufacturing cost technical barrier

Technical Approach: ELO Solar Cell Process Flow



Technical Approach: ELO Solar Cells

Flexible ELO Wafer

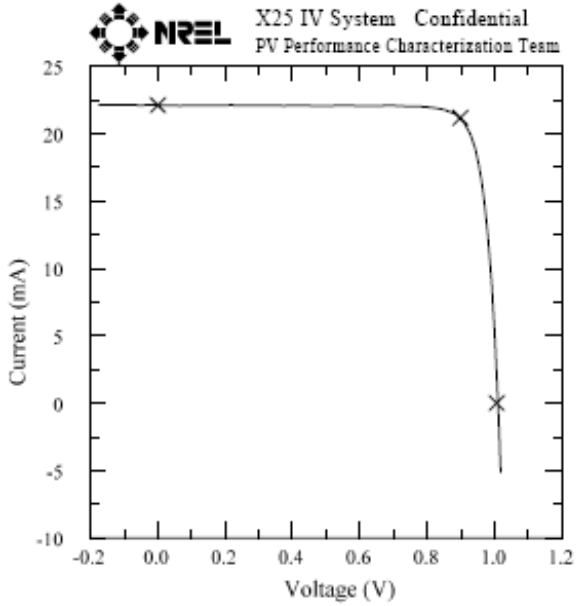


Processed ELO Solar Cell Wafer

ELO Solar Cells

Device ID: 1-1958-2
Feb 15, 2008 07:49
Spectrum: AM1.5-G (IEC 60904)

Device Temperature: 25.0 ± 1.0 °C
Device Area: 0.901 cm^2
Irradiance: 1000.0 W/m^2



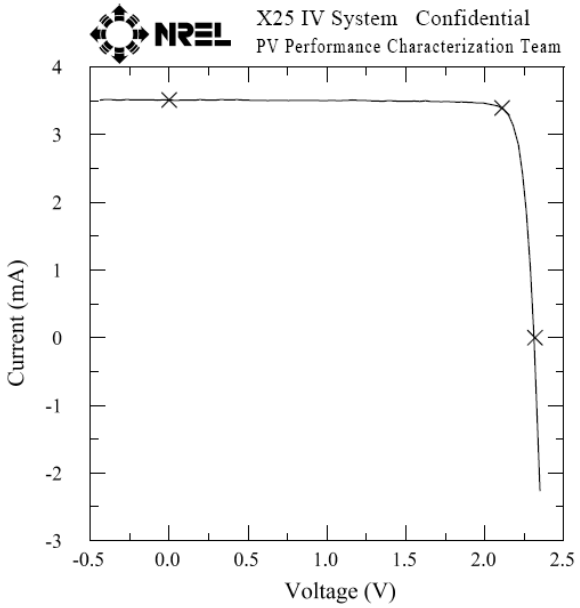
V_{oc} = 1.0071 V
I_{sc} = 22.110 mA
J_{sc} = 24.539 mA/cm^2
Fill Factor = 85.44 %

I_{max} = 21.170 mA
V_{max} = 0.8984 V
P_{max} = 19.020 mW
Efficiency = 21.11 %

GaAs single-junction cells

Device ID: 1-2692-2 E13
Feb 19, 2009 18:30
Spectrum: ASTM G173 direct

Device Temperature: 24.9 ± 0.5 °C
Device Area: 0.2529 cm^2
Irradiance: 1000.0 W/m^2



V_{oc} = 2.3172 V
I_{sc} = 3.5120 mA
J_{sc} = 13.888 mA/cm^2
Fill Factor = 87.91 %

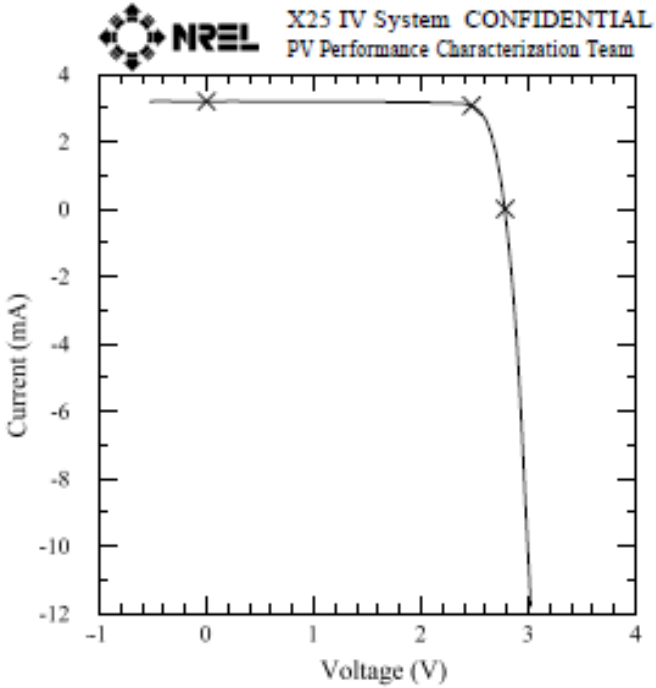
I_{max} = 3.3920 mA
V_{max} = 2.1089 V
P_{max} = 7.1540 mW
Efficiency = 28.29 %

InGaP/GaAs dual-junction cells

High Efficiency Triple Junction Solar Cells

Device ID: 1-2906-2 D-7
Apr 16, 2009 13:50
Spectrum: ASTM G173 direct

Device Temperature: 24.9 ± 0.5 °C
Device Area: 0.2523 cm^2
Irradiance: 1000.0 W/m^2

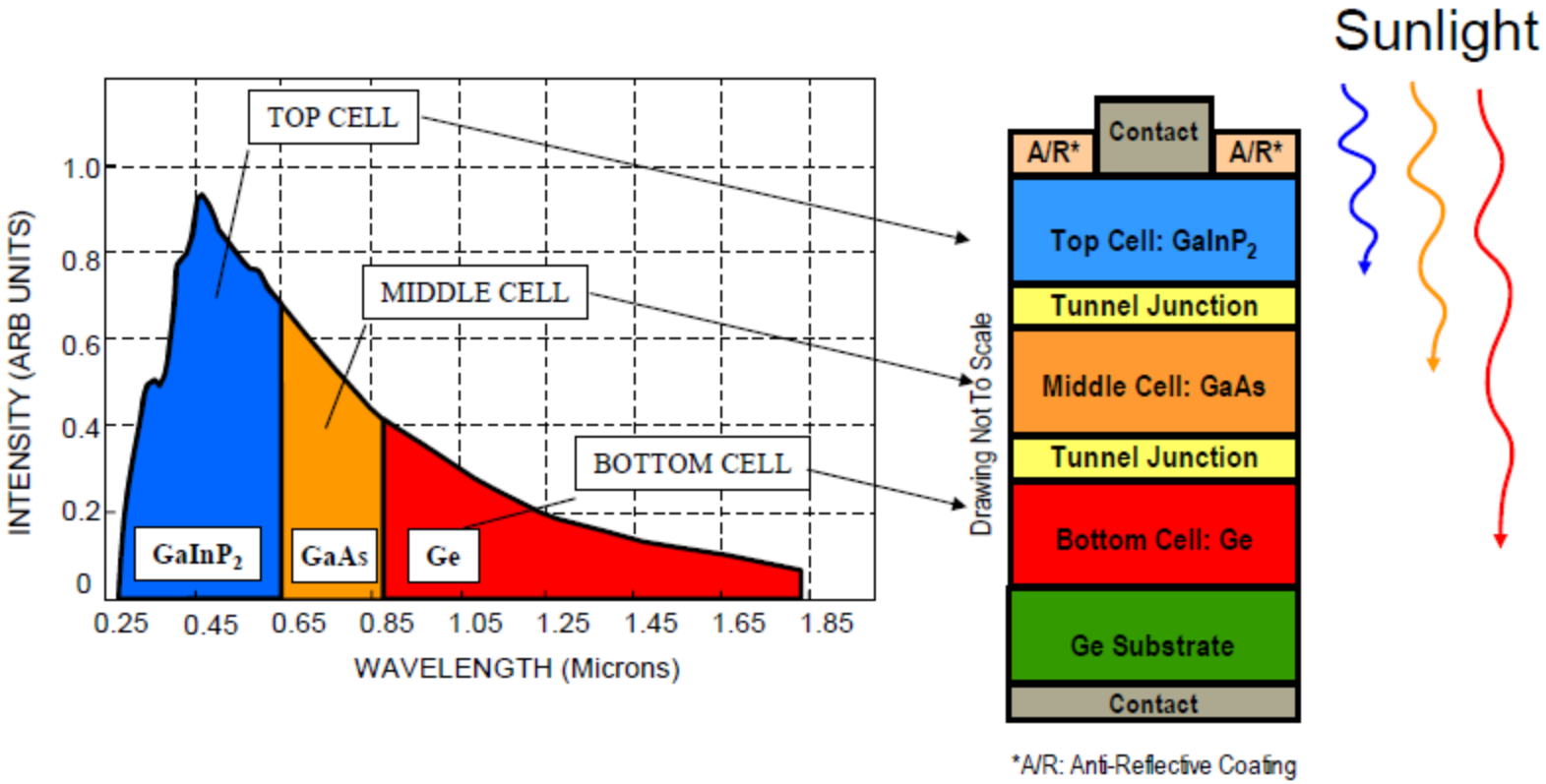


V_{oc} = 2.7823 V
I_{sc} = 3.1911 mA
J_{sc} = 12.648 mA/cm^2
Fill Factor = 85.28 %

I_{max} = 3.0658 mA
V_{max} = 2.4696 V
P_{max} = 7.5714 mW
Efficiency = 30.01 %

Triple junction cells with >30% efficiency

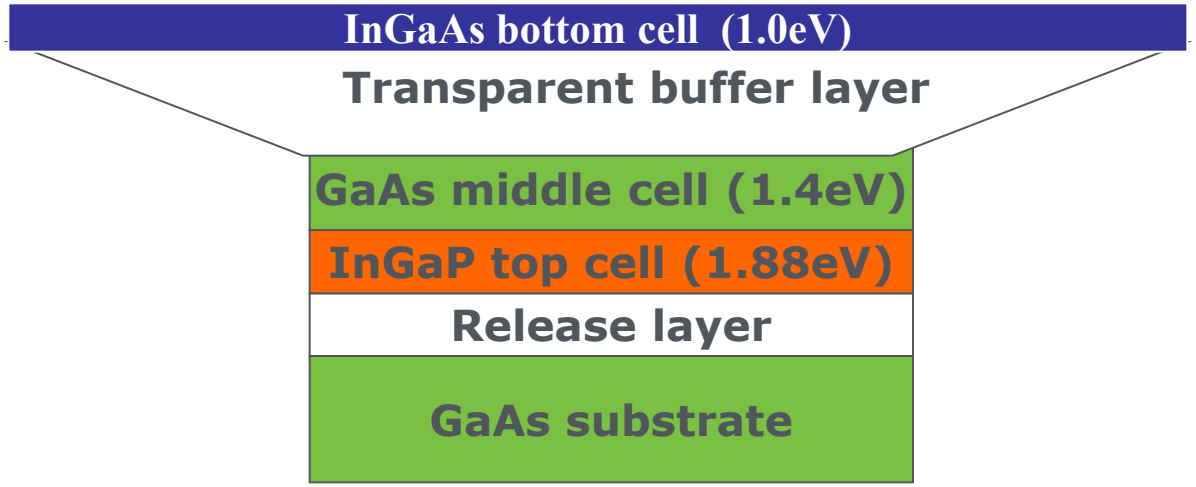
Technical Approach: n-Junction Solar Cell - Efficiency >35%



Increase number of junctions → higher efficiency

Diagram from : R.A. Sheriff et.al, Solar Power 2006

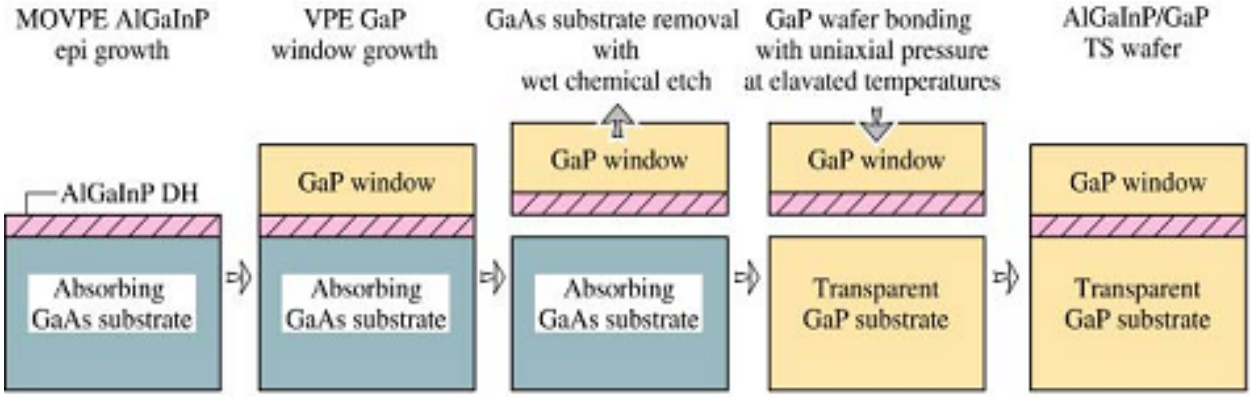
Triple Junction ELO Solar Cells - IMM



- IMM design involves combing materials with two different lattice constants
  - Thick graded buffer
- Higher efficiency designs need more junctions in materials with different lattice constants
- Highly dislocated buffer layers unknown reliability

Wafer Bonding Technology

- Wafer bonding between dissimilar A^3B^5 materials was developed in order to have more flexibility in the design of optoelectronic components
- AlGaAs/GaP LEDs were developed at HP and are in mass production



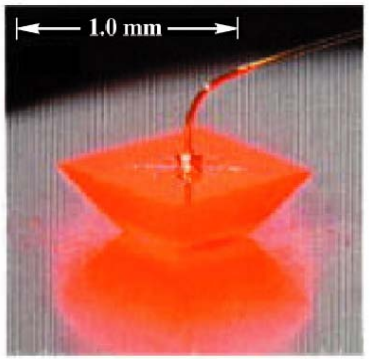


Diagram source:
http://www.rpi.edu/~schubert/Light-Emitting-Diodes-dot-org/chap06/left.htm
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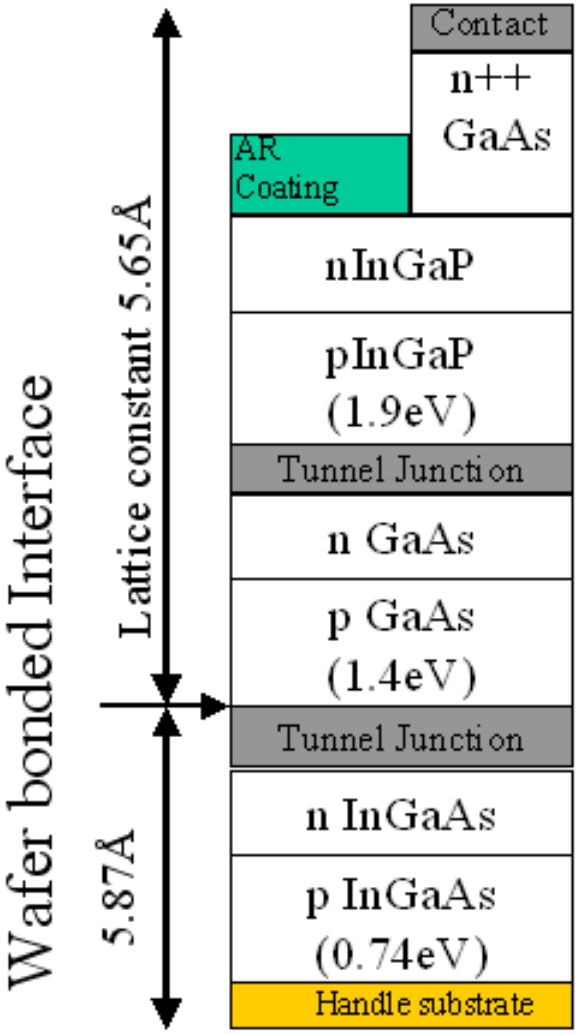
Wafer Bonding



- Eliminates graded and dislocated buffers
- Mix and match lattice constants and bandgaps
- Use of lattice-matched materials improves reliability
- Wafer bonding is extensively used in IC and LED manufacturing

Wafer Bonding and ELO for Solar Cells

- Eliminates graded buffers
  - Improves reliability
- Reduces growth time
  - Improves manufacturability
- Wafer reclaim reduces cell cost
- Higher efficiency can be achieved by making cell with four or more junctions
  - Higher efficiency cells reduce cost of CPV power

Accomplishments / Progress / Results – 29 March to 10 May 2010

- Hardware baseline deliverable
  - Three 0.5 x 0.5 cm^2 working triple-junction cells
  - InGaP/GaAs/InGaAs IMM ELO solar cells tested under AM1.5D at one sun illumination
  - Triple junction ELO cells delivered on a full 4-inch wafer

Accomplishments / Progress / Results – 29 March to 10 May 2010

- Cell design
  - Three junction wafer bonded solar cell based on lattice-matched materials grown on GaAs and InP has been developed
  - Two components:
    - A - GaInP (1.88 eV) / GaAs (1.42 eV) lattice matched to GaAs
    - B - GaInAsP (1.0 eV) or InGaAs (0.74 eV) lattice matched to InP
  - Wafer bonded cell: GaInP/GaAs/(InGaAsP or InGaAs)

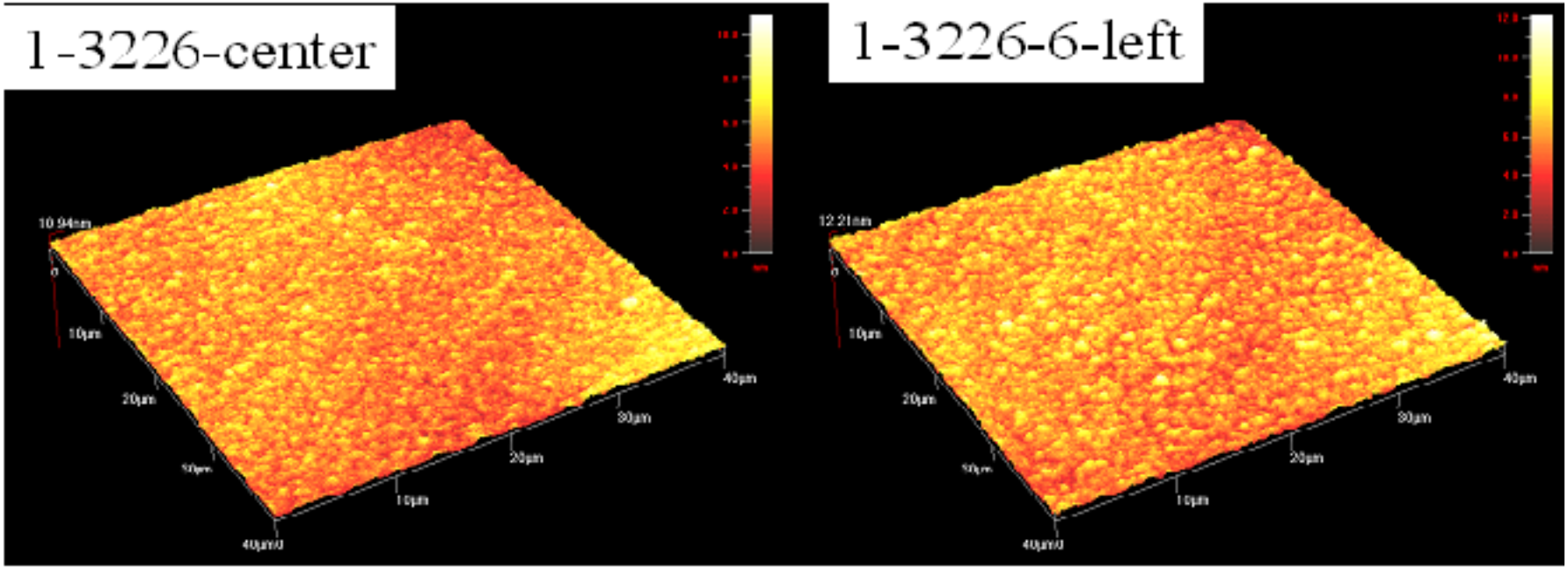
  - Work in process to optimize MOCVD growth for design B
  - In house technology already available for design A

Accomplishments / Progress / Results – 29 March to 10 May 2010

- Atomic Force Microscopy (AFM)
  - AFM studies of InP and GaAs wafer surfaces indicated average surface roughness < 1 nm
  - AFM studies of InP and GaAs epitaxial wafer surfaces indicated average surface roughness >2 nm
  - Surface roughness <1 nm is necessary for successful wafer bonding

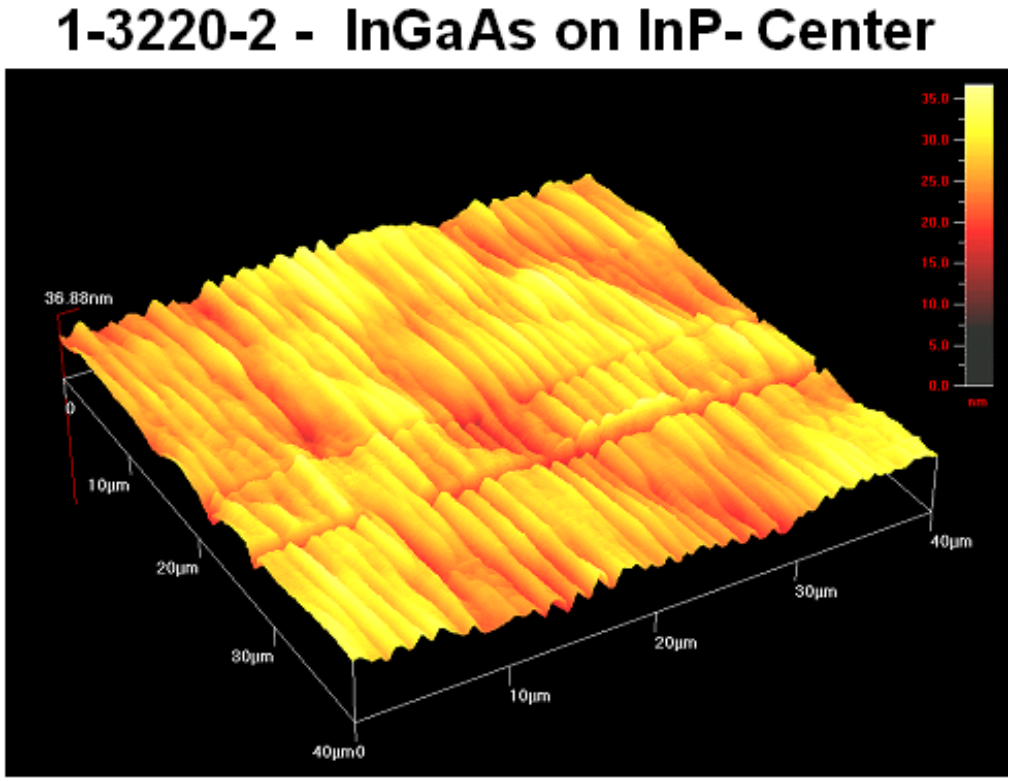
AFM studies of GaAs epitaxial solar cell surfaces

1-3226-6 Dual junction inverted solar cell



Epitaxial surfaces on GaAs substrates: r.m.s 1 nm to 1.3 nm

AFM studies of InP epitaxial solar cell surfaces



Epitaxial surfaces on InP substrates r.m.s 2 nm to 2.5 nm

Task 3: Wafer Bonding

Successful wafer bonding of semiconductor to semiconductor requires

- **Efficient surface activation process**

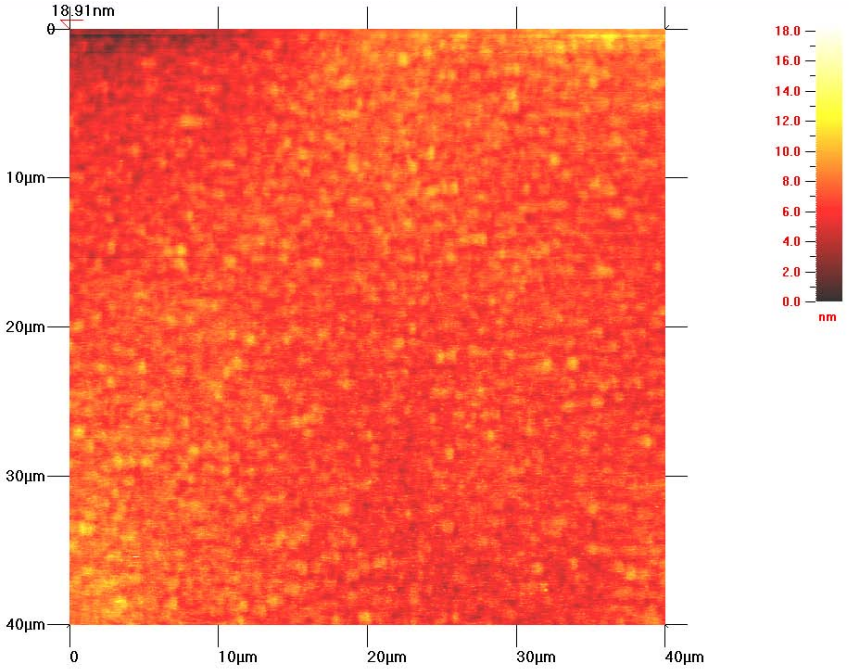
Surface activation such as S-termination is essential for low temperature wafer bonding

- **Smooth bonding surfaces**

Bonding surfaces with average surface roughness <1nm are necessary for low temperature wafer bonding

Semiconductor surface activation
Semiconductor surface smoothness

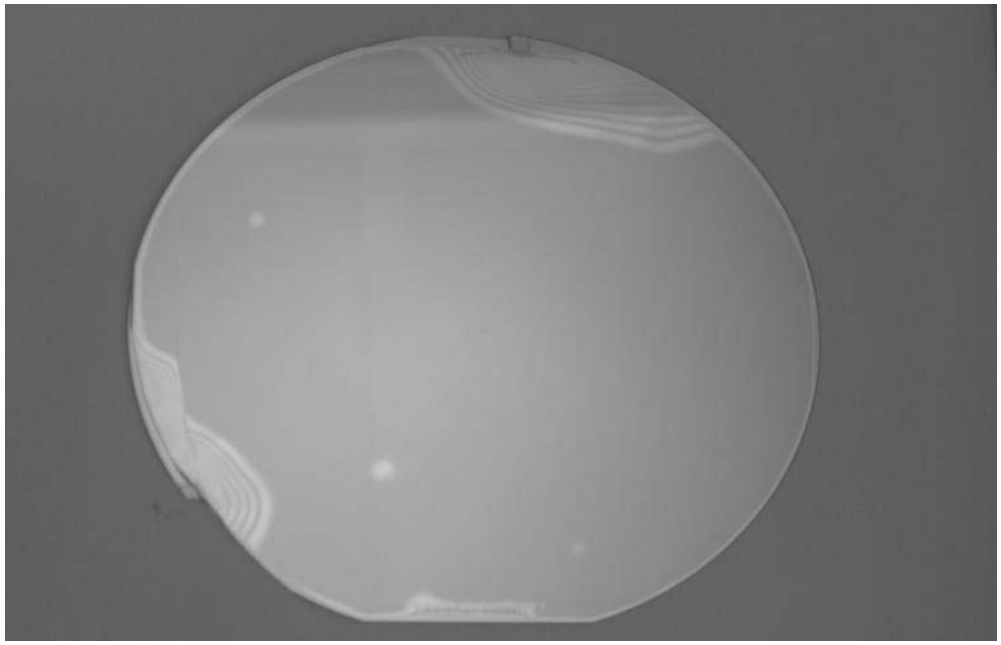
Semiconductor surface activation



- S-termination of GaAs and InP surfaces results in oxide free surfaces
- Facilitates low temperature (<450 ºC) wafer bonding

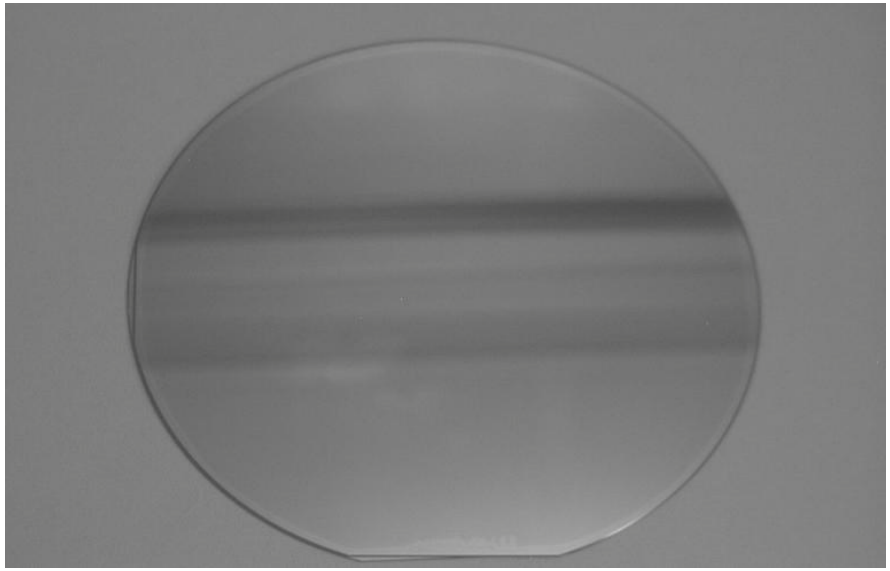
- AFM images after S-treatment:
  - GaAs surface r.m.s 11 Å
  - S-treatment does not increase surface roughness

IR image of GaAs-GaAs wafer bonded sample

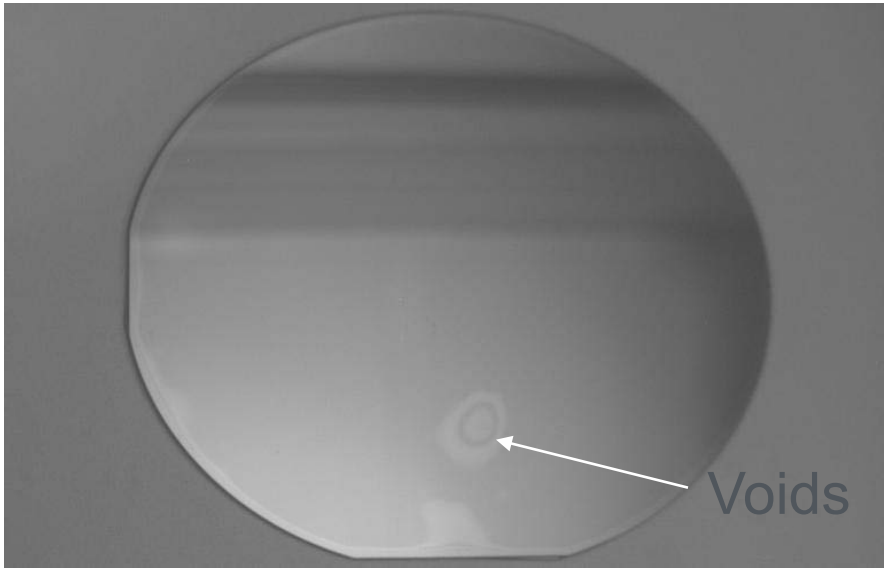


- S-treated
- Bonded at T< 450 °C

IR images of bonded InP-GaAs wafers



Sample 1



Sample 2

- InP-GaAs substrate wafer bonding: 4 inch wafers

Upcoming Tasks FY 2010

- Reduction of InP Epitaxial surface roughness to <1nm
- Wafer-bonding process to bond InP-based and GaAs-based solar cells

- Key upcoming deliverable: Sept 2010
  - Wafer bonded InGaP/GaAs/InGaAs solar cells with 25% efficiency at AM1.5, one sun illumination

- Risk mitigation path
  - Wafer fusion at higher temperatures
  - Substrate Etch

Collaborations

Prof. Mark Goorsky, UCLA.

Wafer bonding process development

And analysis

Summary

- Critical parameters for wafer bonding of epitaxial surfaces such as surface roughness are identified
- Wafer bonding between GaAs and GaAs substrates achieved on 4” wafers
- Wafer bonding between GaAs and InP substrates achieved on 4” wafers
- Work is in progress to achieve bonding between GaAs and InP epitaxial surfaces
- Work in progress to reduce the InP epitaxial surface roughness

Summary Table

Performance Metric or property	Prototype/ Component /Material	Status in FY09	Result in FY10	Notes
Eff >25% @ 1 sun, AM1.5D	Wafer bonded 0.25cm2 cell	N/A	Sept'2010-deliverable hardware	