

# Assessment of Silicon Nanowire Architecture for PV Application

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**Project Title** **Assessment of Silicon  
Nanowire Architecture for PV Application**

Program Team: Los Alamos National Lab, Sharp Labs of America

**Presenter: S. Tom Picraux**

Organization: Los Alamos National Laboratory

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Date: May 10, 2010

## Timeline

- Project start date: Jan. 2010
- Project end date: Dec. 2012
- Percent complete: 10%

## Budget

- Total project funding:  
\$1,049,443 (FY10-13)

## Barriers

Project assesses two key barriers to Si nanowire (nanopillar) photovoltaics:

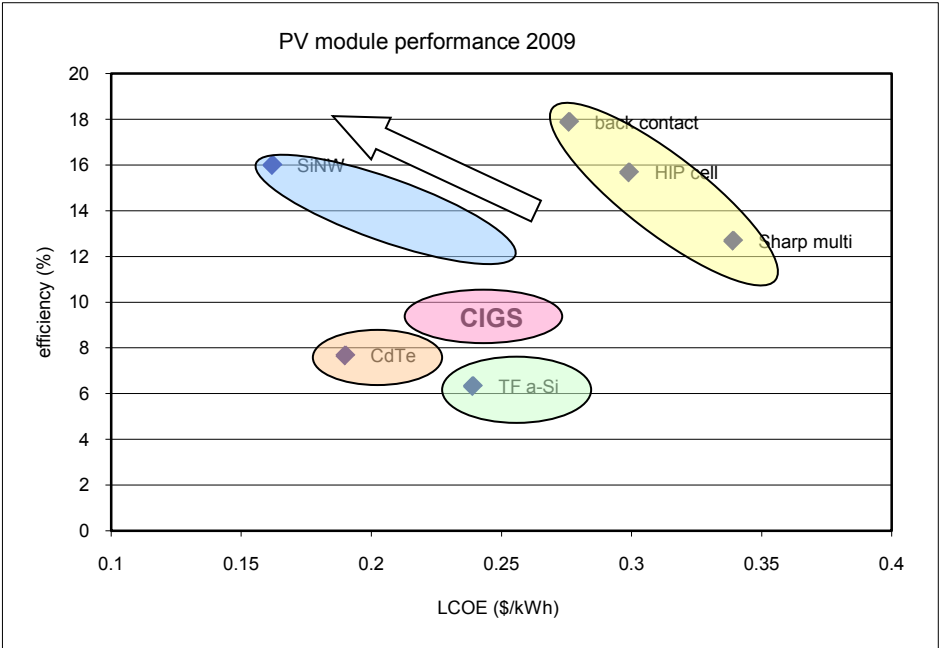
1. Achieving high PV efficiency (assess potential efficiencies via metal-catalyst-free structures).
2. Achieve low cost manufacturing (assess nanowire synthesis on stainless steel substrates).

## Partners

- Project lead:
  - Los Alamos National Laboratory
- Project partner
  - Sharp Laboratories of America

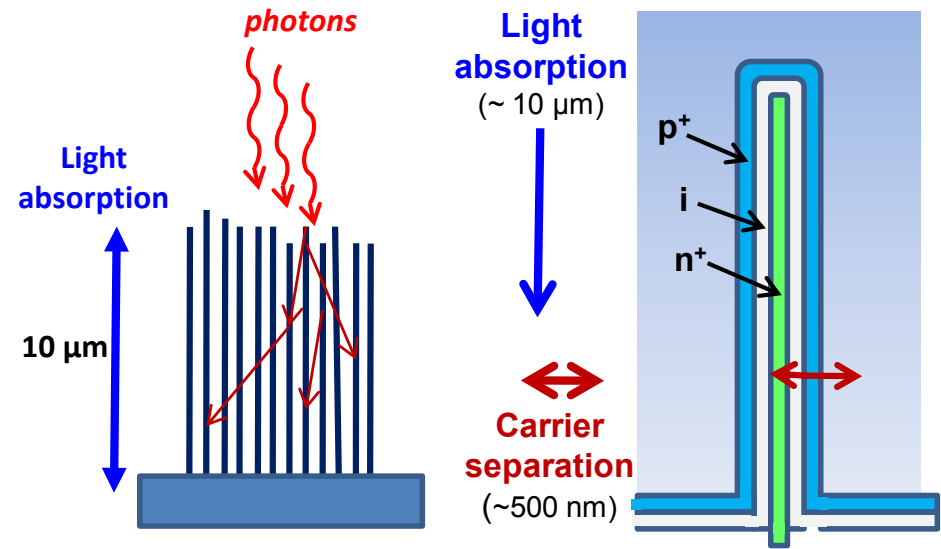
- Objective: The objective of this project is to experimentally determine whether silicon nanowire solar cells can achieve performance close to that of crystalline silicon cells but with the much lower costs of thin film, amorphous Si solar cells.
- Impact: The above performance would lead to a new class of high quality, crystalline solar cells with a cost of ~\$0.5/W and a module levelized cost of energy (LCOE) reduced by  $\frac{1}{3}$  to  $\frac{1}{2}$  from current silicon photovoltaic technology

## Levelized Cost of Energy analysis



(Based on NREL – LCOE calculator)

## Solar energy harvesting concept



*Decouple light absorption and carrier collection*

There are two closely related areas of risk which could impact the objectives of the nanowire PV concept:

1. It may not be possible to grow silicon nanowire PV cells on flexible substrates with single crystal silicon quality performance (efficiency) and sufficient wire density; and
2. The total expense of fabricating crystalline silicon nanowire PV cells may be too great to achieve the low-cost benefits of a thin film approach.

This project has been structured to assess and mitigate these potential barriers throughout the course of the work.

1. Metal-catalyst-free Si pillars will be fabricated by top-down methods and radial p-i-n nanowire PV devices grown by CVD processing to assess the ultimate efficiencies which may be achievable by a radial nanowire solar cell approach.

*Nanowire growth of single crystal Si pillars will rely on metal-catalyzed growth. Questions on the influence of metal contamination on observed efficiencies are difficult to separate from inherent issues of architecture design of achieving high efficiencies. Our approach will bypass the metal issue for assessing ultimate efficiencies and optimal designs.*

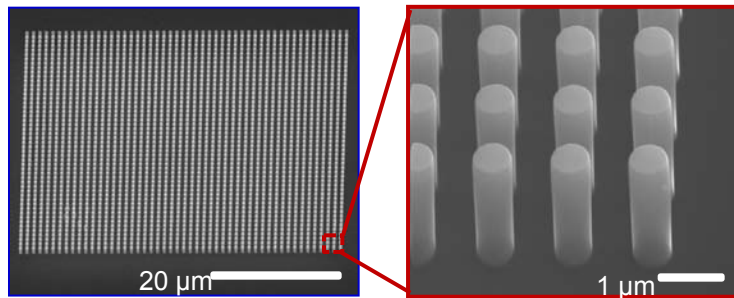
2. Silicon nanowire p-i-n PV devices will be grown by the bottom-up CVD approach on flexible stainless steel substrates to assess the potential for industrial scale manufacturing of nanowire solar cells.

*Nanowire growth of single crystal Si pillars is readily achieved on crystalline substrates. To achieve low cost and large scale manufacturing similar to thin film approaches for commercial viability it would be a great advantage to grow the nanowires directly onto flexible substrates. Our approach will assess the viability of low cost, direct growth methods of achieving high efficiency PV cells on flexible substrates.*

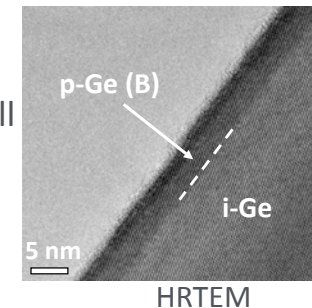
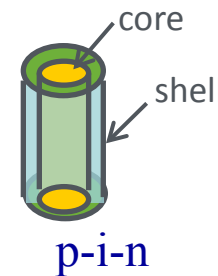
- Industrial Partner: Sharp Laboratories of America  
David Evans, Program Manager;  
Paul Schuele, Principal Integration Engineer
- Contractual Relationship
  - Subcontract issued to SLA (May, 2010)
  - CRADA established with SLA (May, 2010)

## Objective

1. Form dense silicon nanowire arrays by combined top-down and bottom-up growth to study optical interactions and recombination lifetimes



Top-down ordered array of nanowires



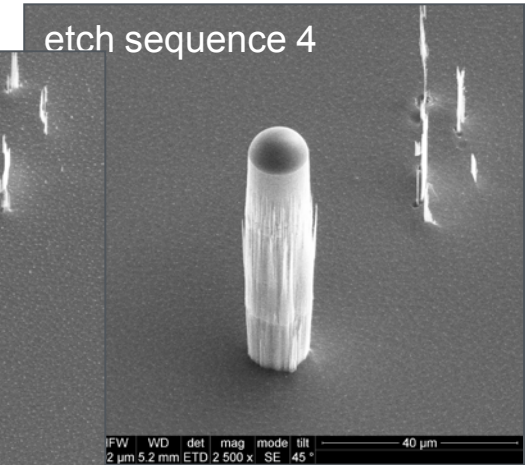
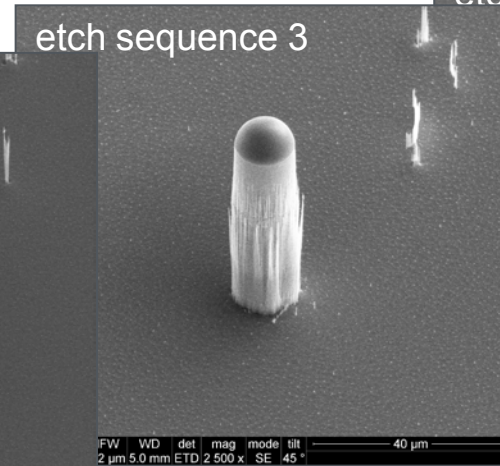
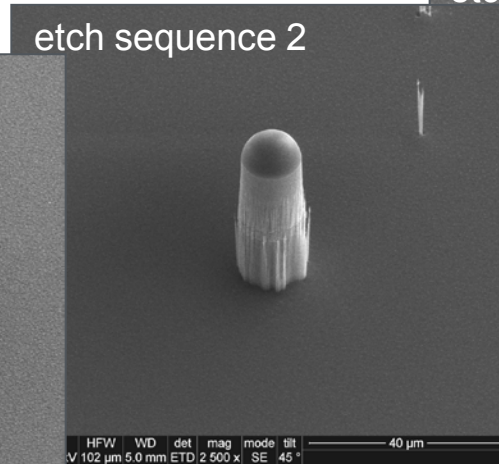
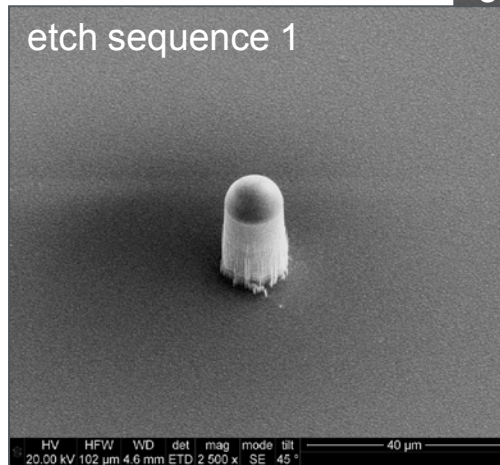
Radial doped processing (core-shell)

# Accomplishments / Progress

## 1. High aspect-ratio fabrication

**Goal:** To develop a top-down approach using a deep reactive ion etch (DRIE) to fabricate tall (10 - 100  $\mu\text{m}$ ) microwires using a non-metal etch mask.

**Approach:** Use Bosch etch chemistry



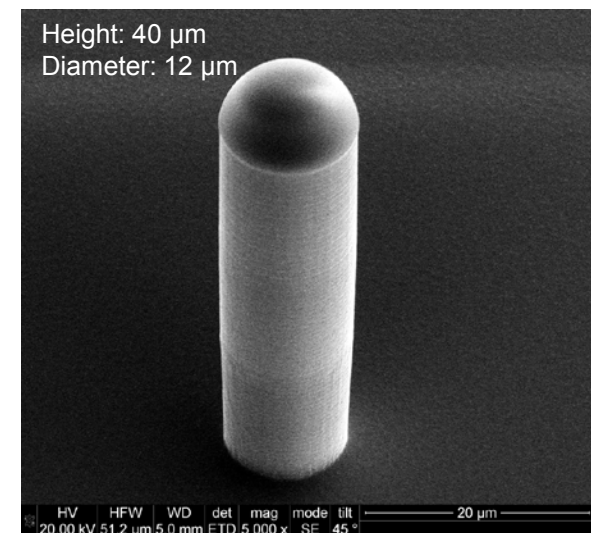
### Initial Results:

- Etch heights of  $>75 \mu\text{m}$  have been reached.
- Excessive sidewall roughness clearly visible with *splintered* nanowire structures protruding from sidewalls.

### Latest Results:

- Maintain nearly-straight sidewall profiles with minimal surface roughness by developing a dynamic etch process (etch parameters are modified throughout the process).

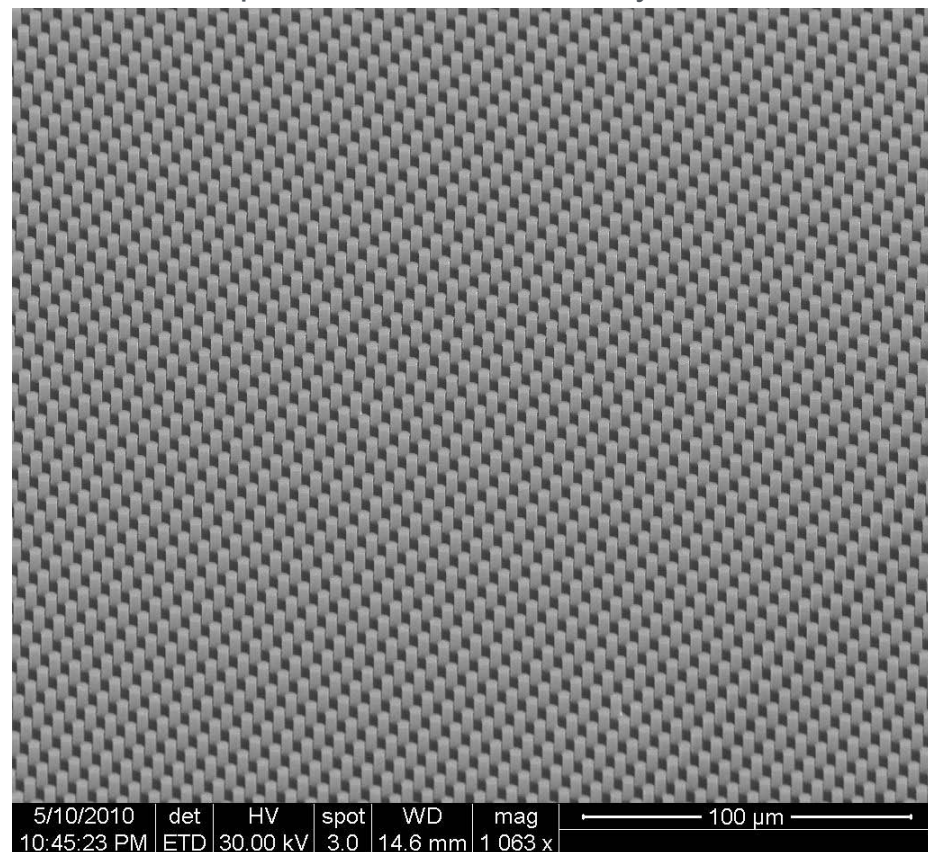
## Smooth Si pillar fabrication



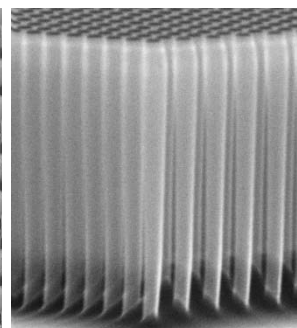
# Accomplishments / Progress

## 1. High aspect-ratio nanowire arrays

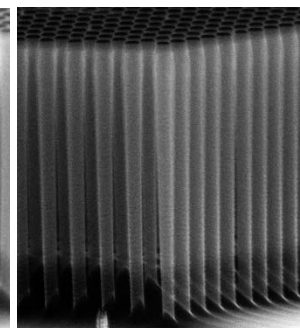
SEM image of large area, top-down, dry-etched perfect Si nanowire array



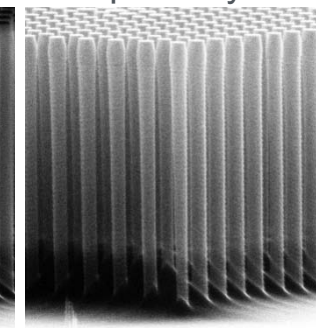
As etched



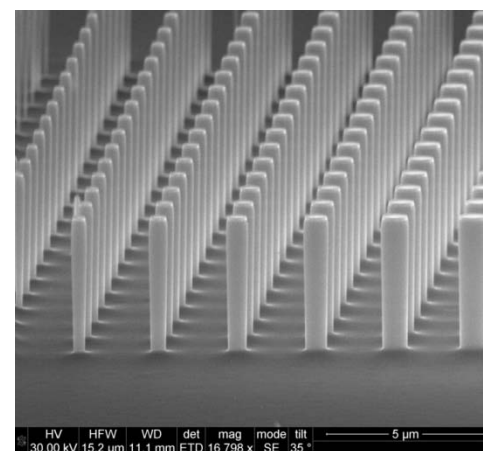
Polymer free



Metal free / epi-ready



Easy access to different aspect ratios: <1 up to 30.



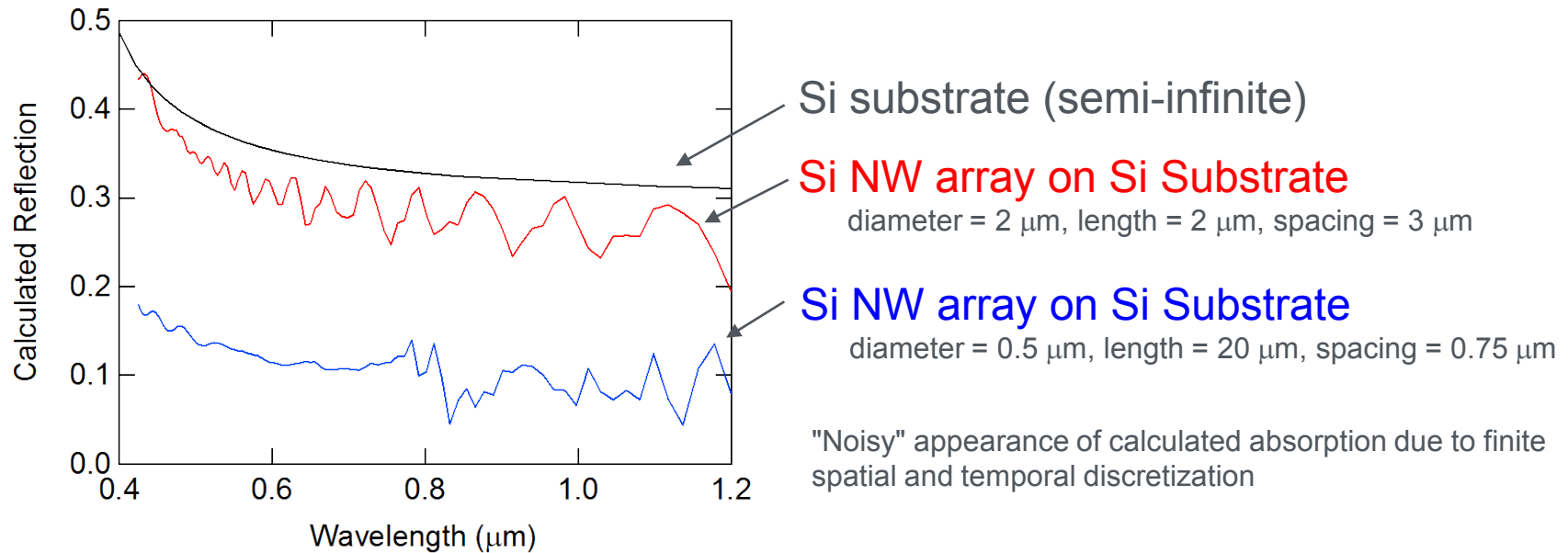
***Si pillar arrays for p-i-n growth demonstrated***

# Accomplishments / Progress

## 1. Nanowire array optical properties

- **Calculate optical properties of Si NW arrays**

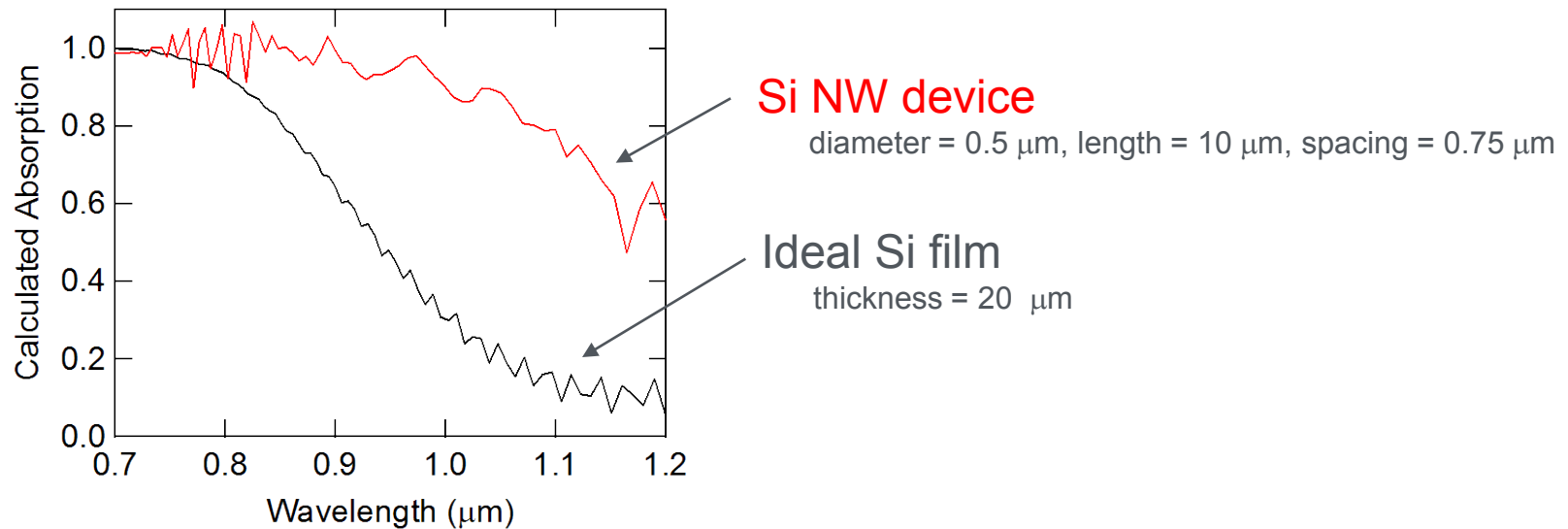
- Calculate optical properties using Finite Difference Time Domain methods (Lumerical Solutions, Inc.)
- Computational technique describes multiple scattering important in NW arrays



***Si arrays dramatically reduce reflection compared to bare Si substrate***

- Low reflection is critical for efficient solar cells

- Calculate ideal optical performance of Si NW devices
  - device geometry assumes Si NWs grown on metal substrate

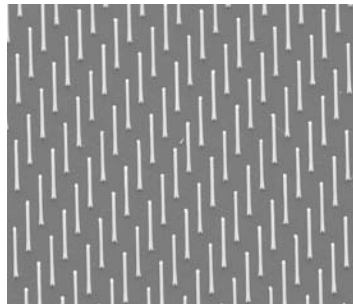


***Si NW devices have dramatically increased absorption at long wavelength***

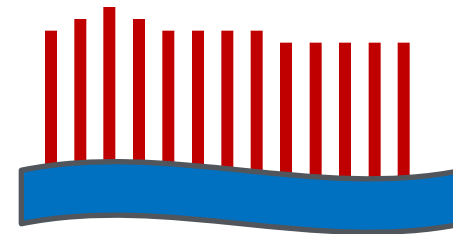
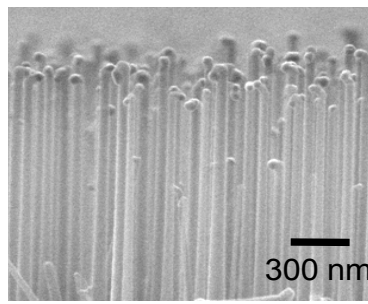
- This is critical for Si, ~50% of useable (above  $E_g$ ) solar photons are at wavelengths  $> 0.7 \mu\text{m}$

## Objectives

2. Synthesize bottom-up silicon nanowires on low-cost flexible substrates and establish limitations



Ge and Si nanowires on (111)  
crystal substrates

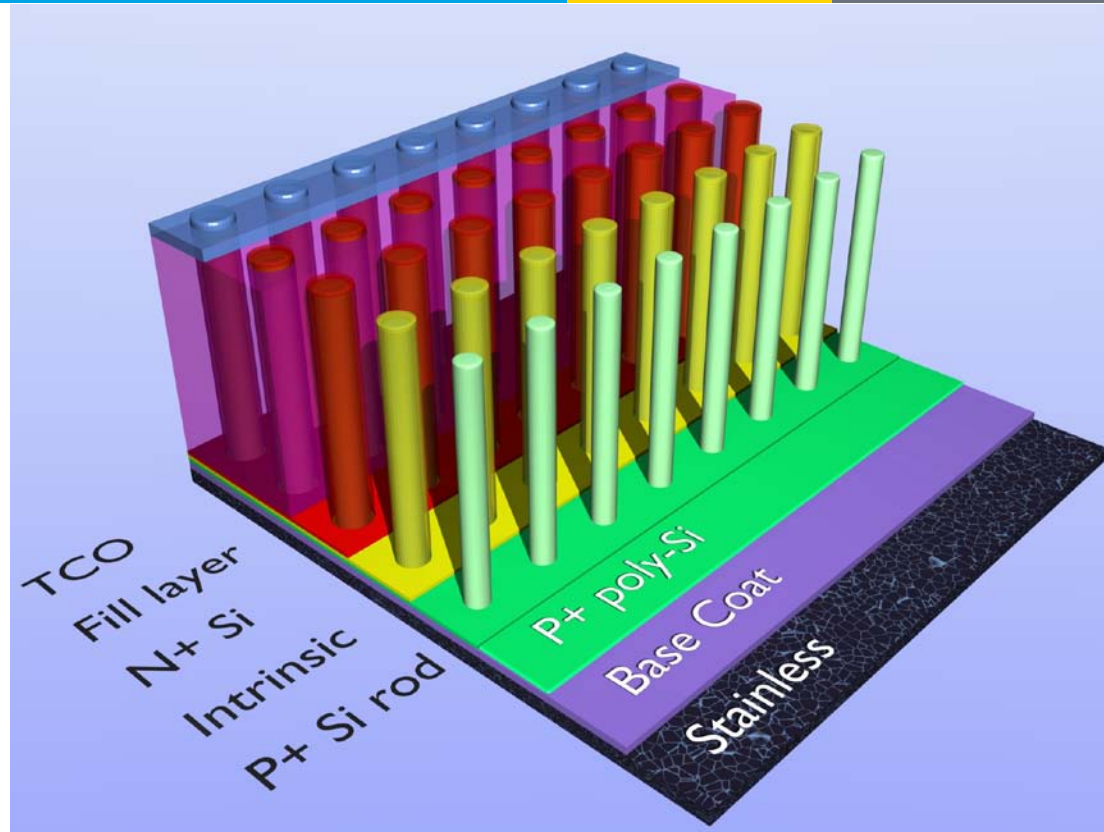


Flexible stainless steel substrate

3. Fabricate and test solar cell prototypes

# Accomplishments / Progress

## 2. Substrate Requirements



- Withstand the temperature of Si nanowire growth  $> 600^{\circ}\text{C}$
- Polished surface with roughness better than 100 nm
- Oxide base coat to prevent diffusion of metals from substrate to cell
- Heavily doped p-type silicon backside electrode
- Scalable to manufacturing using roll-to-roll process tools

- **Low cost 304 stainless steel substrates for Si nanowire photovoltaic fabrication**
  - 500 um thick 150mm diameter wafers: Substrates are rigid and highly polished to minimize handling and surface roughness problems. Basic process development can take place without the effects of substrate distortion and surface roughness. Compatible with prototype fabrication tools at SLA and LANL
  - 125 um thick 100 mm diameter foils: Substrates are flexible with a more roughness so they are handled on carriers
  - The ultimate production target would be a foil about 25 um thick for roll-to-roll processing.
- **The initial substrate preparation process is based on LCD display experience.**
  - Stainless steel foil is cleaned to remove polishing residue.
  - Low temperature PECVD TEOS films deposited on both sides to prevent warping and out-diffusion of metals.
  - The active contact and nanowire growth initiation layer will be heavily boron doped low temperature PECVD poly-Si.
  - Poly-Si grain structure tuned by deposition temperature, anneals or laser crystallization to optimize wire growth.

***Substrate design for Si NW growth is established***

## FY10

- Fabricate NW arrays for optical measurements and compare to calculated designs
- Establish process for radial p-i-n epitaxial layer synthesis for PV cells
- Prepare stainless steel substrates for NW growth

## FY11

- Optimize NW array geometry for PV cells
- Calculate and measure PV response of single NW devices and compare to arrays
- Fabricate NW arrays for PV cells on flexible substrates and measure response
- Design and simulate optimized solar cell based on material and device results

## FY12

- Fabricate and measure optimized PV cell performance
- Assess ultimate commercial viability of NW solar cell approach

- Top-down Si pillar arrays will allow assessment of nanowire PV concept for high efficiency solar cells.
  - Smooth, large area pillar array fabrication process established.
  - Optical design of high aspect ratio pillar arrays to dramatically reduce reflection and increase absorption at long wavelengths being developed.
- Bottom-up growth of Si nanowire arrays on flexible substrates will allow assessment of viability for low-cost manufacturing.
  - Design requirements for flexible stainless steel substrates developed