U.S. Department of Energy
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Polycrystalline CdTe and CIGS Thin-Film PV Research

R. Noufi
X. Wu
T. Gessert
J. Zhou
C. DeHart
T. Coutts
D. Albin
M. Contreras
X. Li
R. Dhere
R. Bhattacharya
B. Egaas
K. Ramanathan
J. Keane
M&C Division

DOE Solar Energy Technologies Program Peer Review

Denver, Colorado • April 17-19, 2007

DOE Contract
DE-AC36-99-GO10337

Purpose

This project leads the development of thin-film CIGS, CdTe, and related materials for use in high-performance stable single-junction solar cells, to

- Support near-term transition to first-time manufacturing
- Build a knowledge-/ technology-/ work force-base for future manufacturing improvements
- Sustain innovation for long-term SETP goals
- Foster and implement collaboration/partnership in the Thin Film PV community.

Approach

1. Improved device structure and material quality for higher performance
2. Contribution toward low-cost fabrication processes
3. Address intrinsic device-stability concerns
4. Technology transfer/working with industry:
   Assist with manufacturing issues encountered by manufacturing entities

Focus Activities

(June 05 – Jan 07)

- Engineering Specifications and Conceptual Design for a CIGS Research Platform. *Purpose: Contributes to manufacturing improvements to narrow the gap in performance between laboratory devices and modules.*
- Improving material qualities and process repeatability of the thin-film layers in the device: glass/Mo/$CuIn_{1-x}Ga_xS$/CdS/ZnO on glass and metal substrates from NREL and industry
- Developing alternative window layers to CdS, such as ZnS, CdZnS, and In_2S_3
- Reducing CIGS and CdTe absorber thickness
- Developing novel/improved materials for CdTe-based device
- Simplifying fabrication processes toward lowering costs
- Developing a manufacturable, stable back-contact for CdTe
- Examining devices under stress to understand degradation mechanisms

Budget

CdTe Research	$1.6M
CIGS Research	$1.31M
TCOs	$0.29M
Total	**$3.2M**

Manpower: October–April 06 11 FTEs

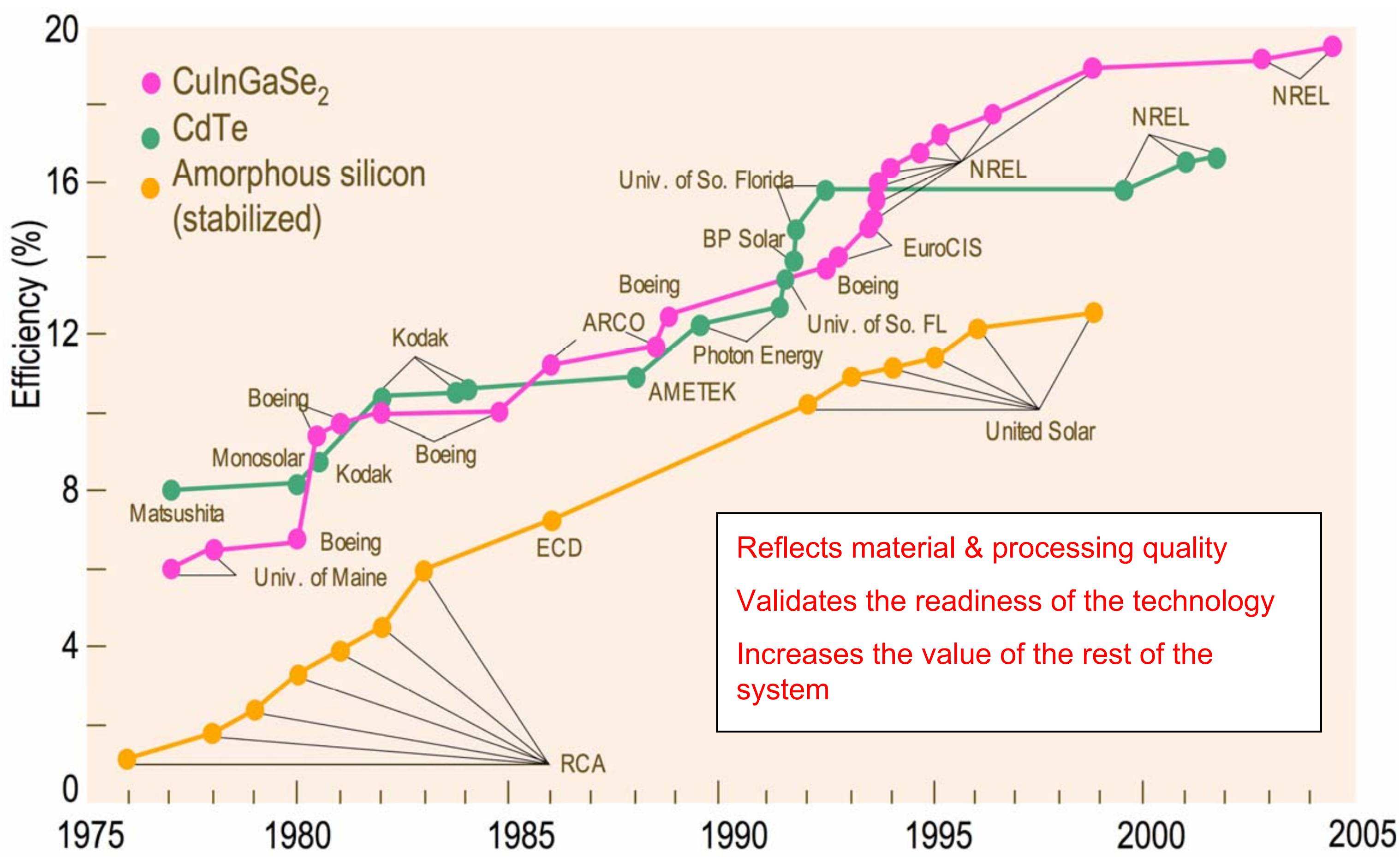
May 06–January 07 9 FTEs (1 scientist and 1 technician joined industry)

Participants: Thin-Film group, Scientists from the Measurement and Characterization Division, Industry, CIS and CdTe National Teams, Graduate Students (Colorado School of Mines)

Results/Accomplishments

Laboratory Cell Efficiencies for Thin Films

Efficiency is the Best Metric to Gauge Progress



- Reflects material & processing quality
- Validates the readiness of the technology
- Increases the value of the rest of the system

LABORATORY MOVE: Sept. 06 to Jan. 07

Moving the laboratory from the SERF to S&TF

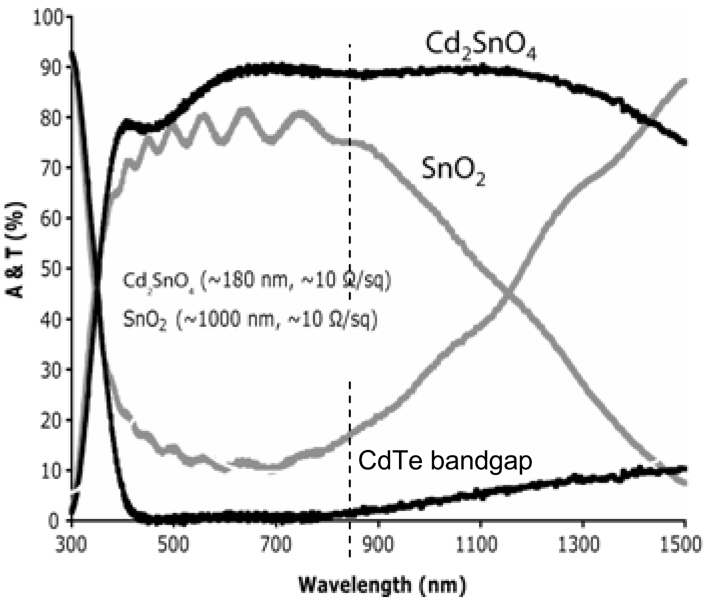
Hook-up; Equipment start-up; Returning to base-line status

Modification/improvement to capabilities

CdTe

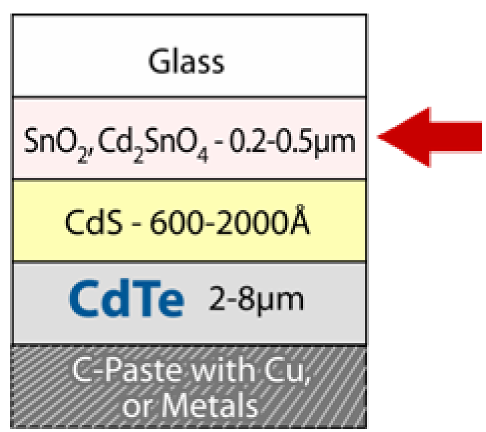
Improved/Novel Buffers and Windows

(Compared to SnO_2)



Sample	Cd_2SnO_4	SnO_2 ($SnCl_4$)	SnO_2 (TMT)
t (nm)	510	~1000	~1000
n (cm^{-3})	8.94×10^{20}	4.95×10^{20}	4.52×10^{20}
μ (cm^2/V-S)	54.5	15.4	42.-0
Resistivity (Ω cm)	1.28×10^{-4}	8.18×10^{-4}	3.29×10^{-4}
R_s (Ω/sq)	2.6	8.6	3.3

High-Quality TCO: Cd_2SnO_4(CTO)



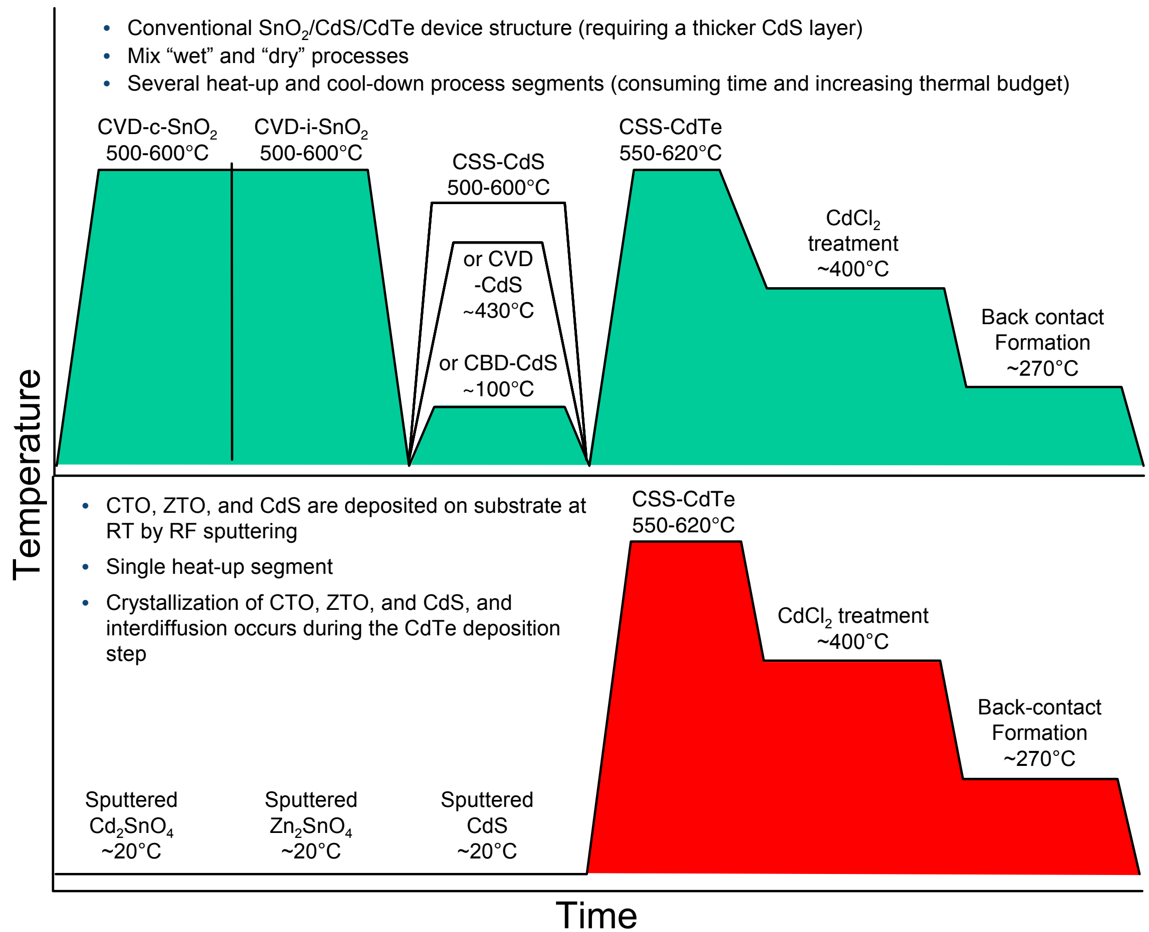
Improved performance

High-Efficiency $Cd_2SnO_4/Zn_2SnO_4/CdS/CdTe$ Cells

CdTe Thickness = 8 µm

Cell #	V_{oc} (mV)	J_{sc} (mA/cm^2)	FF (%)	η (%)	Area (cm^2)
W547-A	847.5	25.86	74.45	16.4	1.131
W553-A	849.9	25.50	74.07	16.1	1.029
W566-A	842.7	25.24	76.04	16.2	1.116
W567-A	845.0	25.88	75.51	16.5	1.032
W597-B	835.6	25.25	76.52	16.1	0.961
W608-B	846.3	25.43	74.24	16.0	1.130
W614-B	842.2	25.65	74.67	16.1	0.948

Simplified CdTe Deposition Process

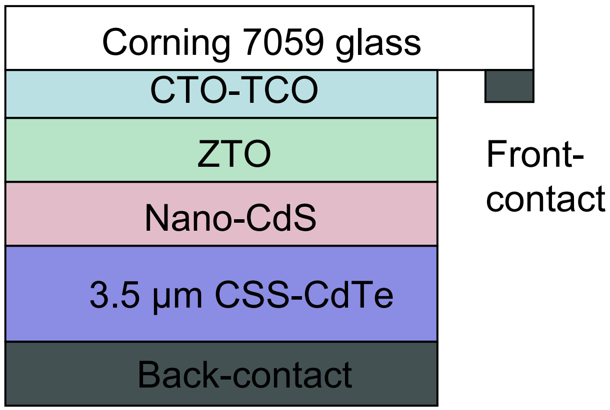


Efficiency = 15%

Improved processing

Reduced CdTe Thickness from 8 μm to 3.5 μm

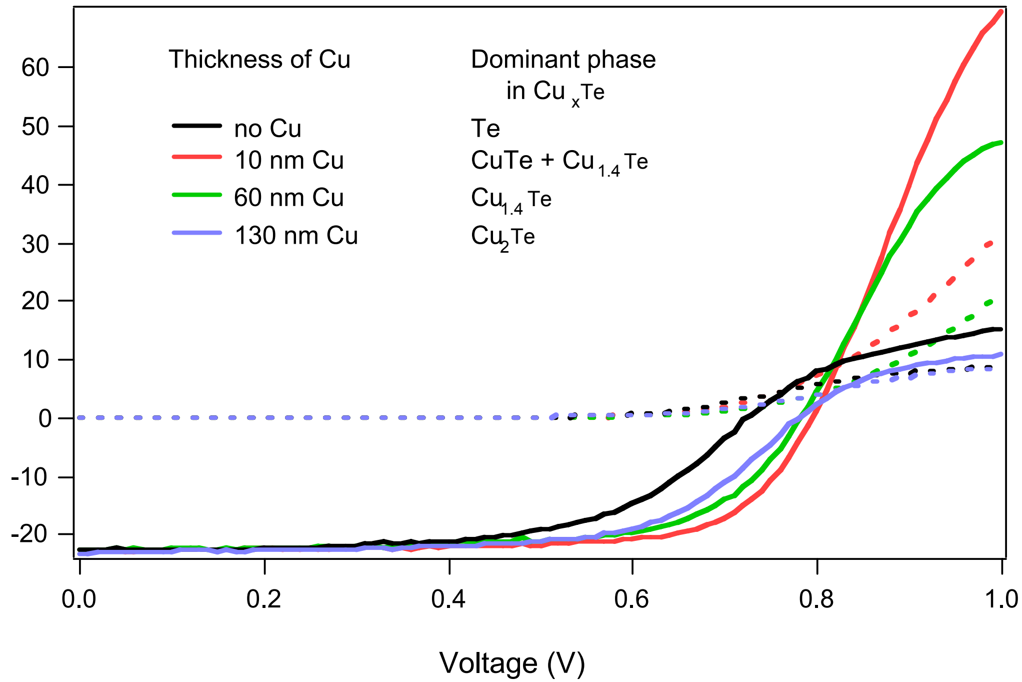
15%-efficient 3.5 μm CSS CdTe solar cell



Improved processing

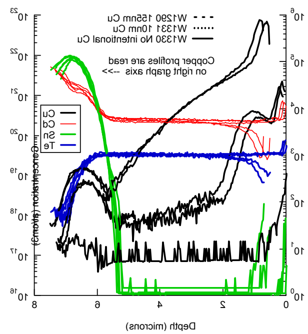
- The limited availability of Te may affect large-scale CdTe manufacturing.
- It is important to investigate how to reduce CdTe thickness without impacting CdTe cell performance.
- We developed the techniques to prepare high-efficiency thin CdTe solar cell by close-spaced sublimation with a high deposition rate.
- We achieved a 3.5-μm-thick CdTe cell with an NREL-confirmed total-area efficiency of 15.02% (V_{oc} = 829 mV, J_{sc} = 24.13 mA/cm^2, fill factor = 75%).

Phase Control of Cu_xTe in the Back-contact of CdTe Device

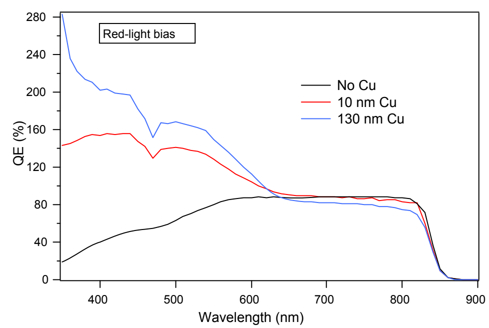


- Cu_xTe has been widely used as a back-contact in CdTe cells.
- Phase x in Cu_xTe significantly affects device performance. Although Cu_2Te has the highest conductivity, it is unstable and not beneficial to CdTe device performance. IV curves show more roll-over and voltage-dependent collection for the cell with Cu_2Te back-contact.
- Phase x control: (1) Cu/Te ratio, and (2) post-annealing temperature.

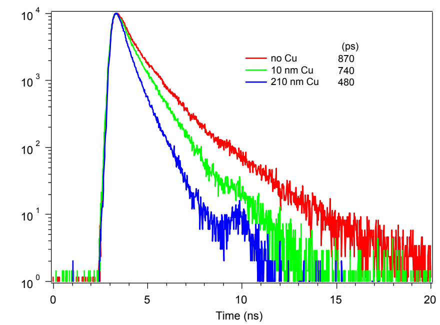
Investigating the Role of Cu in CdTe Cells



SIMS

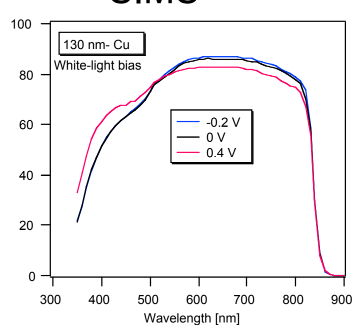


Apparent QE

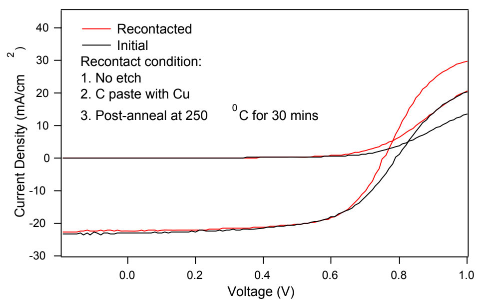


TRPL

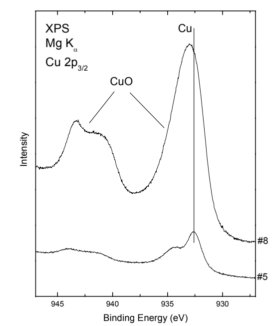
Improved performance and reliability



QE under Voltage Bias



Re-contacting



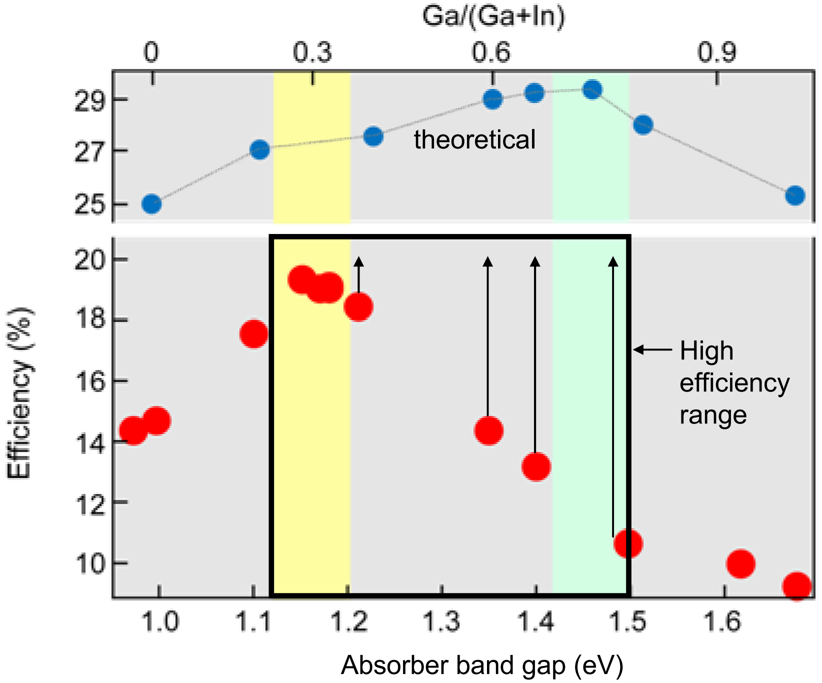
XPS

- Cu diffusion into the CdS causes “cross-over” due to photoconductivity of CdS:Cu.
- Cu diffusion into the CdTe film creates Cu-related defects, which lower photogenerated carrier lifetime and results in voltage-dependent collection.
- “Re-contacting” and other analysis results (such as XPS, XRD, SIMS, TEM/EDS) indicate that the mechanism responsible for the “roll-over” is Cu-related oxides, rather than losing Cu from the back-contact.

CIGS

Efficiency vs. E_g

- Reflects best materials and process properties
- Needs further understanding of limitation at high Ga
  - Understand the performance limiting mechanisms
  - Bulk vs. interface recombination
  - Grainboundaries contribution
  - Phase inhomogeneity



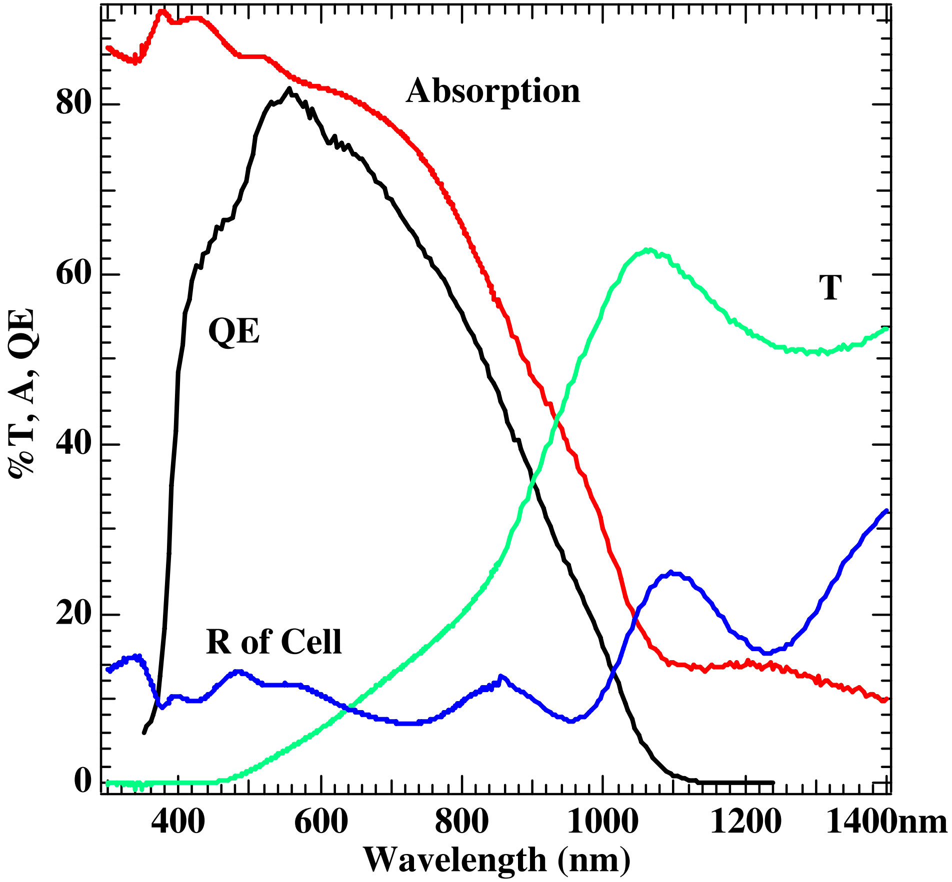
Robust processing improved performance

Minimize the Thickness of CIGS while Maintain High-efficiency and Stability toward Lower Cost

t (μm)	V_{oc} (V)	J_{sc} (mA/cm^2)	FF (%)	Eff (%)
1.0 CIGS	0.676	31.96	79.47	17.16 NREL
0.75 CIGS	0.652	26.0	74.0	12.5
0.40 CIGS	0.565	21.3	75.7	9.1
0.47 CIGS	0.576	26.8	64.2	9.9 EPV

Performance Limited by Absorption of Thin CIGS

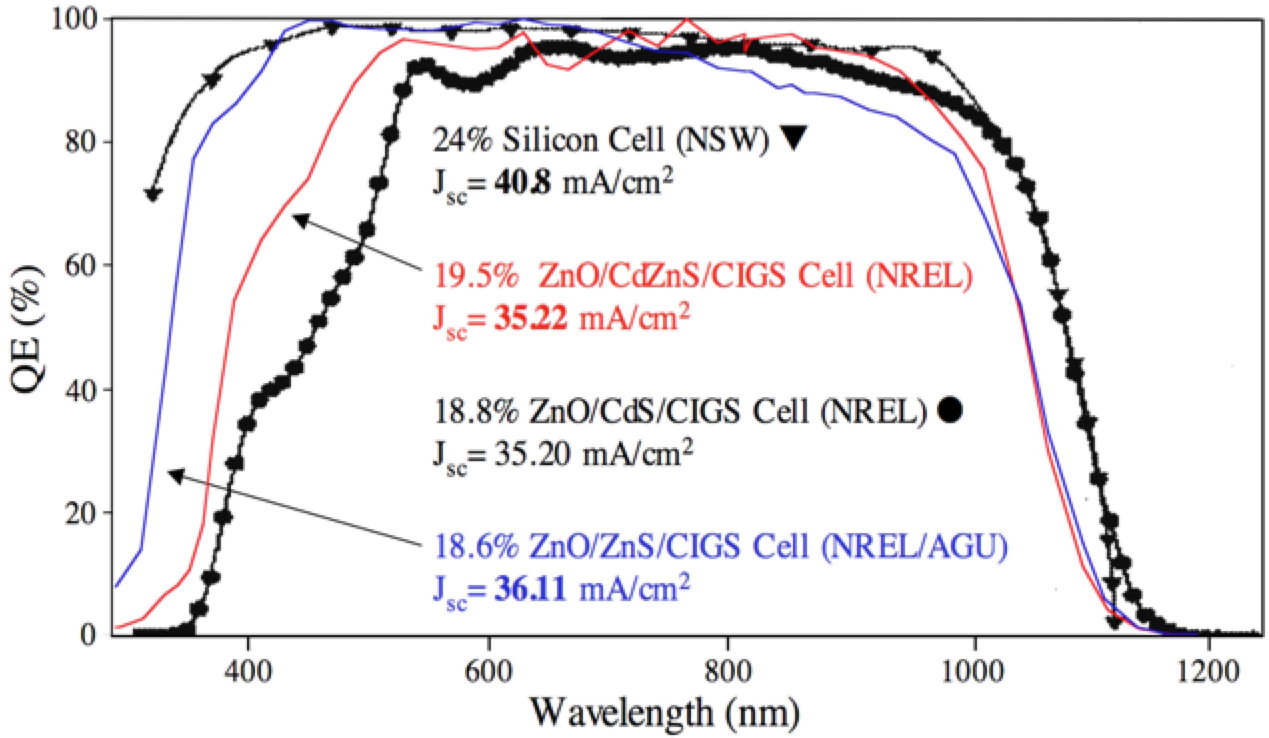
0.4 µm Cell - Optical



Development of Alternative Buffer Layers
ZnO/CdS/Cu(In,Ga)Se_2 Solar Cells

Improvements to current generation (*short term*)
- Current generation is limited by window materials, i.e., CdS
- Develop wider bandgap (alternative) buffer layers to CdS
- (Cd,Zn)S alloys, ZnS, In_xS_y, ZnSe, Cd^+ PE, others

Quantum Efficiency of CIGS Solar Cells using CdS, CdZnS, and ZnS Buffer Layers



Improved performance

CIGS R&D Platform

Type: New – Process Integration Development and Industry Support

Purpose/Application to Industry:

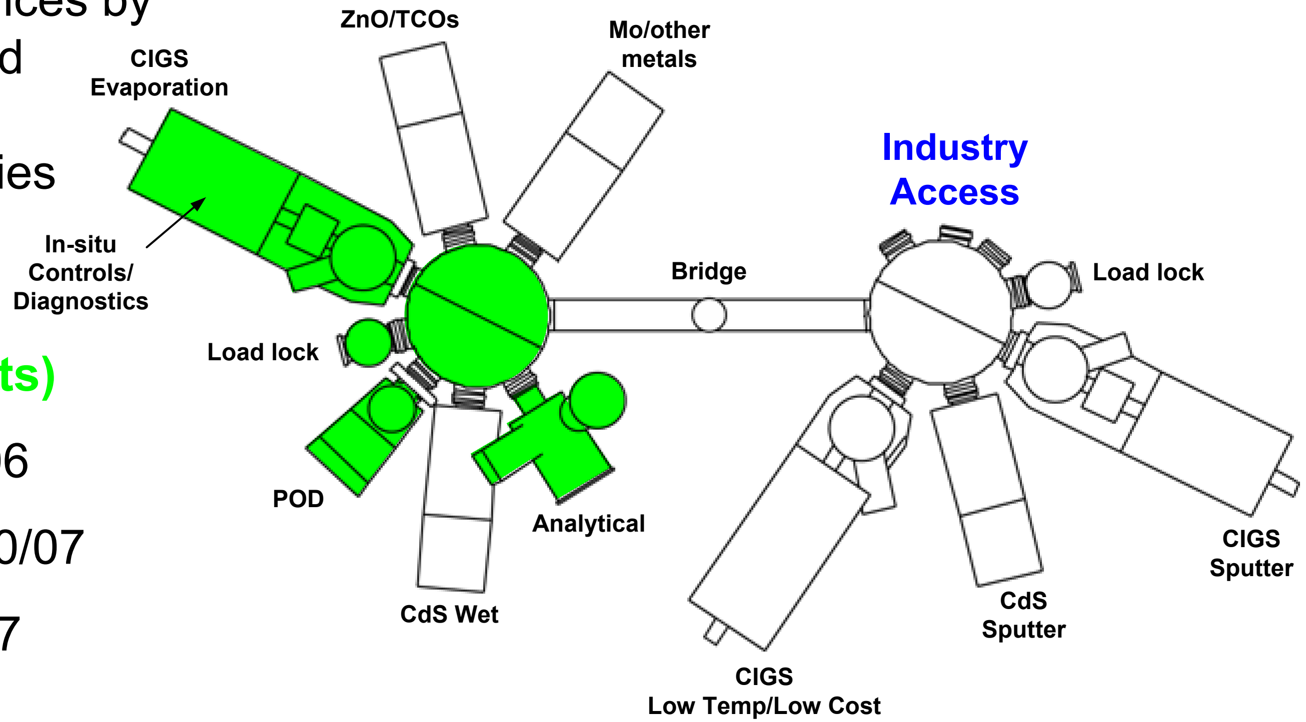
Narrow the performance gaps between laboratory and commercial devices by providing flexible and controllable device "prototype" capabilities

Timeline:
(phase 1 green shaded components)

Vendor chosen 10/06

Expected delivery 10/07

Start operation 11/07



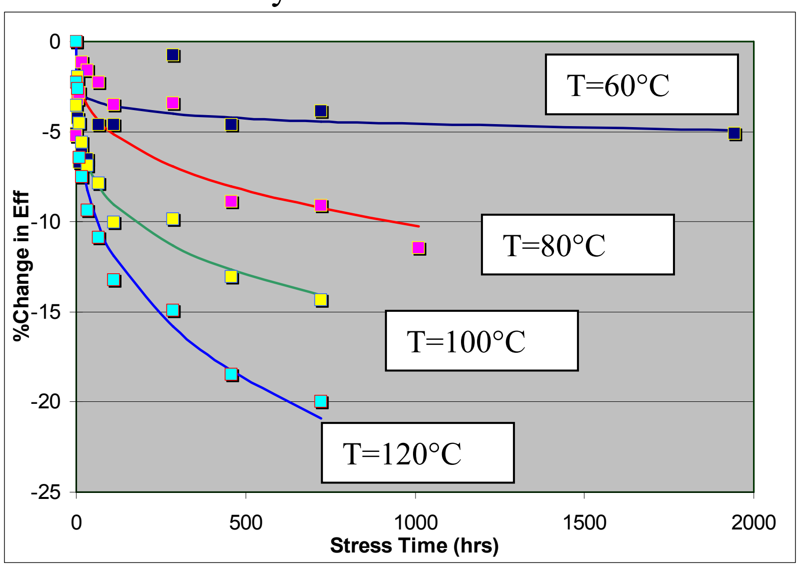
Device Stability

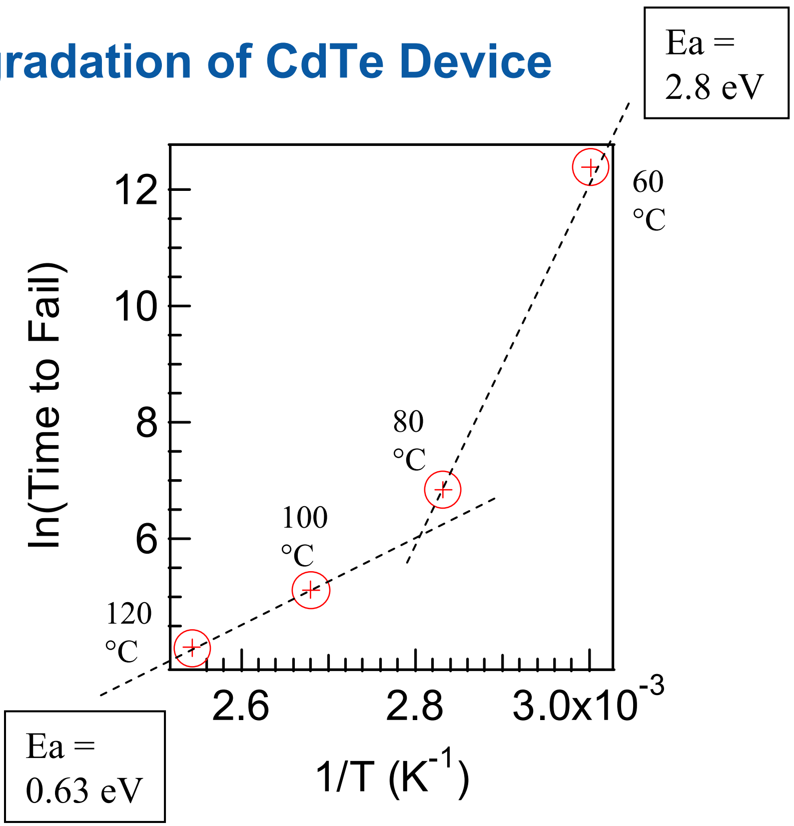
Study Intrinsic Device Stability

Temperature-Dependent Degradation of CdTe Device

Different mechanisms dominate degradation at different temperatures (~90–120°C associated with Cu diffusion)

Stress Data Fit: y = b · x a





Cu diffusivity in CdTe:

$$D = 3.7 \times 10^{-4} \exp(-0.67\ eV/kT)$$

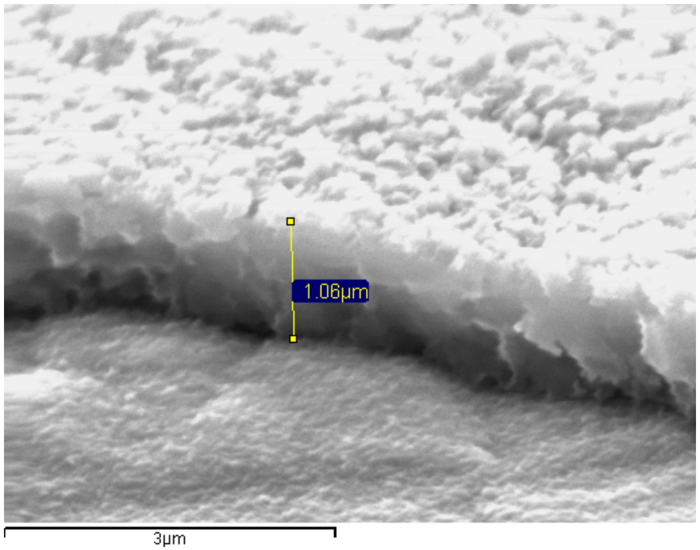
Reliability protocol

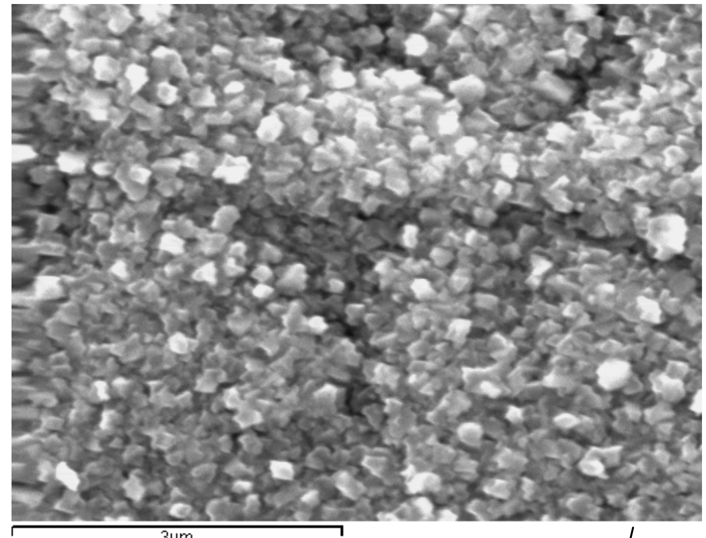
Industry Support

Collaboration with Industry/Technology Transfer

Shell Solar	Windows/Junction
Global Solar Energy	Problem-solving (license)
NanoSolar	Materials (bench marking)
DayStar	Tech transfer, work force
Miasole	Tech transfer (extensive)
HelioVolt	Assist in tech start-up (using NREL facilities)
Solyndra	Tech transfer to new start-up
First Solar	Assist On-site
PrimeStar	Tech transfer to new start-up
Applied Materials	Explore viability of new deposition methods
IBM, VeeCo, others	Interaction RE thin-film PV interest

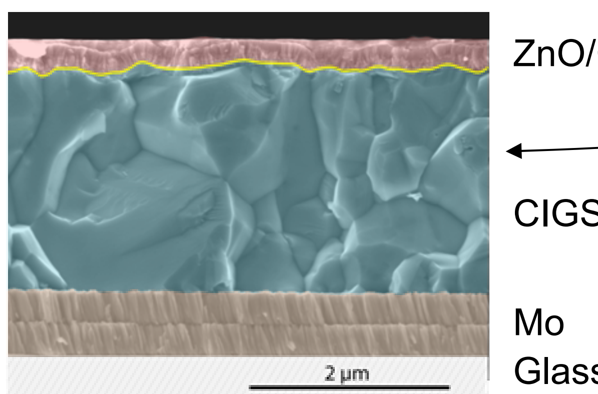
Sample Film from Industry





"Complete make-over"

High-quality material, NREL



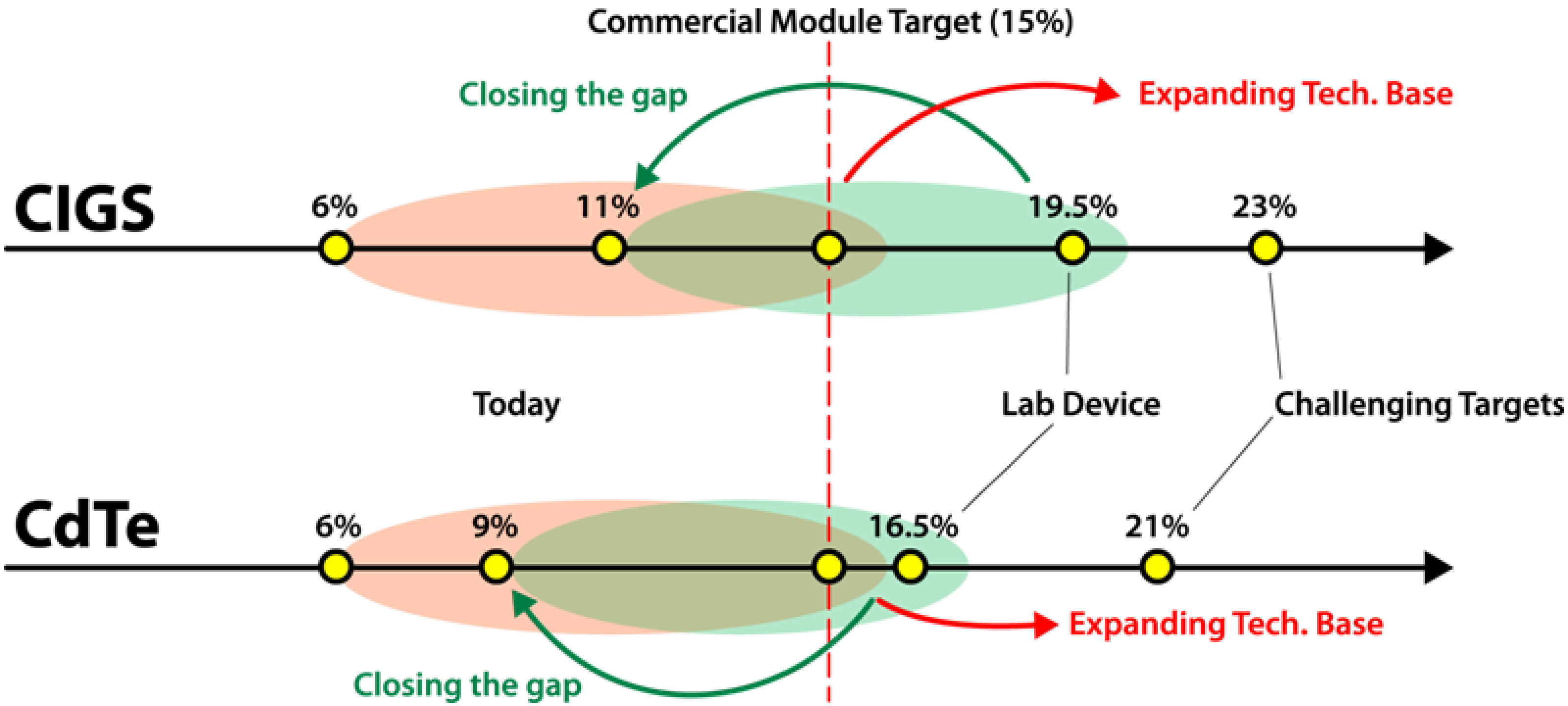
Key FY06 Milestones

	Milestone	Status	Due Date
1.	Specs and engineering design for the CIGS cluster tool completed	Complete	9/30/06
2.	Demonstrate a 14% efficient thin CdTe cell (2-3 μm)	15%	9/30/06
3.	Demonstrate 17% efficiency for a solar cell using 1 μm thick CIGS film	17.2%	1/30/06
4.	Assessment of the feasibility of a CVD-based CIGS deposition	Complete	9/30/06
5.	Demonstrate high-performing (>18%) alternative buffers and windows	Complete 19%	8/30/06

Challenges Forward

Closing the Gap Between Laboratory Cells and Modules

What is the pathway?



Challenge 1

Adapt NREL’s high-efficiency CIGS and CdTe insights and device processing to close the gap between laboratory cells and modules.

- Formal/informal technology transfer
- Address manufacturing challenges by seeking solutions on NREL’s equipment

Impact: Higher module performance

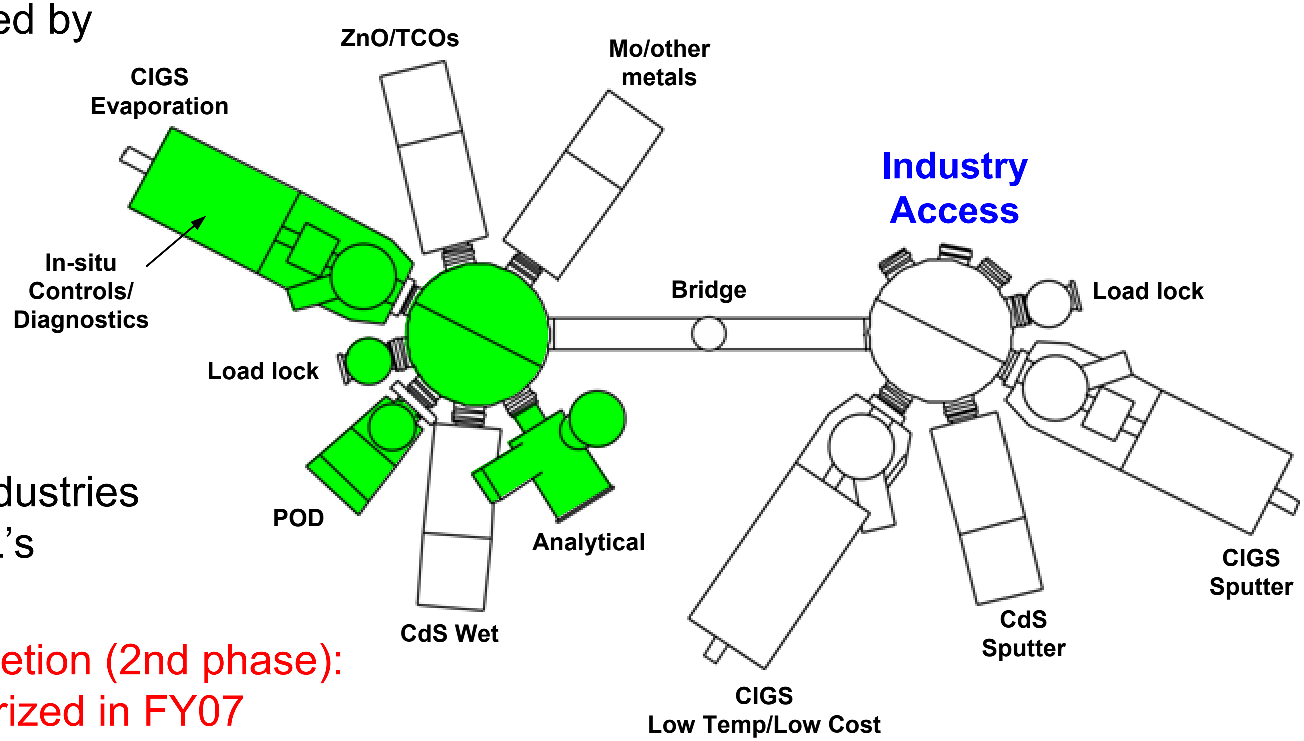
Lower costs of individual layer fabrication

Approach

Completion of CIGS R&D Platform

Construction/development of new state-of-the-art capabilities aimed at contribution to manufacturing improvements.

- Allow integration of processes similar to what is practiced by industry
- Derive measurable material properties that are predictive of device performance
- Couple the knowledge to industrial processes
- Benchmark/Prototype industries processes against NREL's



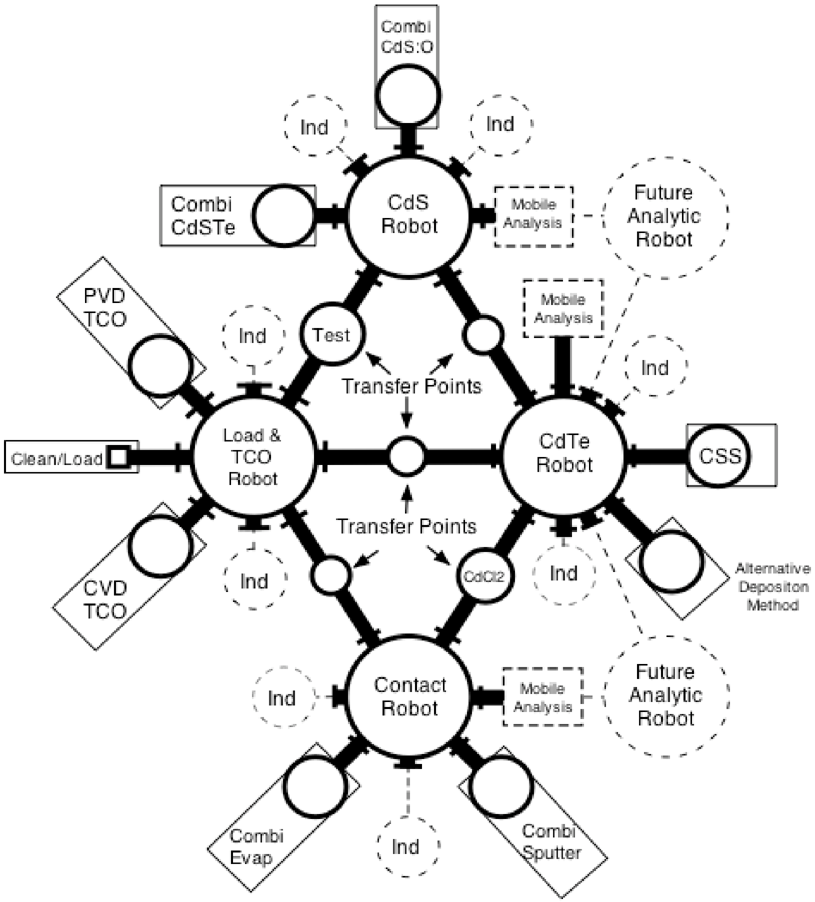
Planned Date for Completion (2nd phase): 01/09 if funds are authorized in FY07

CdTe Research Platform

Construction/development of new state-of-the-art capabilities aimed at contribution to manufacturing improvements.

- Allow integration of processes similar to what is practiced by industry
- Derive measurable material properties that are predictive of device performance
- Couple the knowledge to industrial processes
- Benchmark industries processes against NREL's

Planned Date for Completion (1st phase): 06/09 if funds are authorized in FY07



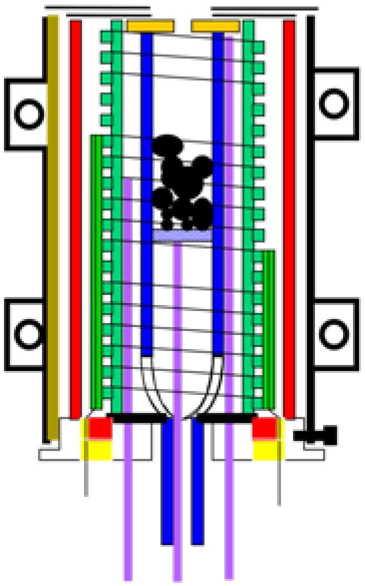
Approach *(cont.)*

CdTe platform

- Multi-source deposition process to improve CdTe material properties and reproducibility

Timeline

- Bench-top prototype for proof of operation, Nov. 07
- Depending on outcome, produce working specifications by Sept. 08
- Cluster tool completion, June 09



Some Reasons for Developing Multi-source Deposition
- Separate source from substrate temperatures
- Control stoichiometry variation
- Allow for alloy/dopant incorporation
- Control material properties as function of film thickness
- Improvements toward industrial processes
- Improve layer reproducibility
- A path for higher performance

Challenge 2

Extend the higher performance range of CIGS to higher Ga content

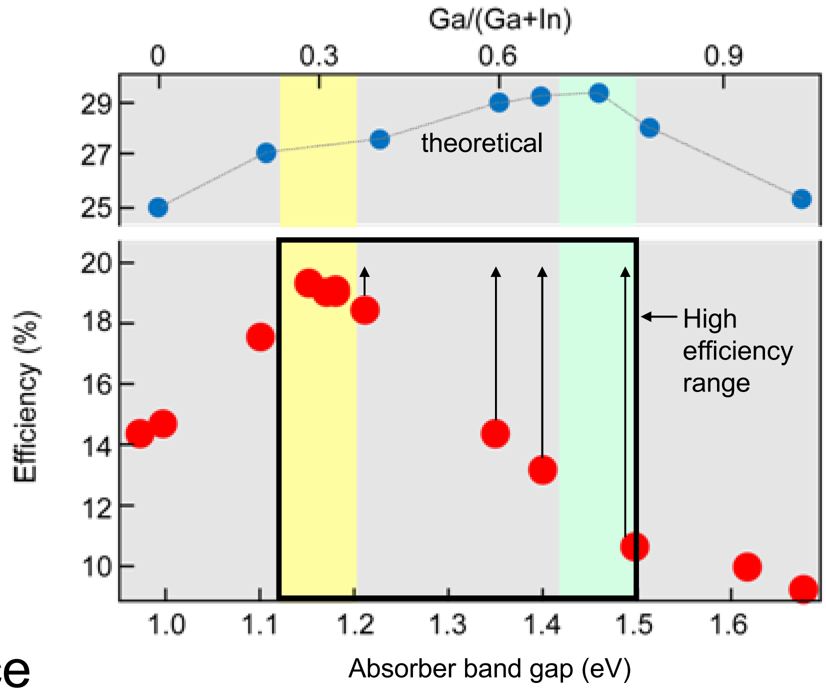
- Understand the performance limiting mechanisms
- Bulk vs. interface recombination
- Grain-boundaries contribution
- Phase inhomogeneity

Duration: Feb. 07 to Sept. 08

Impact: Choice of high-performance cell parameters

More robust deposition process

for manufacturing



Efficiency vs. E_g

Challenge 3

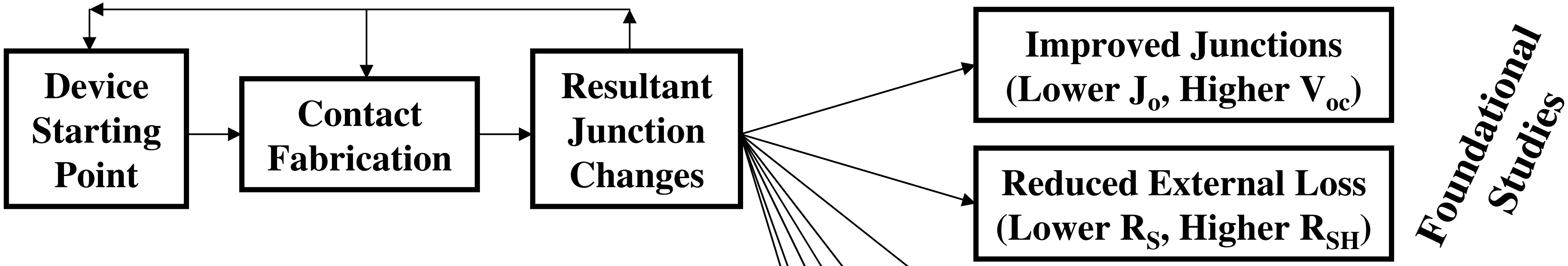
Impact of back-contact on CdTe device performance

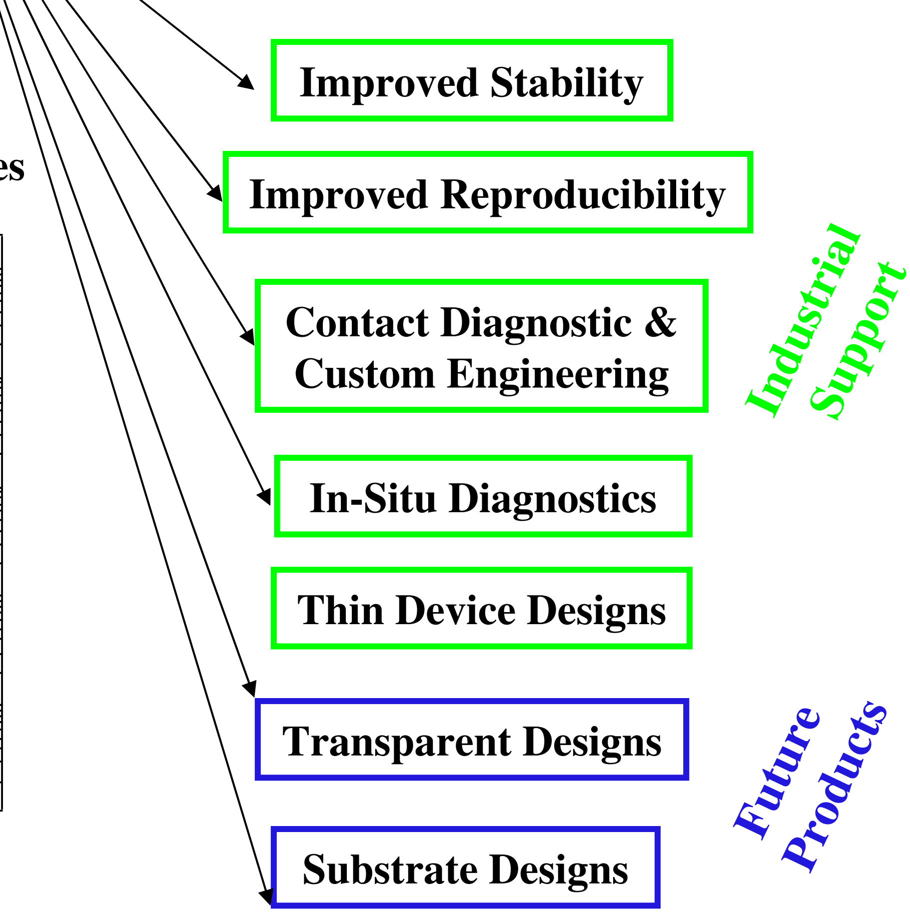
- The Cu-containing back-contact determines how the device operates, i.e., p-i-n or p-n
- To get a handle on the resultant junction, we need to:
  1. Correlate doping level with carrier lifetime
  2. Control the amount of Cu diffusion
  3. Compare devices from various sources (NREL, IEC, industry)

Duration: March 07 to April 08

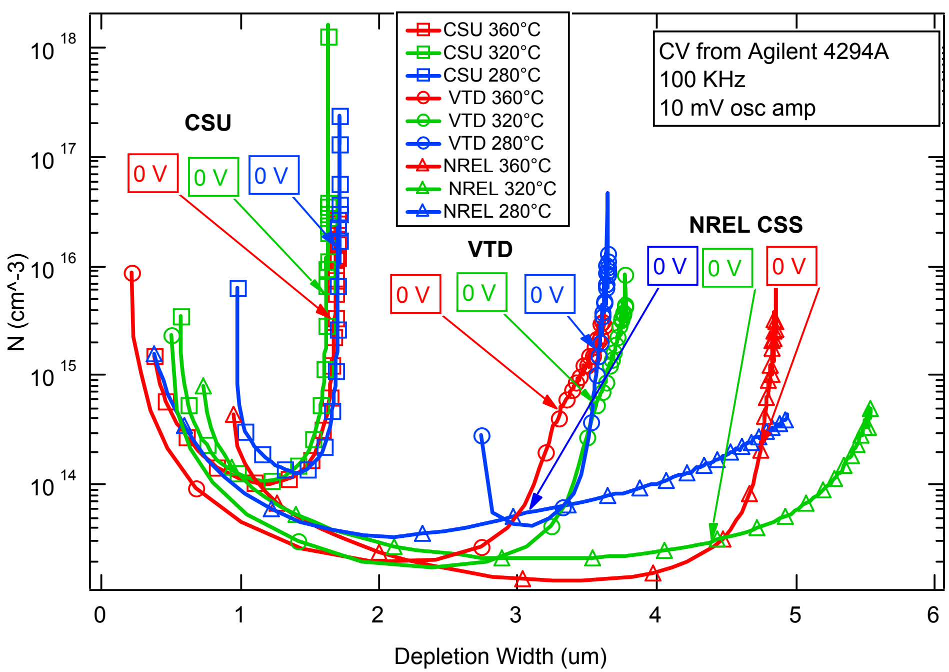
Impact: Increase module performance and reliability

Importance of Studying CdS/CdTe Back Contacts





Comparison of Contact-Induced Depletion Width Changes for Three Different Types of Uncontacted Devices



Tim Gessert
10/06

Challenge 4

Technology transfer/partnership with industry

- Position ourselves to partner with industry through the TPP in a timely manner
- Continue technology transfer to industry not participating in TPP

Key FY2007 Thin-Film Polycrystalline Compounds Milestones

	Milestones	**Planned Completion**
1	Validate readiness of the PDIL CIGS platform by performing an acceptance test at NREL	10/07
2	In collaboration with industry, design a set of experiments to perform in the CIGS platform whose outcome is transferable to industry	09/07
3	Determine minimum absorber thickness for CIGS and CdTe at which precipitous efficiency and stability drops will occur; transfer results to industry	09/07 conclusion of task
4	Correlate doping (with Cu) with lifetime and the effect on operating parameters in the CdTe device	09/07 conclusion of task
5	Construct and test the integrity of the hardware elements in a multi-source CdTe deposiyion system capable of versatile and fast process aimed at high performance and lower cost	09/07

END

Additional Results and Accomplishment Will Not Be Presented at The Review Meeting

Polycrystalline Thin-Film Multi-Junction Solar Cell Research

EMD DIVISION

M&C DIVISION

Objective

Develop approaches toward improving transparent top cells, an appropriate bottom cell, and interconnect, toward a target 25%-efficient polycrystalline thin-film tandem solar cell.

Ultimate goal is monolithic tandem cell

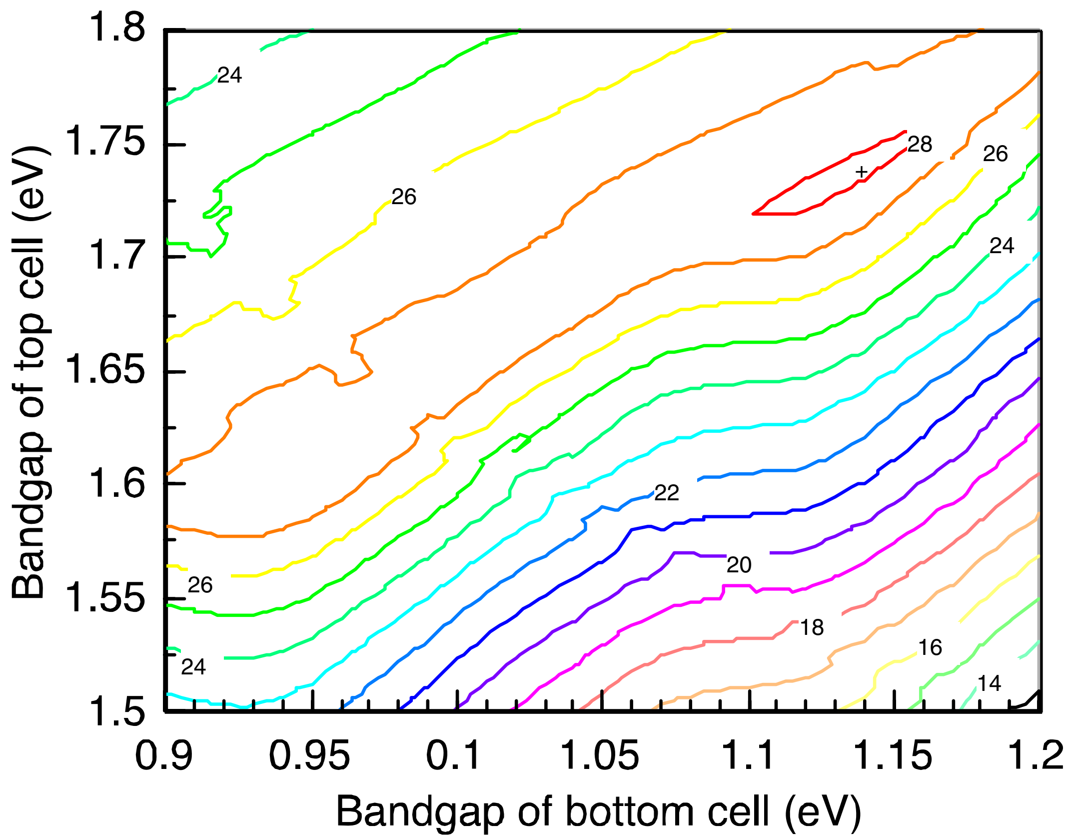
Task Elements

Status of Research:

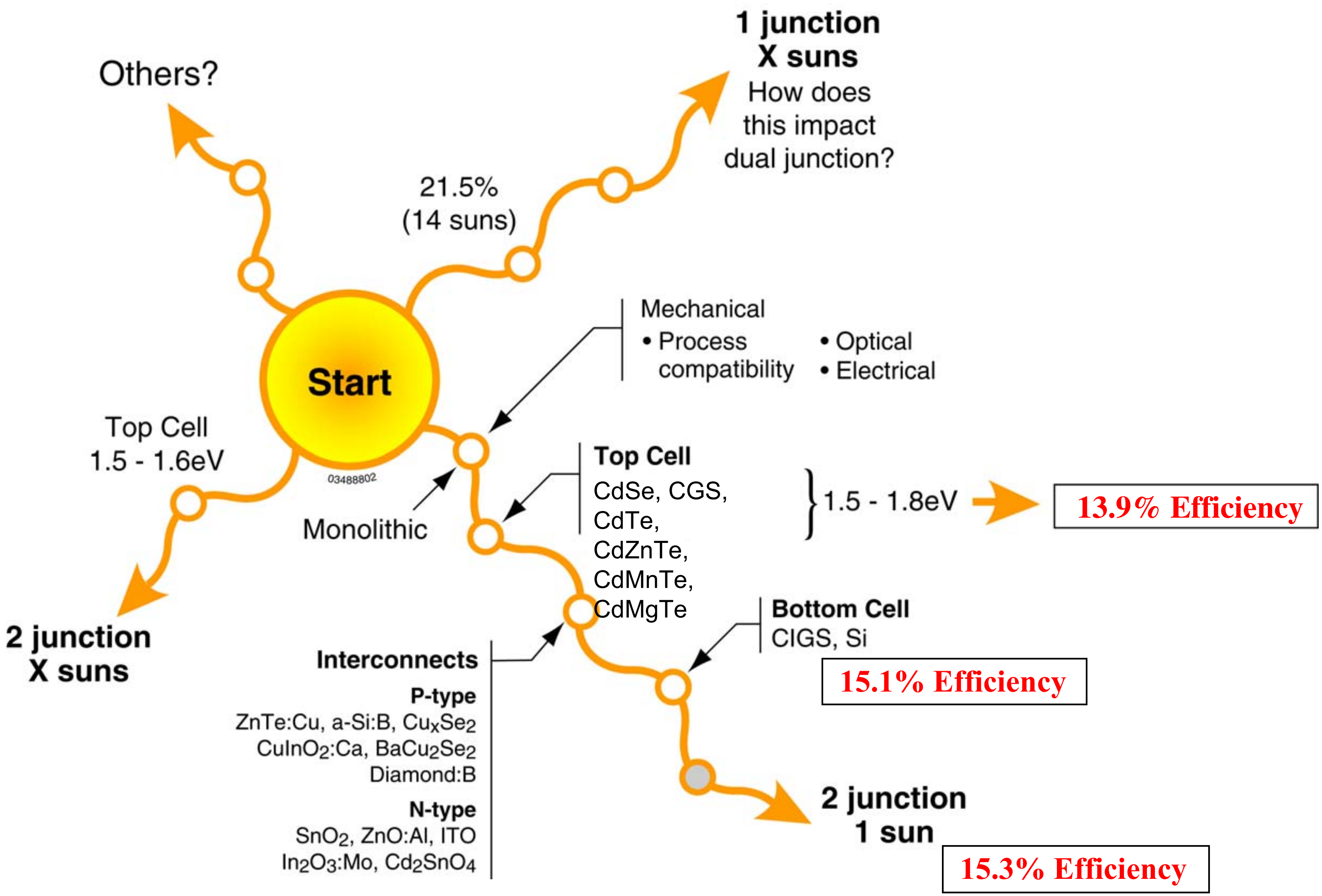
- $CuGaSe_2$ top cell (1.7 eV)
- Transparent CdTe top cell (1.5 eV)
- $CuInSe_2$ bottom cell (1.0 eV)
- Mechanical-stacked tandem (CGS/CIS)
- Mechanical-stacked tandem (CdTe/CIS)
- CGS/c-Si (monolithic tandem)
- CdMgTe new alloy for top cell

Modeled Tandem Efficiency

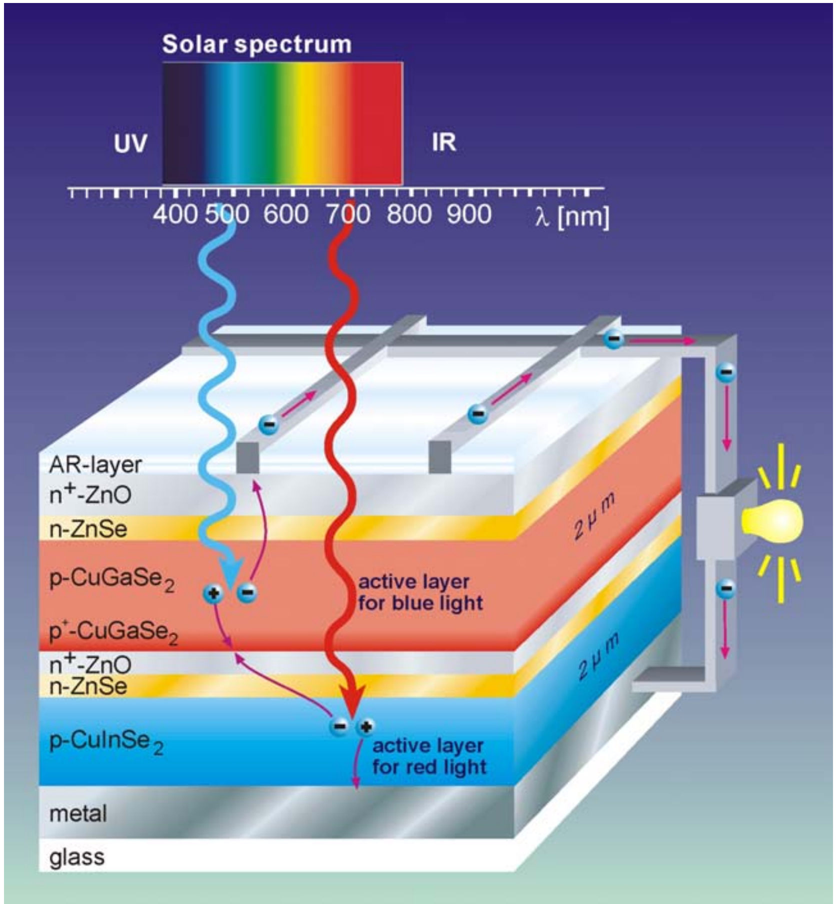
- Assumes all photons reach the top absorber
- Absolute maximum is 28.2%
- If realistic optical properties of TCO layers included, maximum efficiency only ~25%



Exploring and Accelerating Ultimate Pathways



Goal: Monolithic Tandem Cell



Thin-film tandem cell combining low-cost thin-film technology with highest efficiencies

Achieved:

- Bottom cell with $E_G \approx 1.1$ eV and $\eta \approx 20\%$
- Tunnel contact TCO/Cu(InGa)Se_2

To Do:

- Top cell with $E_G \approx 1.7$ eV and $\eta \approx 20\%$ or at least 15%
- Transparency > 70% for $E < E_G$
- Low-temperature process for top cell (T < 200°C)
- or Temperature-stable bottom cell (T > 450°C)
- or New idea

S. Siebentritt, HMI, Berlin

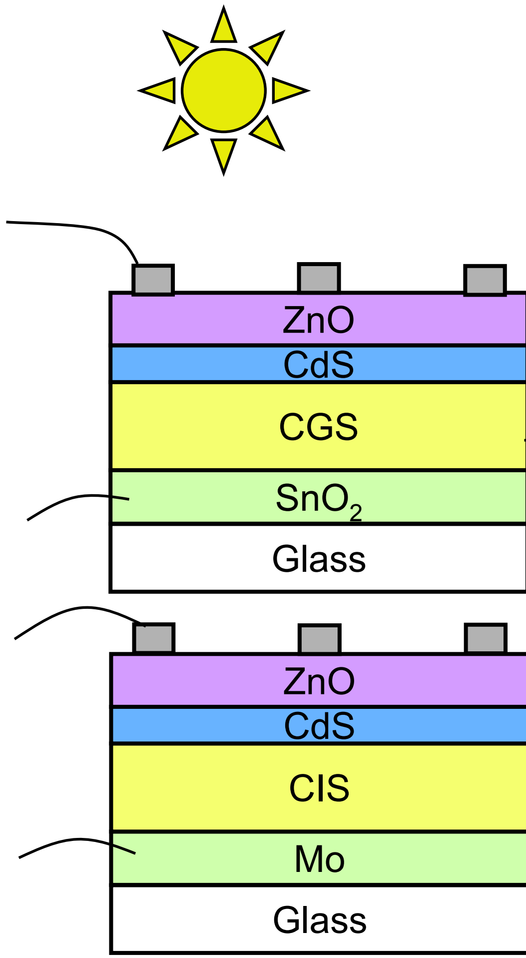
CGS/CIS Tandem

Mechanically stacked, series-connected by addition, CGS/CIS cell

Eff. = 10.7%, V_{OC} = 1.32 V

***NREL official measurement

Eff. = 9.7%, V_{OC} = 1.29 V



Transparent CGS solar cell

Eff. = 6.8%

V_{OC} = 0.864 V

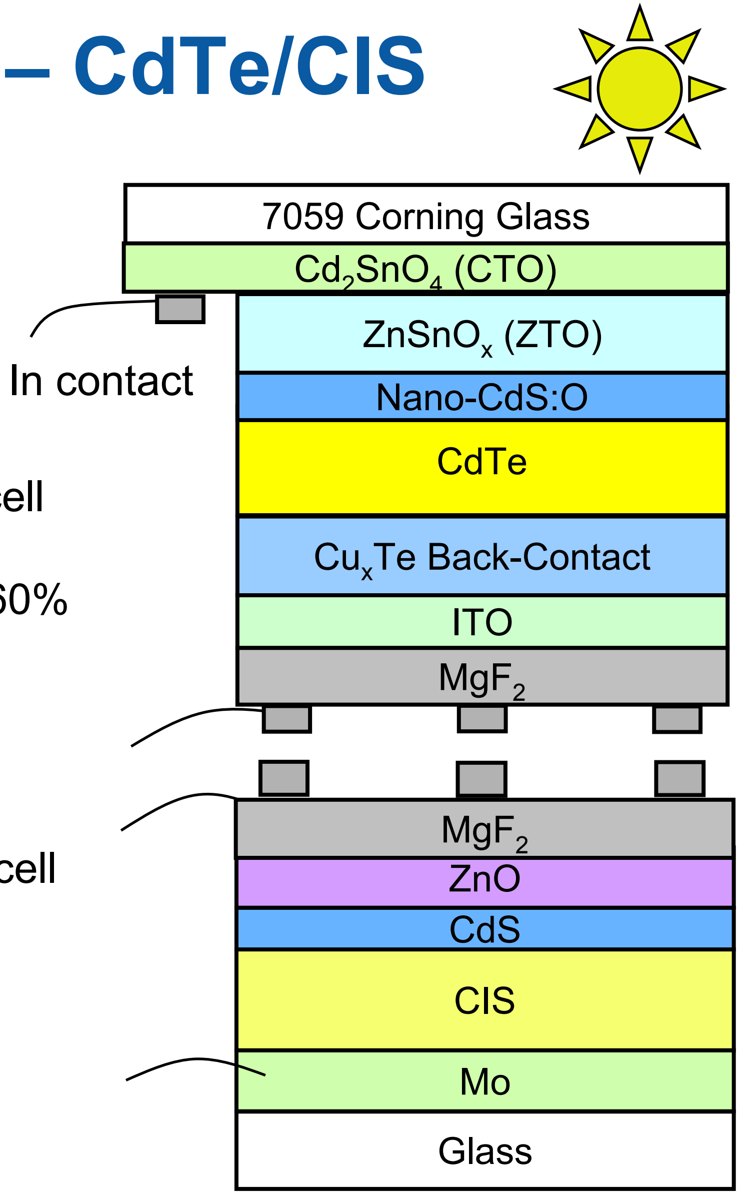
Previous record CIS bottom cell (14.5%*)

Eff. = 3.9%

V_{OC} = 0.456 V

* **J. AbuShama** et al., *Prog. Photovolt: Res. Appl.* **12,** 39 (2004).

Tandem – CdTe/CIS



Transparent CdTe cell
(Eff. = 13.8%)
Transmission ~40–60%

Record CIS bottom cell
(Eff. = 15%)

NREL official measurement

Eff. = 15.31%, V_{OC} = 1.144 V

Device Stucture (top cell):
Modified borosilicate-glass/CTO Cd_2SnO_4)/ZTO ($ZnSnO_x$) Nano-CdS:O/CdTe/Cu_xTe/ITO/Ni-Al grid

CIS cell as measured under top cell (Eff. = 1.5%)

High-Bandgap Structures/Operating Parameters
(NREL verified)

Organization	High-Bandgap Top-Cell Structure (eV)	Voc (V)	Jsc (mA/cm^2)	Fill Factor (%)	Efficiency (%)	Comments
NREL	Glass/Mo/CGS/CdS/ZnO (1.64 eV)	0.823	18.61	66.8	10.2	Surface modified CGS
NREL	Glass/Mo/CGS/CdS/ZnO (1.68 eV)	0.905	14.8	70.9	9.53	
NREL	Glass/SnO_2/CGS/CdS/ ZnO (1.68 eV)	0.864	15.36	51.25	6.8	60%–70% transmission
NREL	Glass/TCO/CdS/CdMgTe	0.8	19.51	15.72	8	
University of Delaware (IEC)	Glass/Mo/Cu(InGa)Se_2S/CdS/ ZnO/ITO (1.5 eV)	0.77	20.6	75.3	11.9	
NREL	Glass/Cd_2SnO_4/$ZnSnO_x$/nano -CdS:O/CdTe/Cu_xTe (1.5 eV)	0.806	24.97	69.22	13.9	60%–40% transmission

Polycrystalline Thin-Film Tandems

Tandem Solar Cells/Operating Parameters

(NREL verified)

Organization	Tandem Structure	Voc (V)	Jsc (mA/cm^2)	Fill Factor (%)	Efficiency (%)	Comment
NREL	Top cell: glass/SnO_2/CGS/CdS/ZnO Bottom cell: glass/Mo/CIS/CdS/ZnO Mechanical stack	0.864 0.456 1.29	15.36 12.46	51.25 69.17	6.8 3.9 9.7	4-terminal device
NREL	Topcell: glass/Cd_2SnO_4/$ZnSnO_x$/nano-CdS:O/CdTe/Cu_xTe Bottom cell: glass/Mo/CIS/CdS/ZnO Mechanical stack	0.786 0.357 1.14	25.5 6.059	68.9 68.01	13.8 1.47 15.3	4-terminal device
University of Delaware (IEC)	Monolithic structure: ZnO/ITO/CdS/ Cu(InGa)Se_2 /ZnO/CdS/CIS/Mo/glass	0.688	10.4	52.8	3.8	
University of Toledo	Monolithic structure: SnO_2:F/CdS/CdTe/ZnTe:N/ZnO:Al/CdS/ HgCdTe	0.960	2	62	1.2	

$Cd_{1-x}Mg_xTe$ Alloys

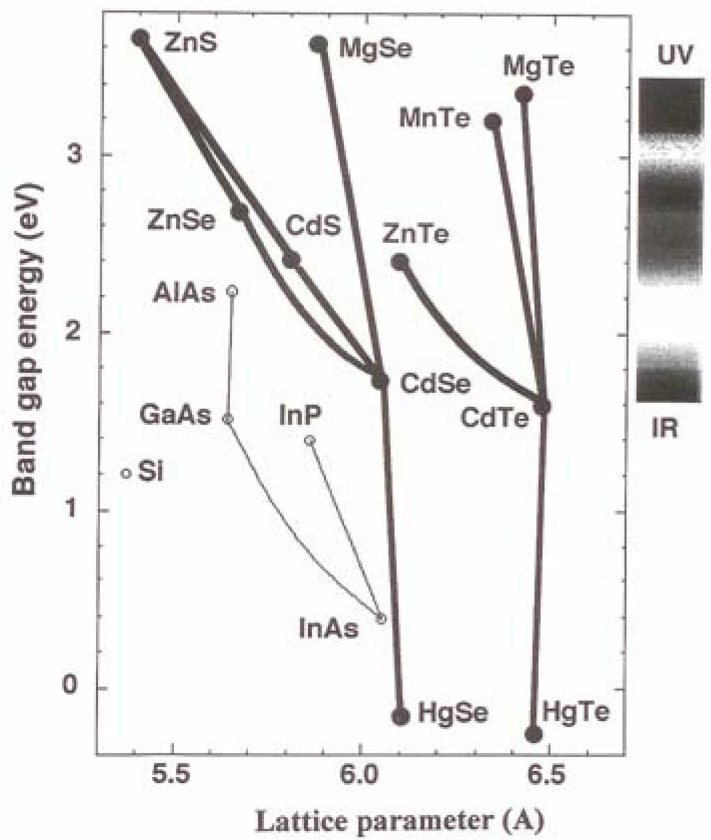
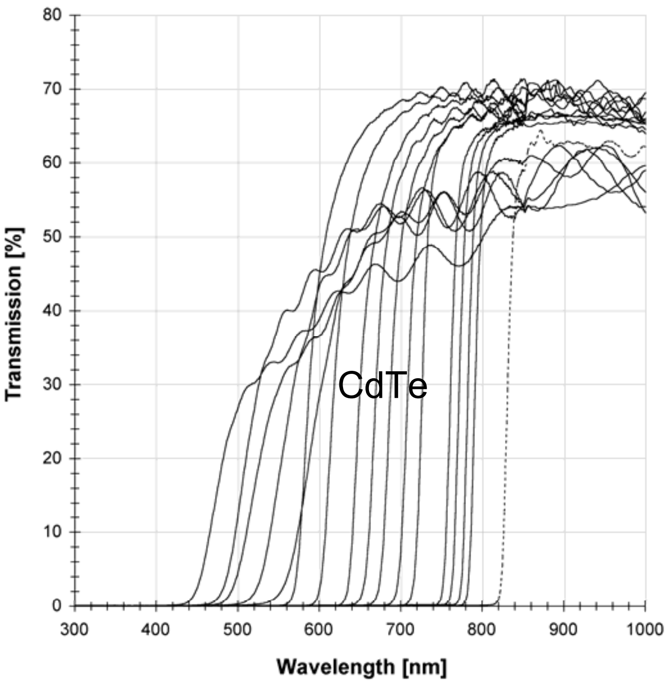
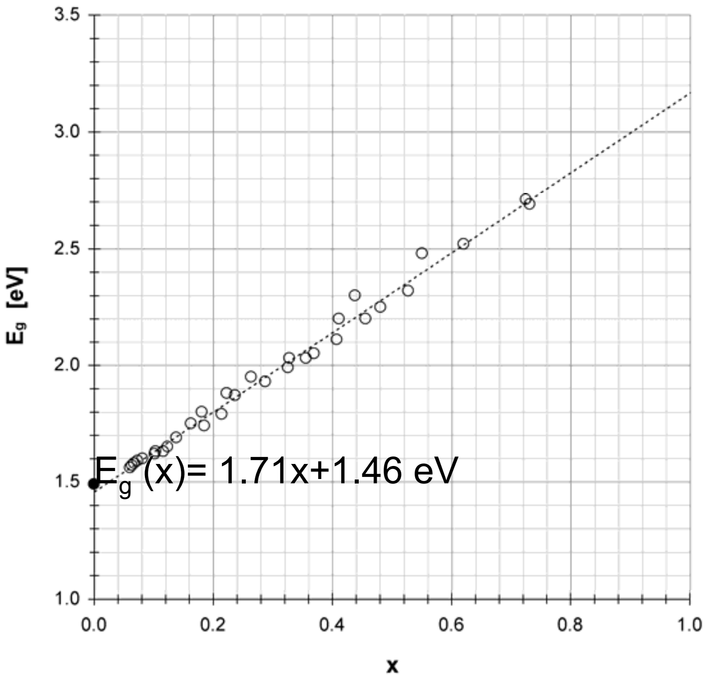


FIGURE 1. Bandgap energy versus lattice parameter for common II-VI semiconductors. The bold lines indicate the possible ternary alloys. Note that at present, there is some uncertainty in the values of parameters for Mn and Mg related compounds. Parameters for III-V compound semiconductors in the cubic phase and for silicon are also indicated for comparison.

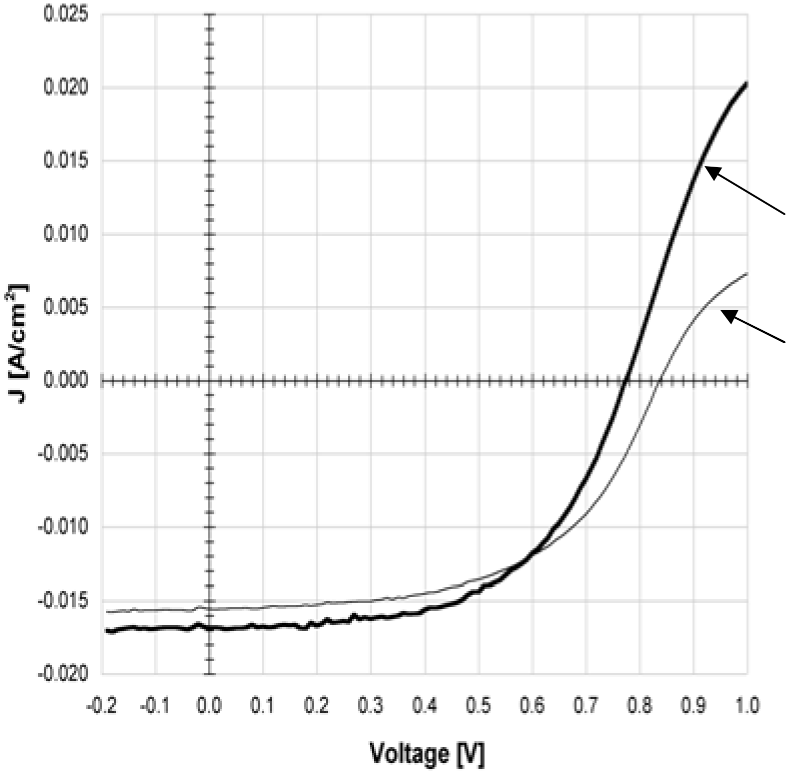
- Largest range of energy gaps with the least addition of alloying element (Mg)
- Least deviation from the lattice constant of CdTe
- Linear variation of E_g with x
- Tetrahedral radius of CdTe = 2.81 Å, MgTe = 2.76 Å
- Amphoteric doping possible

Optical Properties of $Cd_{1-x}Mg_xTe$ Alloys





Device Performance of CMT Devices



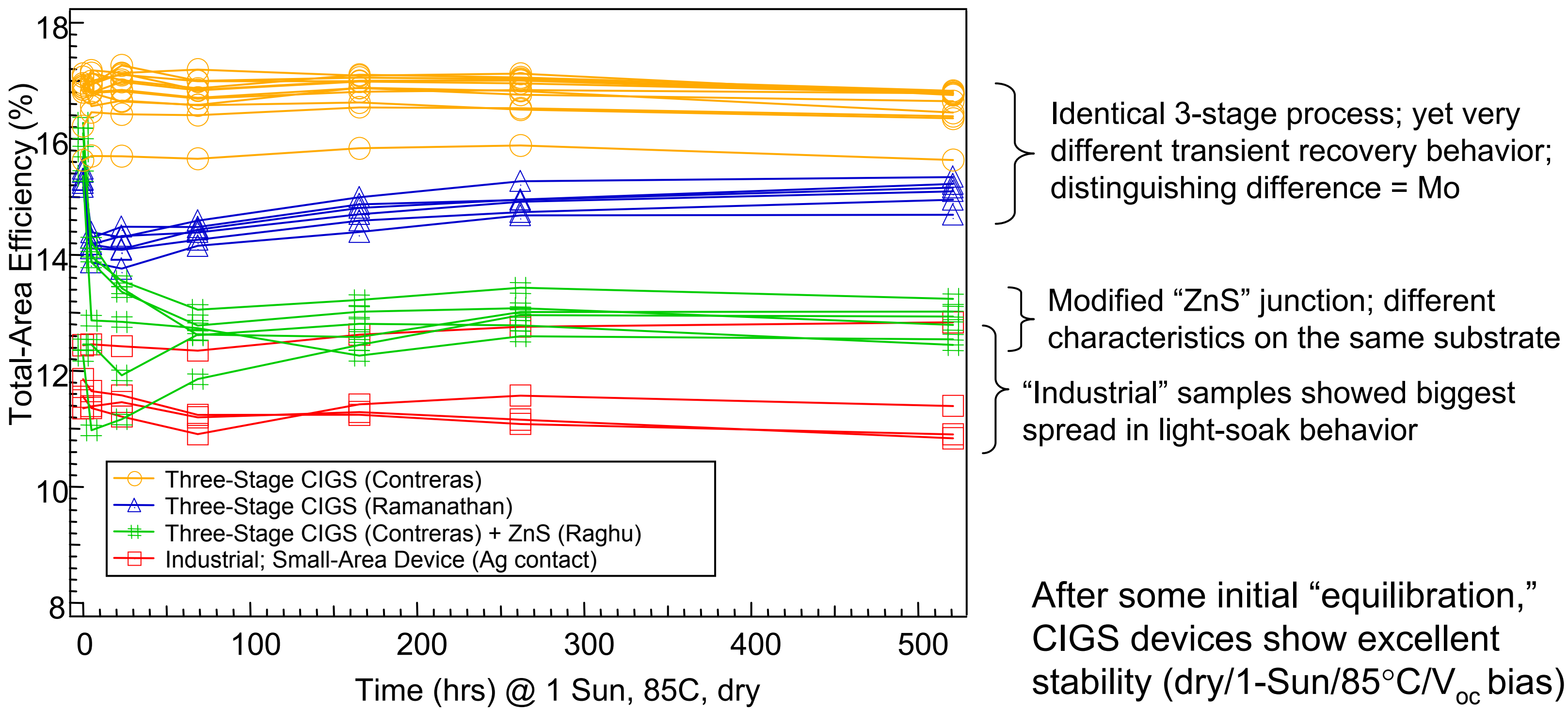
Alloy	V_{oc} (V)	J_{sc} (mA/cm^2)	Fill factor (%)	Efficiency (%)
$Cd_{0.93}Mg_{0.07}Te$ (1.6 eV)	0.796	19.51	51.78	8.04
$Cd_{0.92}Mg_{0.08}Te$ (1.62 eV)	0.845	16.38	52.36	7.25
CdTe (1.49 eV)	0.779	21.09	56.89	9.35

Relevance/Impact of Research

"This project clearly addresses multiple issues that are critical to the objectives of the DOE program. It addresses not only the top cell issues but a variety of other issues such as TCOs and mechanical stacks as alternatives to the monolithic approach."

"The work provides multiple paths to achieving DOE goals and excellent progress has been made in multiple areas. The top cell development should remain a priority for the program in view of the success achieved with CGS." **The impact of the research is scored near outstanding.** Peer Review 05

CIGS Stability Dry/1-Sun/85°C/V_{oc} Bias

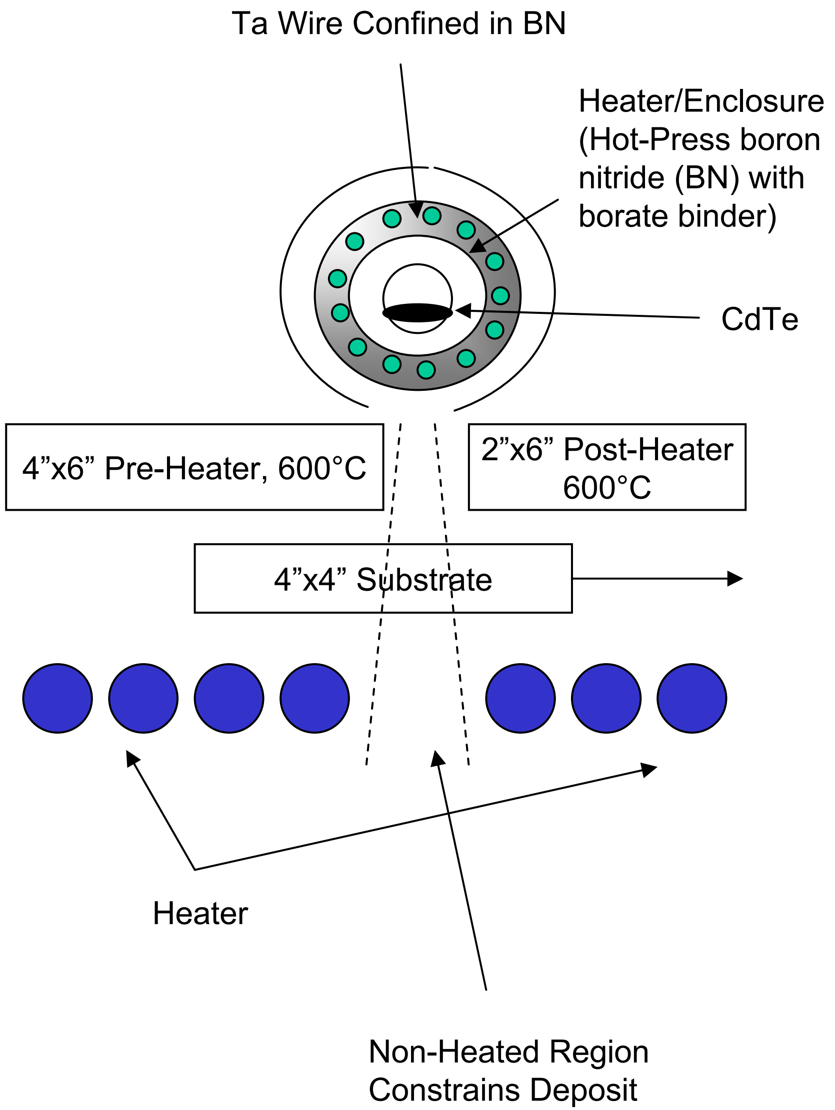


After some initial "equilibration," CIGS devices show excellent stability (dry/1-Sun/85°C/V_{oc} bias)

The relevance of the research is thought to be quite strong. The work is described as "[v]ery sound fundamental research addressing a significant barrier to large scale utilization of CdTe."

Peer Review FY05

IEC VTD



Close-Spaced Sublimation (CSS) Schematic