# Advances in Continuous In-Line Processing of CdS/CdTe Devices Including Large Area (16” X 16”) Deposition

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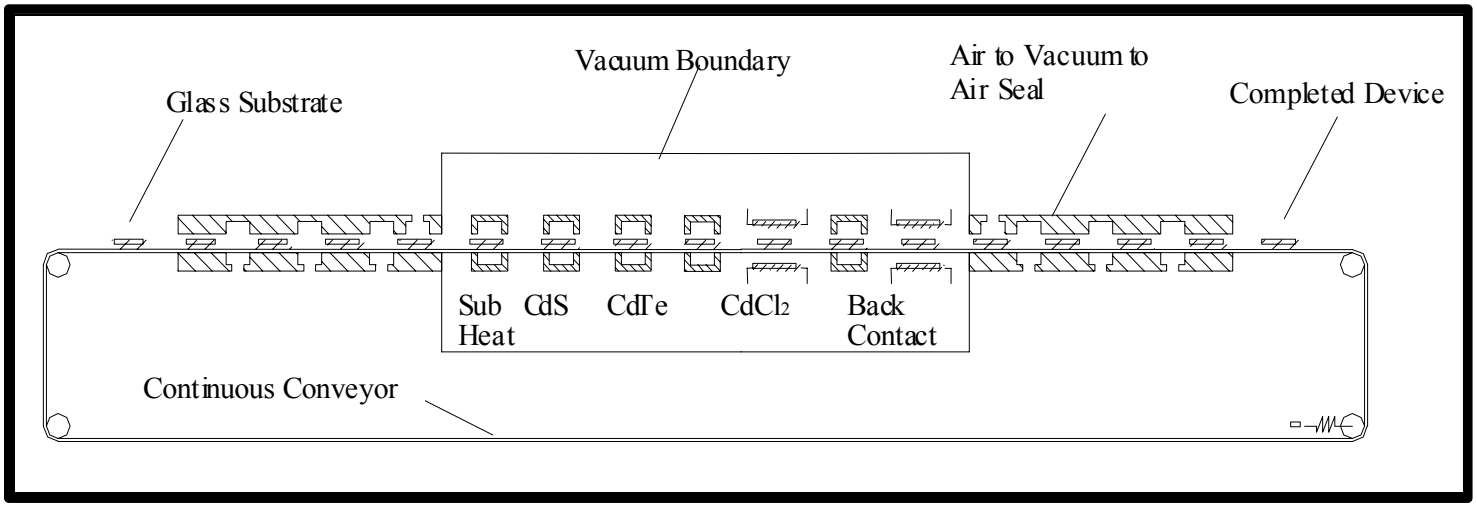
# Overview

1. Process Description
2. Device Results
3. Characterization Studies
4. Scale-up and Large Area Processing

# Process Schematic Semiconductor Fab.




## I. Semiconductor Processing

- Vacuum thin film deposition in modest vacuum
- Sublimation of solid materials
- 7 process deposition, annealing and heat treatment process steps
- All process heads similar

## II. Manufacturing efficiency

- Fully lean, automated continuous
- 2 min cycle time

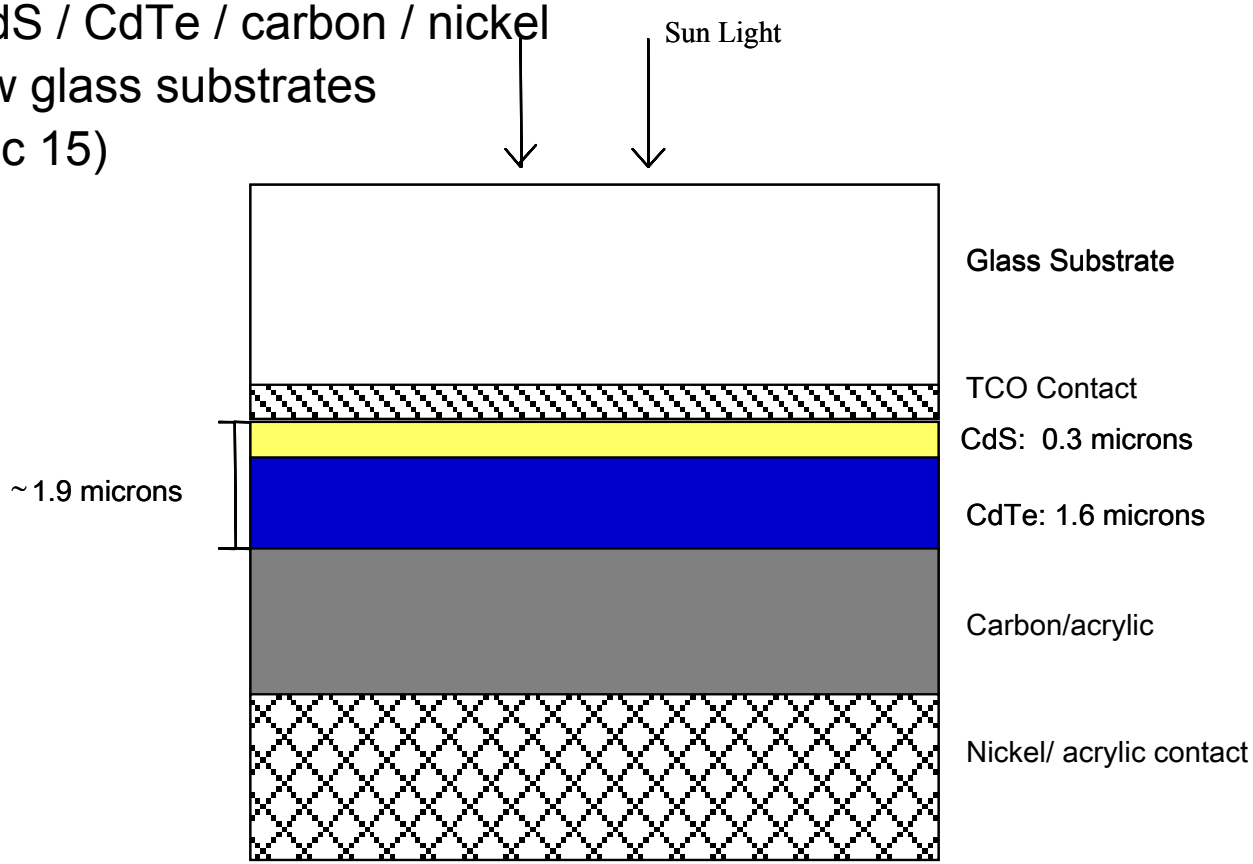
*Glass in / Completed device out every 2 min.*

# Pilot Scale System for Process Development

# Device Structure

Device structure:

- Glass/ $SnO_X$:F / CdS / CdTe / carbon / nickel
- Unmodified window glass substrates (Pilkington LOF Tec 15)

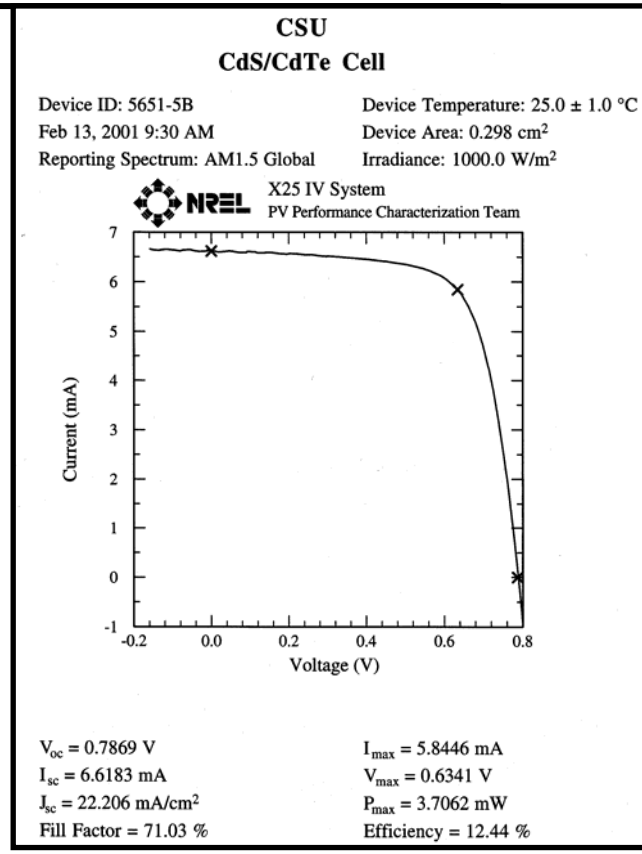



**Device structure (not to scale)**

# Device Performance

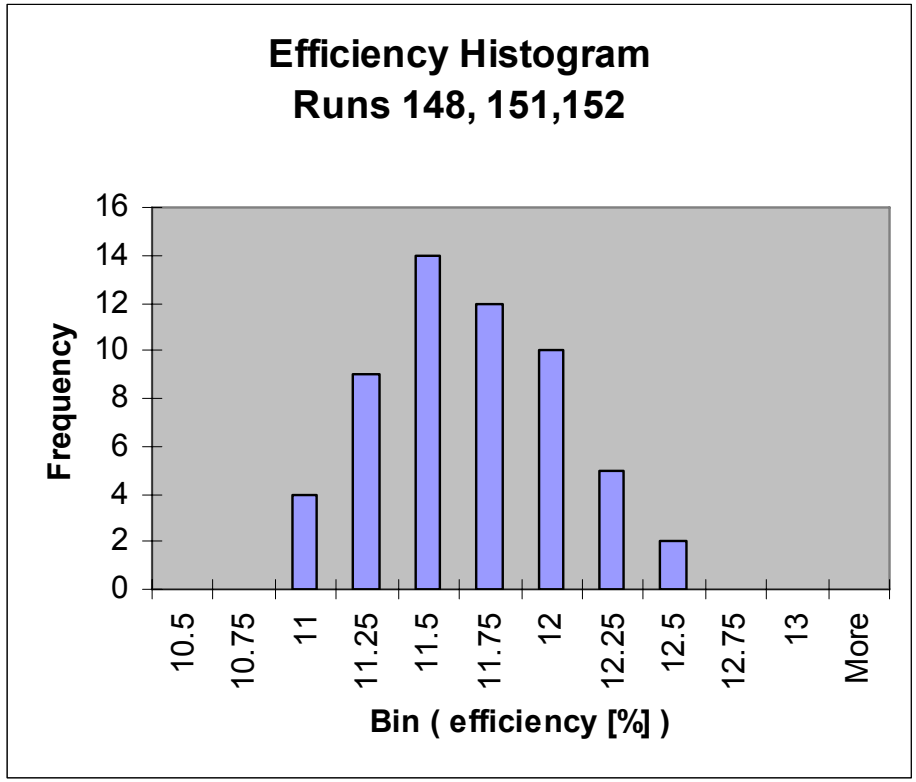
- Initial Device Performance
  - Routine 11.5 – 13% efficiency
  - NREL verified 12.44%

- Long Term Performance
  - Devices tested outdoors
  - 700 devices tested for performance under stress
  - Conditions (temp controlled)
    - 65 and 77° C with a 5/8 hr illumination
    - 100° C continuous illumination
    - One sun
    - Desiccated air



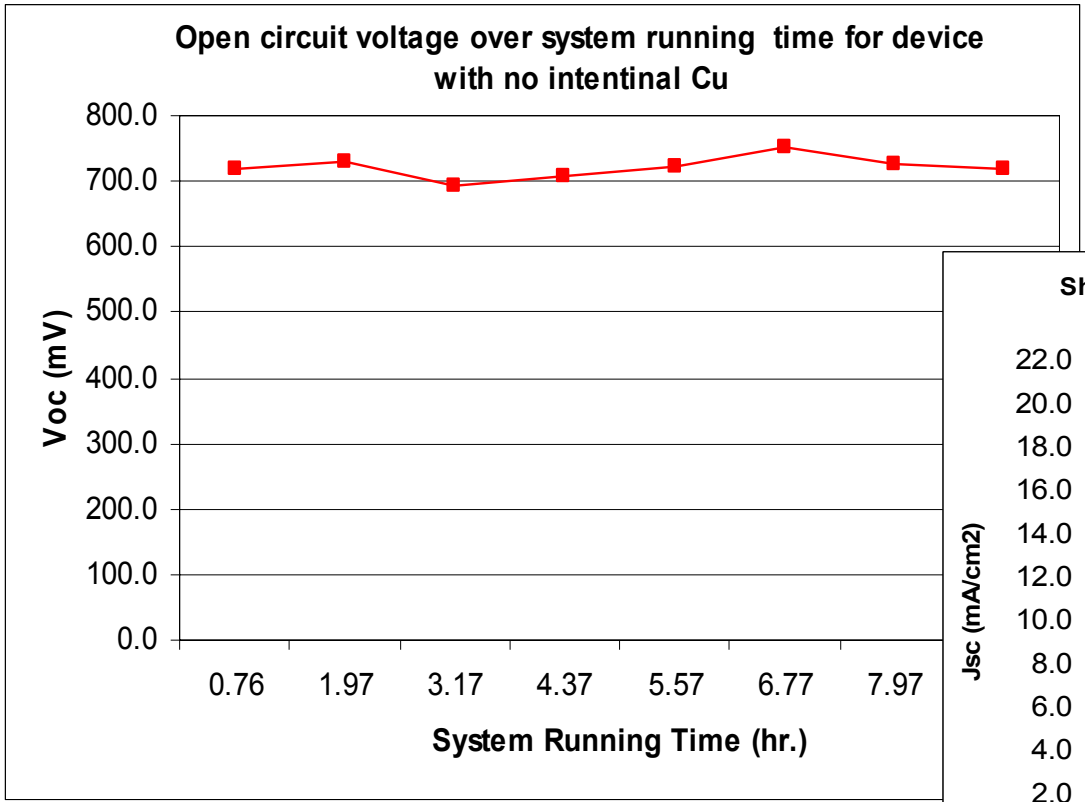

*Reliability is critical aspect for PV, 20 year life expected*
*Challenge: to determine life (without testing for 20 years) and develop a QC technique to ensure manufacture of reliable modules*

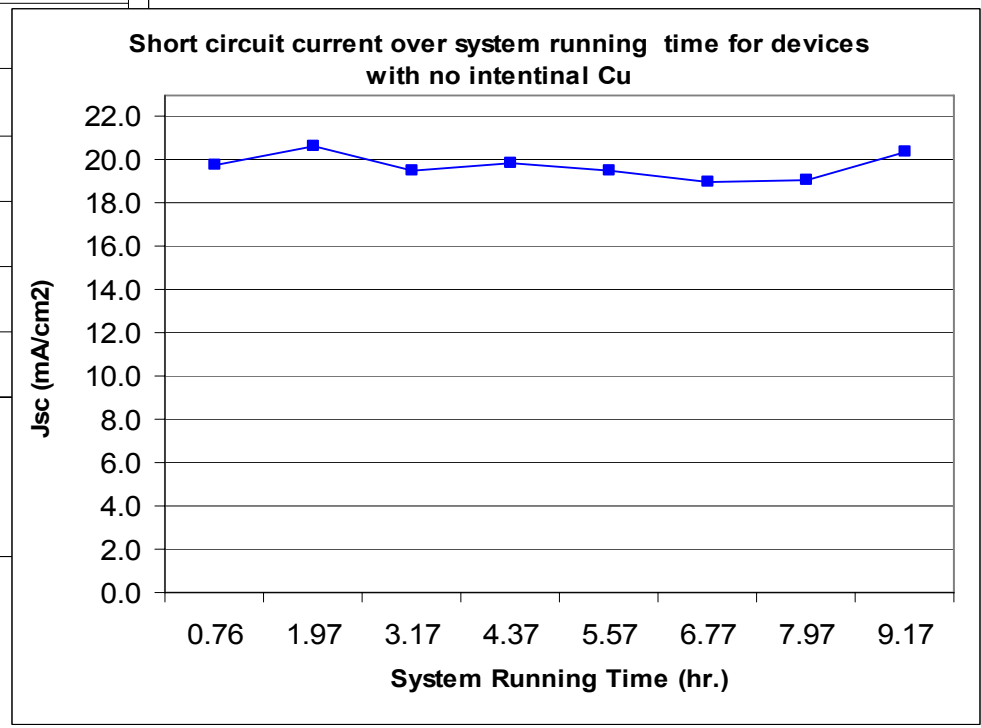
# Nine Hour Run with Same Source charge




**Efficiency distribution of devices processed over long duration of system operation with same source charge CdS, CdTe and $CdCl_2$ . The source charge materials suitable for industrial processing.**

# Nine Hour Run with Same Source charge



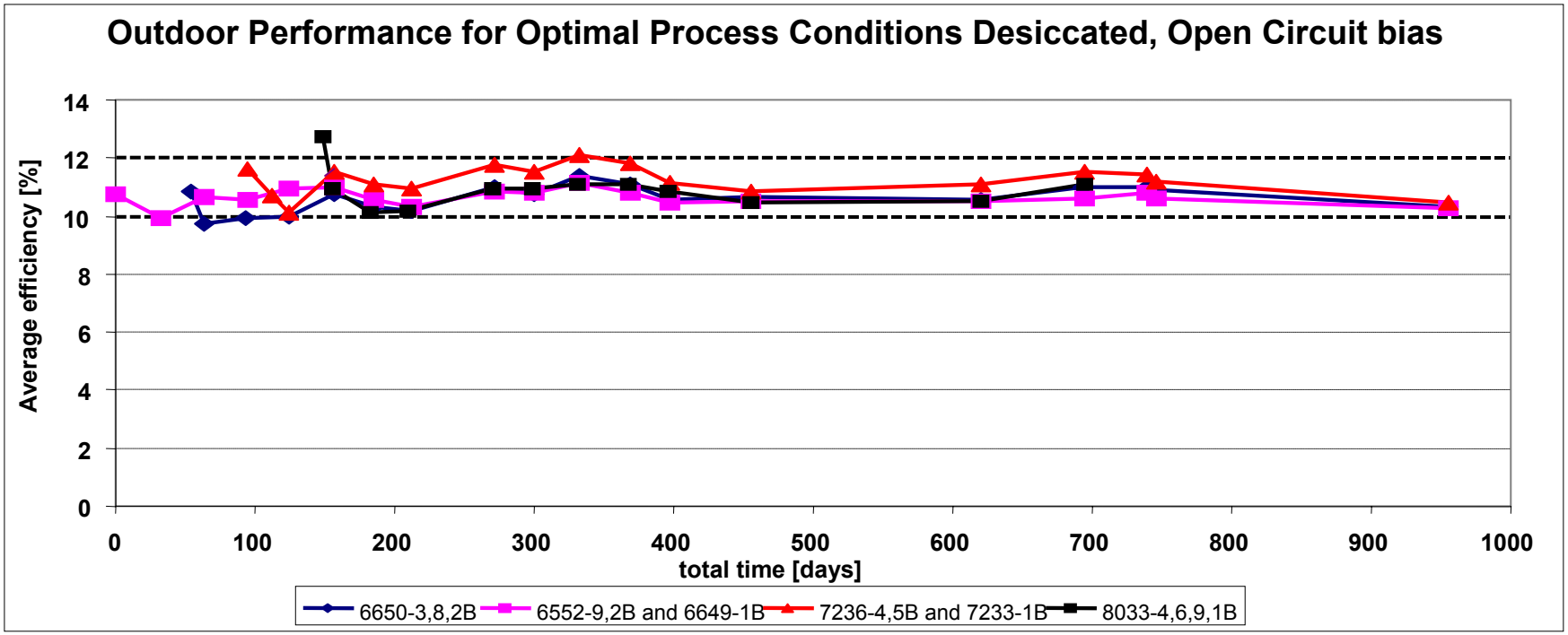




**Voc and Jsc during 9 hour processing with the same source charge for CdS, CdTe and $CdCl_2$. These devices had no back contact (no Cu doping) but had the back electrode (sprayed C and Ni films)**

# Pathways to Improve Efficiency

1. Low iron white glass to improve current.
2. Substrates sent for tin oxide coating by APCVD.
3. Intrinsic tin oxide buffer layer by APCVD and reduce CdS thickness to increase voltage and current.
4. Alloy CdTe to optimize the bandgap.

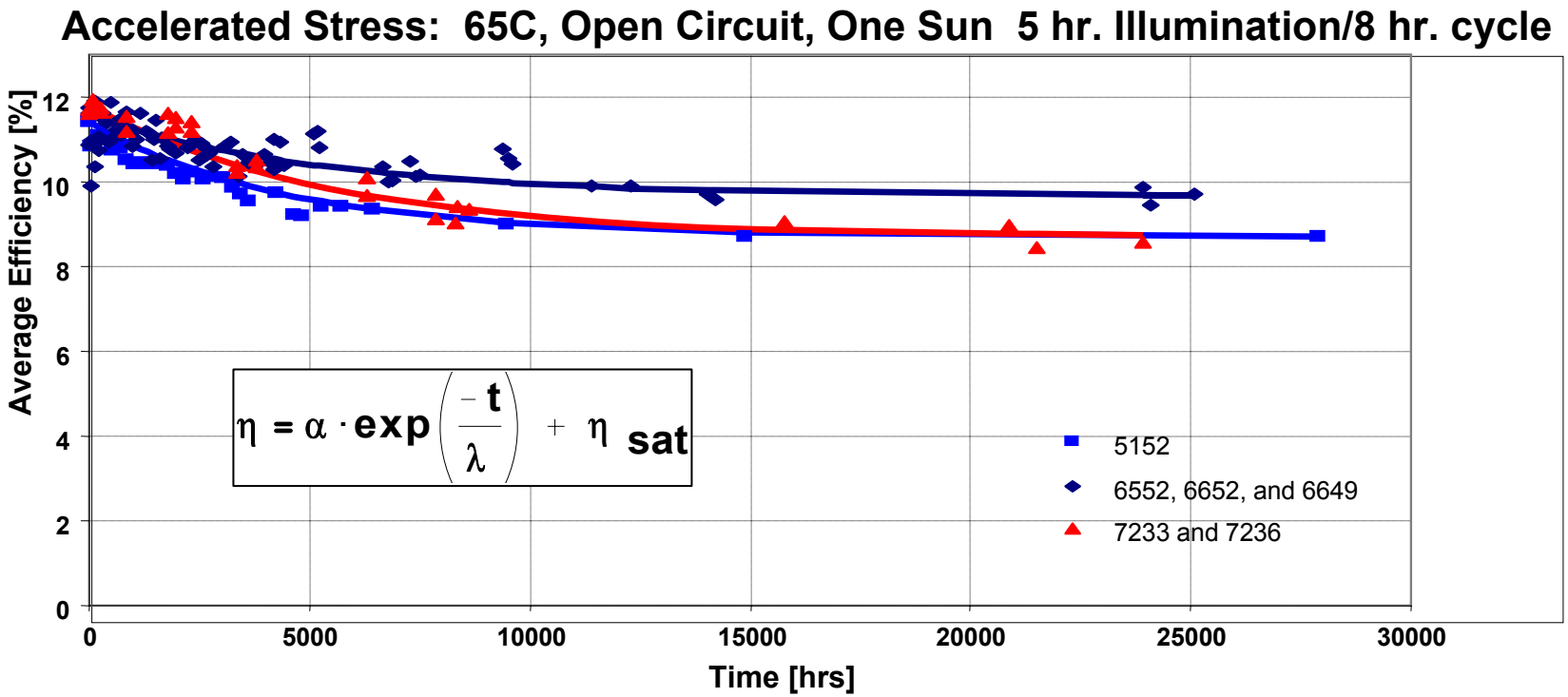
# Device Reliability Tests




## Outdoor Stability Performance

- Excellent performance in outdoor conditions
- Specialized fixture to test cells (no module issues)
- Tests ongoing
- Little or no change on average, *even at stressful open circuit conditions*

# Device Reliability Tests



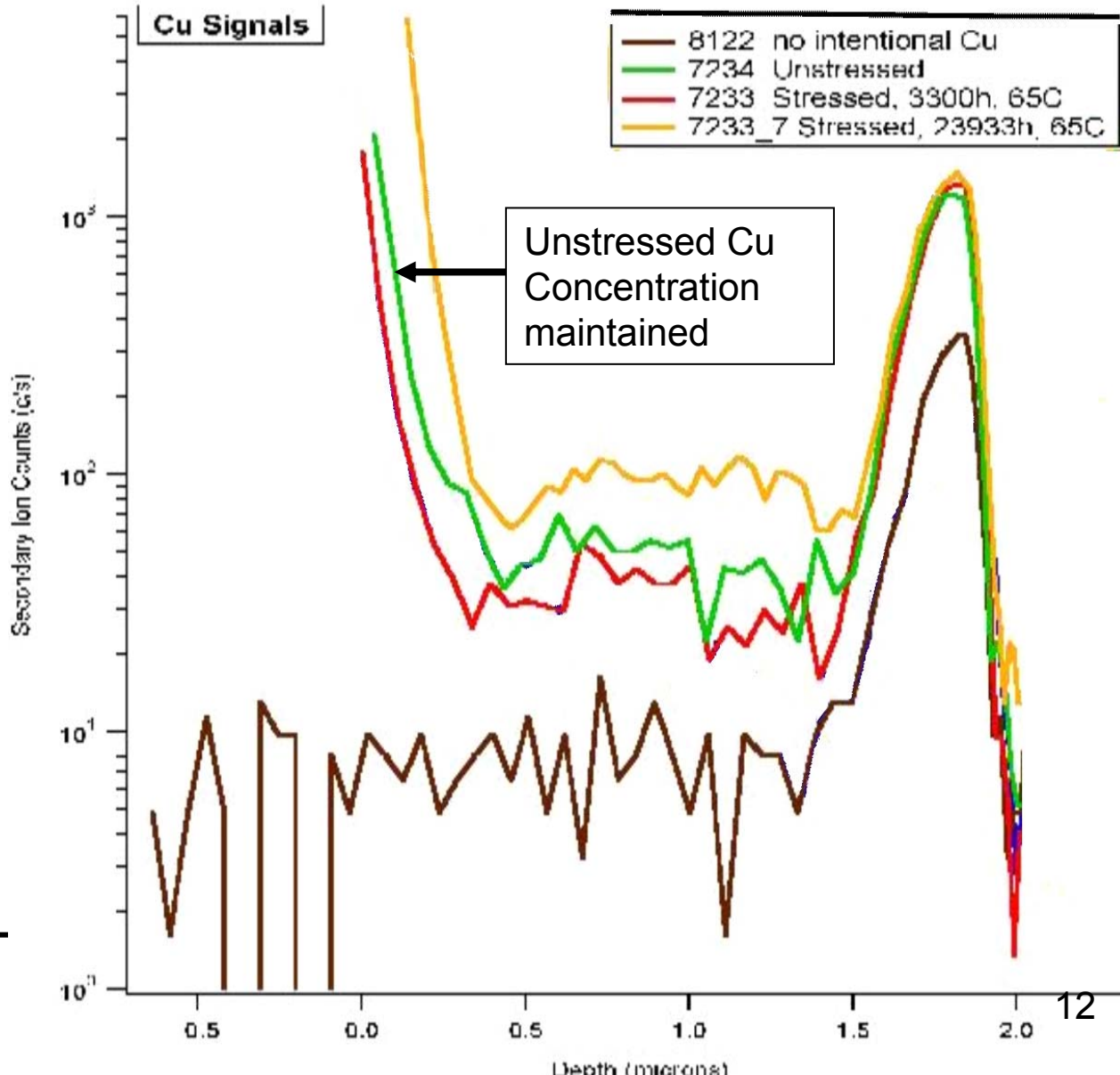

## Accelerated Stress Performance

- Extremely long term testing under stressful temperature and bias
- Efficiency levels
- Tests ongoing.

# SIMS Cu Profiles Before and After Long Term Accelerated Stress

- **Minimal changes in Cu depth profile with stress.**
- **If device is optimally processed: Cu migration is <u>not</u> a 1st order stability problem**

*SIMS data: S. Asher NREL*



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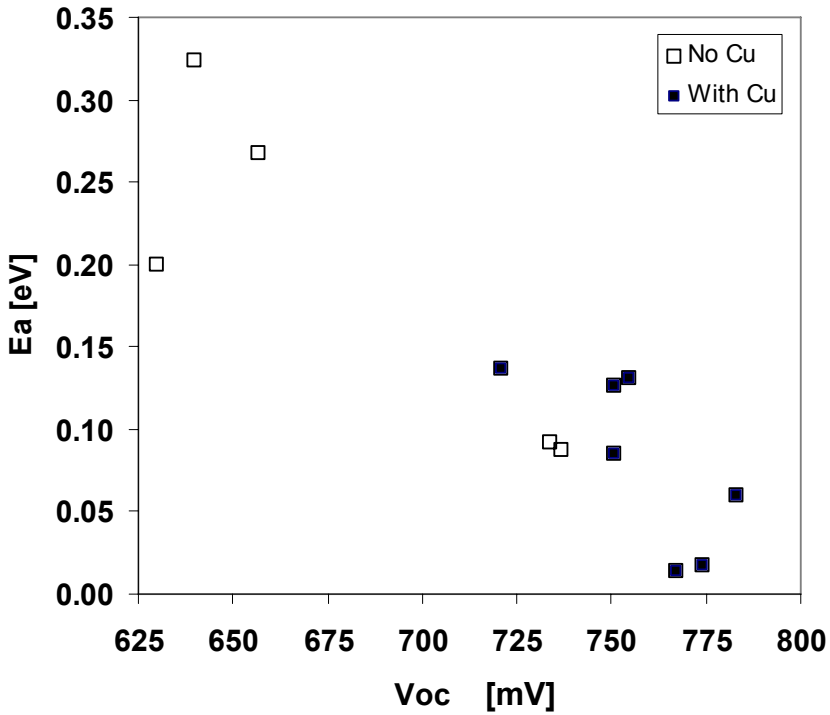
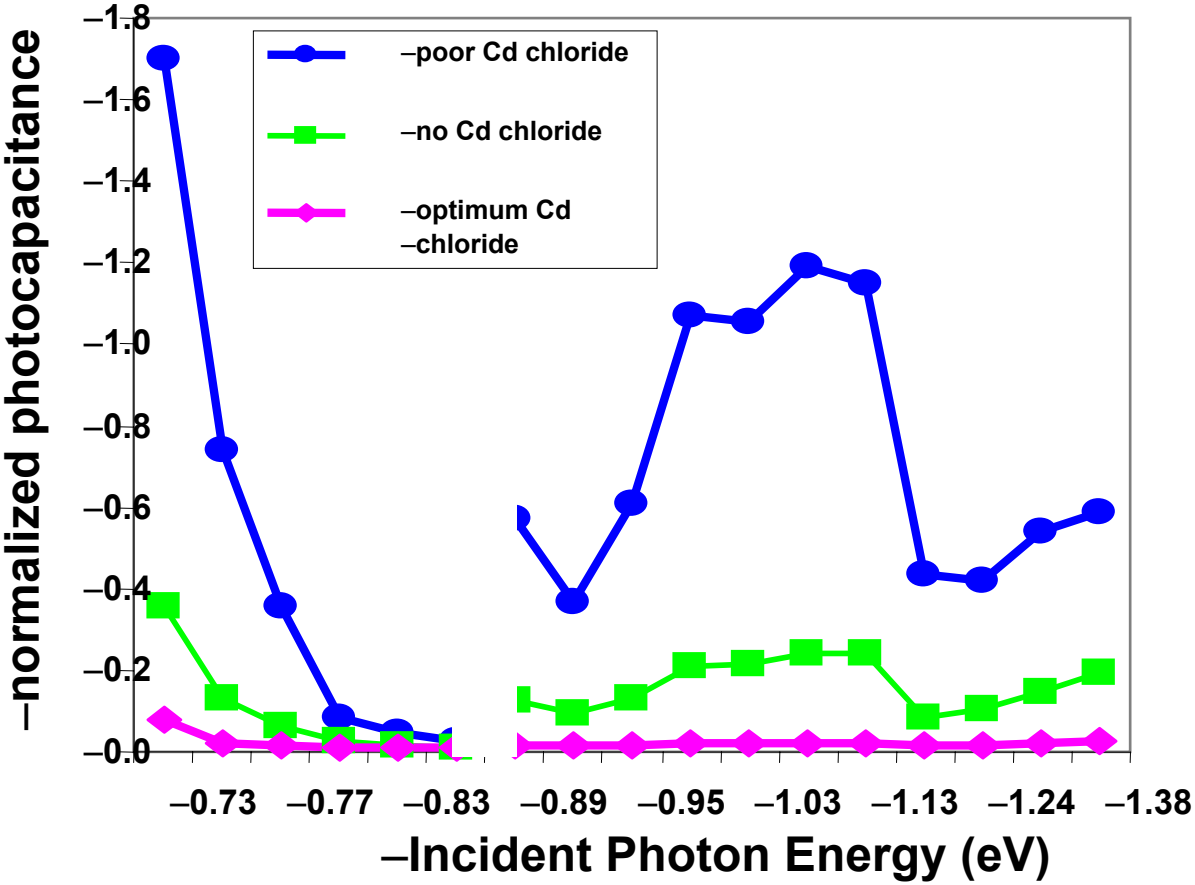
# Results from Thermal Admittance Spectroscopy

## Trap activation energy vs initial open circuit voltage




- Three devices with initial Voc's of 801, 774 and 744 had undetectable TAS signatures (devices not plotted in the above figure)
- Devices with lower defect activation energies (Ea) have better light JV performance

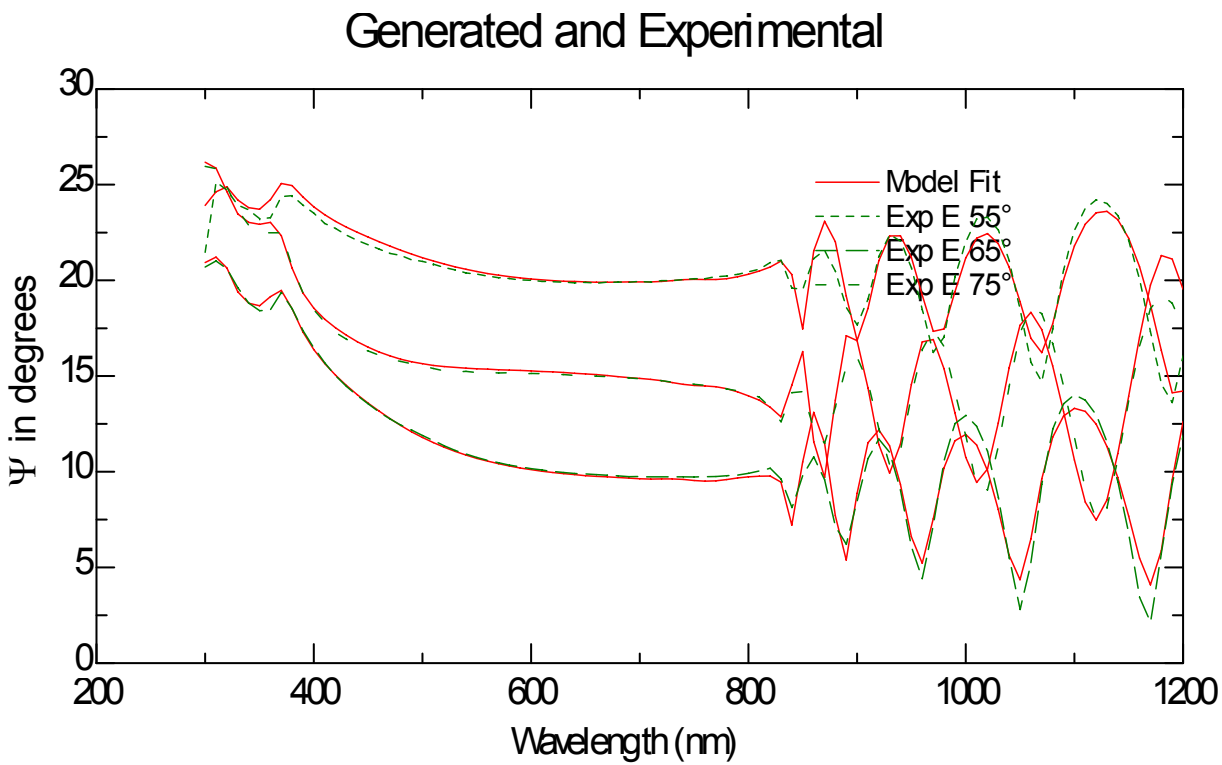
# Steady State Photocapacitance Spectrums




- *+0.4 V during PHCAP ; +1 V bias at room temp and during cool down*

- **Poor treatment increases trap density over non treated sample**
- **Optimum treatment decreases trap density over non treated sample**

# Ellipsometry




Spectroscopic ellipsometry data and model fit for a LOF Tec 15 substrate with SnO:F/CdS/CdTe:Cu which had received $CdCl_2$ treatment.

# Scale up strategy

## I. Step by step approach: Developing highly controlled, scalable processes and hardware

- Develop detailed understanding of process
- Develop only process that are scalable and manufacturability and lean
- Define process conditions at each stage

3x3 inch pilot process → 2 MW/yr. prod. prototype → Large scale manufacturing

- Each stage of the process defined:
  - Substrate temperature
  - Vapor flux
  - Residual gas

# 2 MW/yr. system under construction

# Results with the 2 MW system

1. Substrate transport with loadlock operational
2. 16.5 X 16.5 inch$^{-1}$ substrates heated from 25C to ~500C in two minutes with no glass cracking
3. Films deposited on 16.5 x 16.5 inch substrates with +/- 5% uniformity in another setup

# Approach for making modules

1. Nd-YAg laser promising for scribing SnO:F. Mechanical scribing of CdS/CdTe films better for low series resistance.
2. Preliminary results suggest that tempered 3 mm glass substrates will lead to adequate resistance to hail impact and static load.
3. Fixtures simulating glass/EVA/glass package with Truseal solar edge tape have passed 3000+ hours of damp heat testing.

# Conclusions

1. Consistent device performance demonstrated in continuous in-line processing of CdS/CdTe devices.
2. Optimum processing leads to stable SIMS copper profile.
3. Optimum $CdCl_2$ treatment leads to lower defect densities as measured by TAS (thermal admittance spectroscopy) and PHCAP (photocapacitance).
4. Rapid heating of 16.5 X 16.5 inch substrates and uniform film deposition demonstrated.