High Temperature Capacitor R&D

Steven Boyd
Email: steven.boyd@ee.doe.gov
Phone:202-586-8967
Organization: DOE Vehicle Technologies Program

Laboratories: Argonne & Sandia

University: Pennsylvania State University

Project Duration: FY 2003 – FY 2012

DOE Vehicle Technologies Program
Advanced Power Electronics and
Electric Machines Projects
2008 DOE OVT Annual Merit Review Meeting

Bethesda North Marriott
Bethesda, MD

February 28, 2008

This presentation does not contain any proprietary or confidential information

Purpose of Work

•Develop technologies to enable a range of new, high performance, economical, capacitors for hybrid electric vehicles power electronic systems.

DC bus capacitors for inverters

(600 V, 2000 µF, <3 mΩ ESR, 250 A ripple current,140°C, benign failure)

-Examine the underpinning issues of capacitor performance
-Develop robust fabrication techniques
-Develop low cost capacitor designs
-Transfer technology to industrial partners for commercial manufacturing

Response to Reviewers' Comments

- "Determine applicability of PLZT on Cu to future power inverters in terms of size, voltage withstand, and temperature."
  - Fabricating PLZT on Cu foils (see slide #8, "Uniqueness of Project").
- "Need to withstand PWB flexing and vibration modes will have on the embedded capacitor."
  - These important considerations are included in our list of necessary component tests (Argonne/Delphi CRADA).
- "Accomplishments are very good. The PI has listened to past comments & followed thru' to incorporate recommendations into his research plan."
  - Thank you reviewers for your valuable comments/recommendations.
- "Glass ceramics show considerable promise. The issues will be mechanical integrity and tangent delta at high temperature."
  - Glass is a major material in automobiles. We are exploring fabrication techniques to minimize damage.
- "What is the status on benign failure mode?"
  - Initiated work on electrodes on glass to demonstrate benign failure.
- "Need characterization data on prototype norborene caps."
  - Currently working with ECI to fabricate & evaluate prototype capacitors.

Relevance to Overall DOE Objectives of Petroleum Displacement

- **Advanced inverters are essential for electric traction operations in HEVs, PHEVs, and FCVs.**

- **Future availability of advanced high-temperature (together with lower cost, weight, & volume) inverters will advance the marketplace application of highly fuel efficient & environmentally beneficial hybrid vehicles.**

- **Capacitors have direct impact on overall size, cost, & performance of inverters.**

Role of Capacitors:

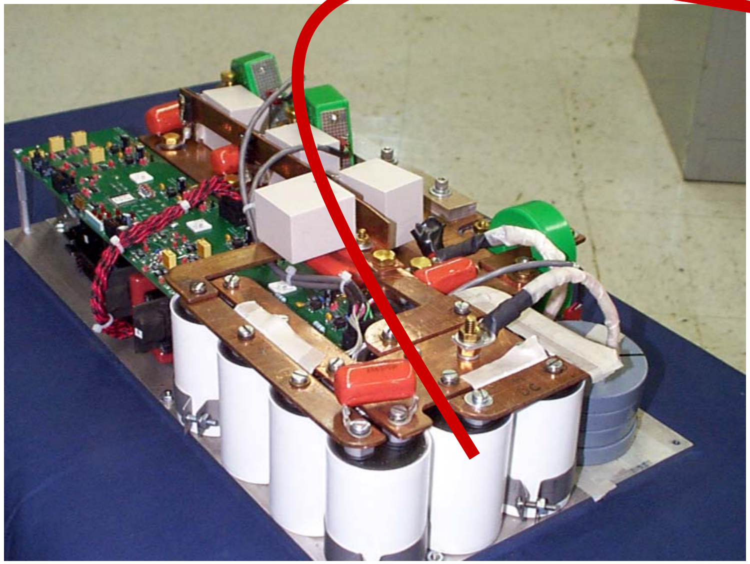
- **DC bus capacitors are essential to prevent ripple currents from feeding back to the power source**

- **Serve to smooth out DC bus voltage variations**

The Problem/Barriers

- **Capacitors have a significant influence on inverter lifetime, reliability, and high temperature operation.**

Capacitor development will reduce the size & increase the temperature of operation of one of the largest components in the inverter: the DC bus capacitor



Power Converter fabricated by ORNL

Capacitors are a significant fraction of the inverter volume (≈35-40%), weight (≈23%), and cost (≈23%).

Technology Approaches

Organization	Dielectric Materials Technology	Strengths for Vehicle Technologies Program
Argonne National Laboratory	Embedded ceramic dielectric films on base-metal foil	Reduced size, weight, and cost, concomitant with increased capacitance density, higher temperature operation, reduced inductive losses, improved reliability, & graceful failure
Pennsylvania State University	Glass ceramics	High breakdown field at elevated temperatures Graceful failure
Sandia National Laboratory	Polymer films	High temperature performance, Volumetric efficiency, Cost effective

High Dielectric Constant Capacitors for Power Electronic Systems

U. (Balu) Balachandran
Email: balu@anl.gov
Phone:630-252-4250
Organization: Argonne National Laboratory

Collaborator: Penn State University (sub-contract thru' Argonne)

Project Duration: FY 2003 – FY 2012

FY 2008 Funding: $940K

DOE Vehicle Technologies Program
Advanced Power Electronics and
Electric Machines Projects
2008 DOE OVT Annual Merit Review Meeting

Bethesda North Marriott
Bethesda, MD

February 28, 2008

This presentation does not contain any proprietary or confidential information

Uniqueness of Project and Impact – Film-on-Foils
(caps embedded directly into PWB – caps are “invisible”)

Basic Element

Metal foil coated with thin film PLZT dielectric

- PLZT/Ni Film-on-Foil
- PLZT/Cu Film-on-Foil

Component

Stack & embed coated foils directly into printed wire circuit board for power electronics in (P)HEV

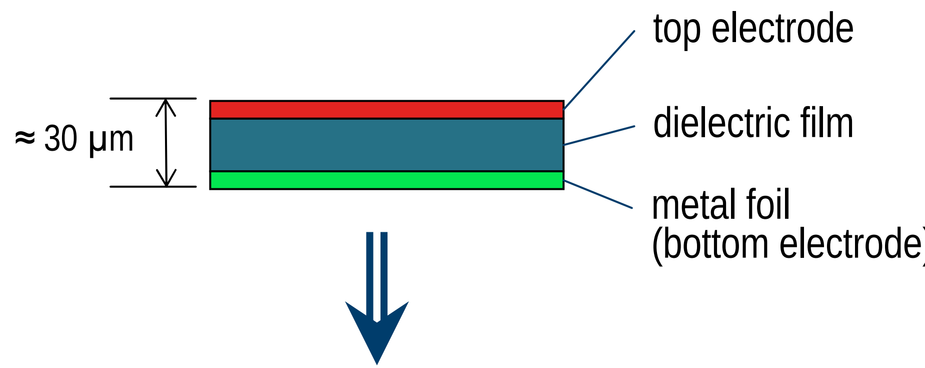
Advantages

Reduces component footprint

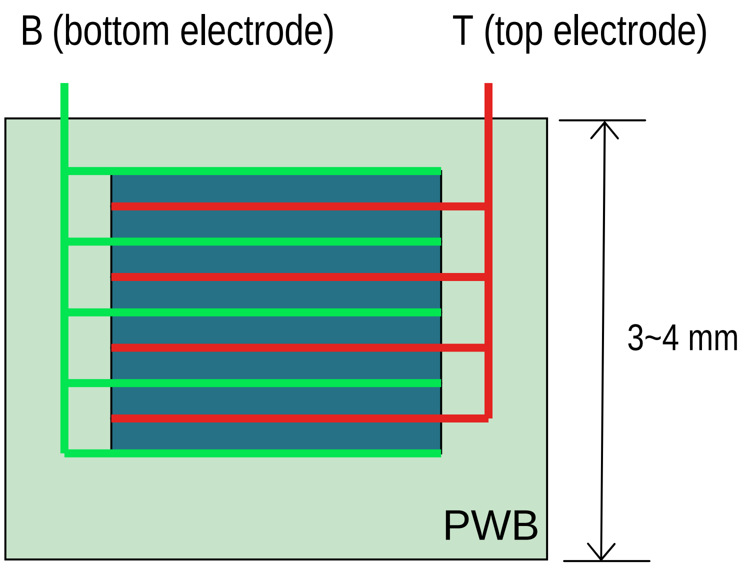
Shortens interconnect lengths

Reduces parasitic inductive losses & electromagnetic interference

Film-on-foil capacitor



PWB Embedded capacitor with interconnections



Reliability is improved because the number & size of interconnections are reduced. Solder joints that are most susceptible to failure are no longer needed.

Technology Related Challenges/Barriers

Embedded film-on-foil capacitors:

- Adhesion/delamination of PLZT on metallic foils

  -Optimize process to minimize residual stresses & enhance bonding

- Oxidation of Cu

  -Control processing atmosphere to prevent oxidation

- Defects in PLZT film (pin holes, voids, cracks, variation in composition, etc)

  -Improve solution stability & crystallization conditions

- Incorporating graceful failure in embedded architecture

  -Capitalize on proven graceful failure of film-on-foil caps thru' prudent design

- Integrating thin film caps into PWB manufacturing scheme (chemicals, connectivity, terminations, etc)

  -Bridge any gaps that develop between established PWB scheme & cap processing

- Minimization of heat treatment steps to make fabrication process economically attractive

  -Investigate techniques to increase thickness of individual cap layers

Technical Approach for FY08

- Develop film-on-foil fabrication routines to scale-up foil sizes to Printed Wire Board (PWB) areas.
- Characterize the dielectric properties and high-temperature reliability of film-on-foil capacitors.
- Produce prototype embedded capacitors.
- Electrically characterize the capacitor after embedding into a PWB.
- Develop new fabrication methodologies (eg., tape casting, dip-coating, etc.) & compositions to further enhance performance.
  - increase breakdown field and capacitance density by a factor of two, decrease loss factor by 50%, and increase energy density to >50 J/cm^3 (this will reduce the capacitor volume by ≈75%).
  - new fabrication methodologies are needed to reduce processing steps involved in making film-on-foil caps for power electronic systems.

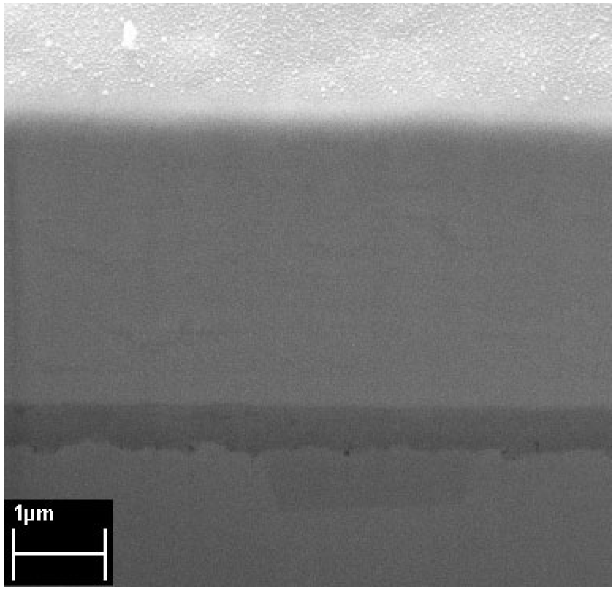
Technical Accomplishments – film-on-foils

- Demonstrated film-on-foil dielectrics with k ≈1400, capacitance density ≈1.5 μF/cm^2, breakdown field ≈2.5 MV/cm, and leakage current <10^{-6} A/cm^2.
- Film-on-foil dielectrics are thermally cycled (about 1000 cycles) between -50°C and +150°C with no measurable degradation in k.
- Demonstrated graceful failure mode by self-clearing method in film-on-foil dielectrics (U.S. Patent 7,099,141 B1, Aug. 29, 2006).
- Thin ceramic dielectric on relatively thick Ni substrate is quite strain tolerant; tolerance limit depends on thickness of sample (measured at ORNL by Andy Wereszczak).
- A CRADA with Delphi has been established. Samples have been provided to Delphi for testing embeddability.
- Acquired a large-area commercial coater to fabricate samples for embedding into printed wiring boards.
- Over 25 publications and presentations have been made.

PLZT

LNO

Ni

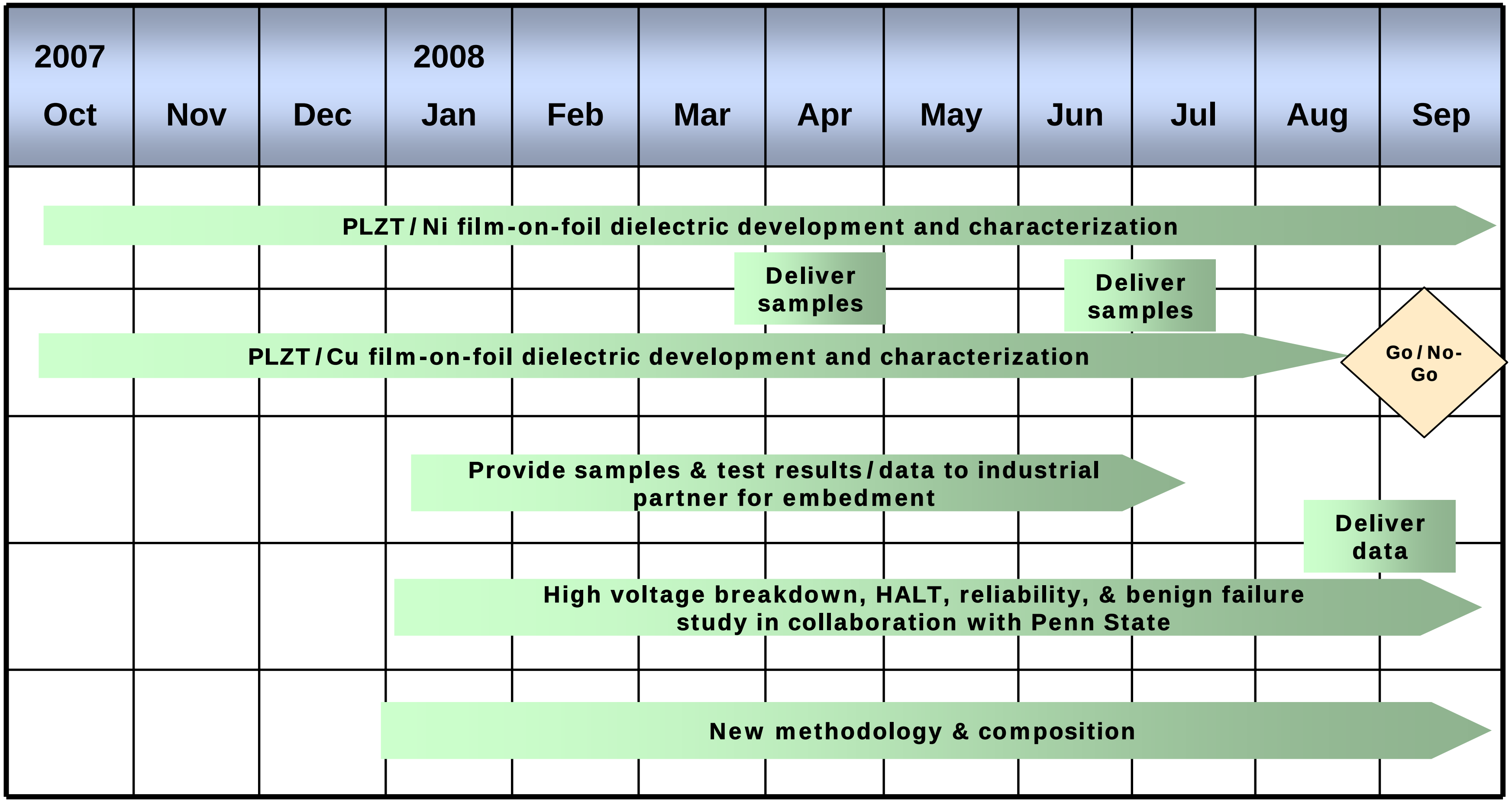


PLZT – $Pb_{0.92}La_{0.08}Zr_{0.52}Ti_{0.48}O_3$

Future Work – Film-on-foil Caps

- **FY09**
  - **Fabricate large number of large area film-on-foils defined by the inverter application requirements for embedding into inverter circuit boards.**
  - **Test fabrication methodologies & compositions for enhanced performance.**
- **FY10**
  - **Develop process for manufacturing large area caps for hybrid electric power electronic systems.**
  - **Develop down-selected methodology/composition for performance-enhanced caps.**
- **FY11**
  - **Fabricate prototype device to demonstrate enhanced properties & establish industrial collaboration.**
- **FY12**
  - **Work with industrial collaborator(s) to fabricate device with enhanced performance.**
  - **Transition to production.**

Timeline for FY 08 – Argonne's Embedded Cap Approach



Decision point discussion: Either continue the two-pronged approach, i.e., PLZT/Ni and PLZT/Cu, or down-select one over the other.

Glass Ceramic Dielectrics for DC Bus Capacitors

Mike Lanagan
Email: mlanagan@psu.edu
Phone:814-867-6094
Organization: Penn State University

(sub-contract thru' Argonne)

Project Duration: FY 2006 – FY 2010

FY 2008 Funding: $150K

DOE Vehicle Technologies Program
Advanced Power Electronics and
Electric Machines Projects
2008 DOE OVT Annual Merit Review Meeting

Bethesda North Marriott
Bethesda, MD

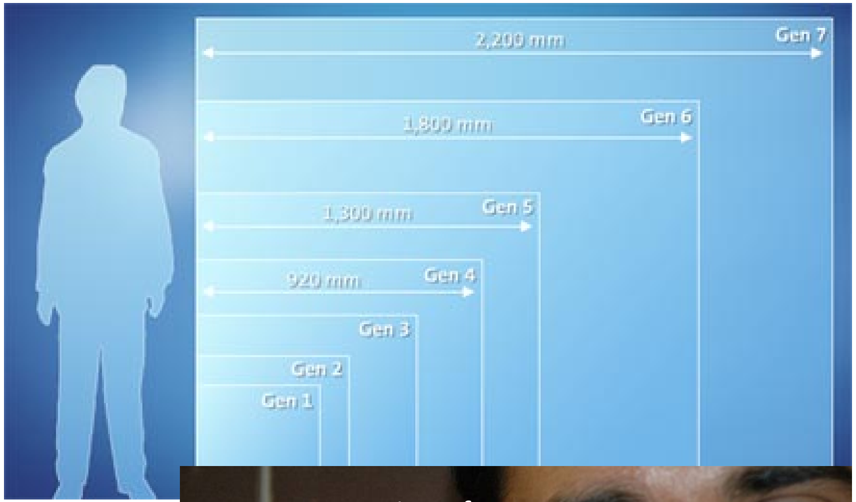
February 28, 2008

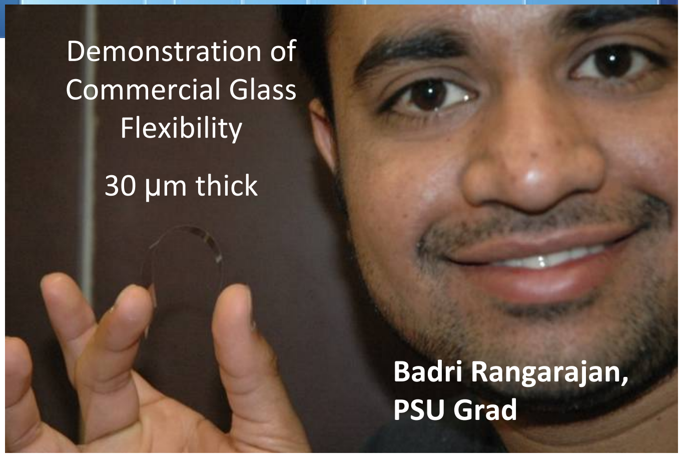
This presentation does not contain any proprietary or confidential information

Uniqueness of Project and Impact – Glass Ceramics

- Large scale processes have been developed for producing thin glass sheets.
- Commercial market is growing rapidly for flat panel displays.
- Companies are interested in exploring new markets for flat panel glass (i.e. capacitors for HEV and PHEV).

Projected glass plate dimensions for active matrix liquid crystal displays. The glass is an excellent commodity material for high temperature capacitors for use in hybrid electric vehicles.

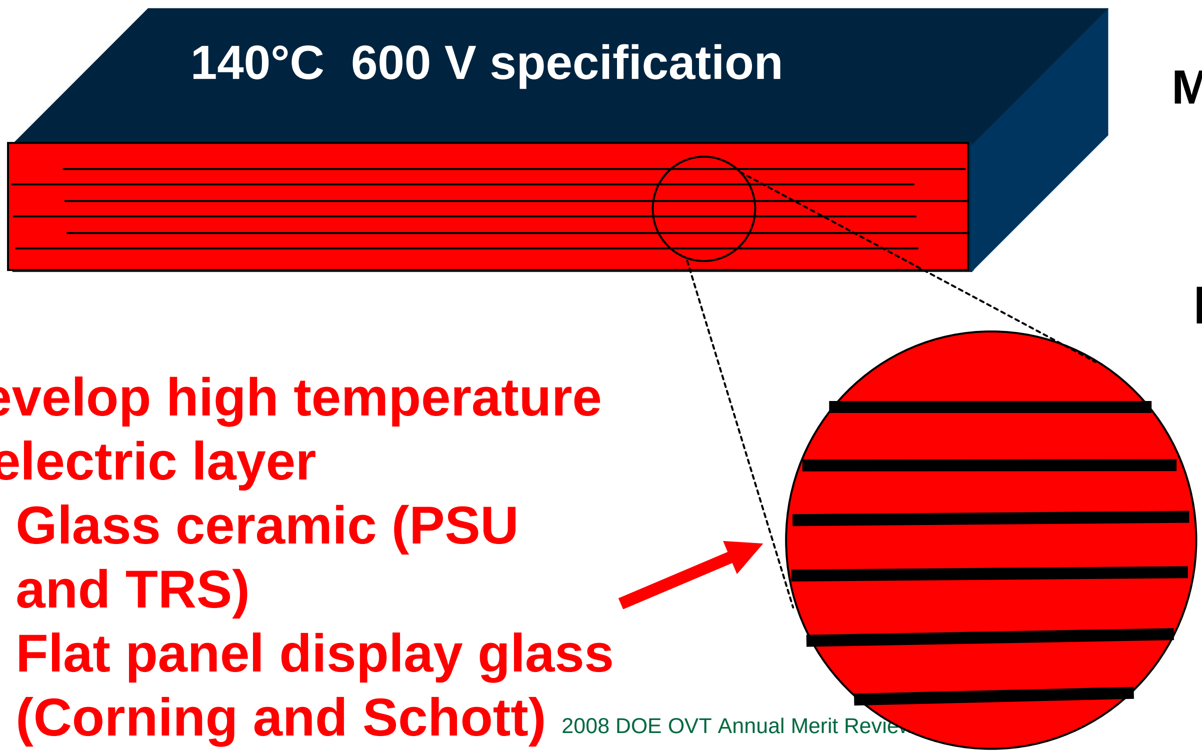




Technology Related Challenges/Barriers

Glass Ceramic Capacitors:

- Scale-up to meet 2000 μF, 600 V DC bus requirements
  - Collaborate with industrial partners (Corning, Schott, & TRS)
- Electrode degradation during high temperature reliability characterization
  - Perform highly accelerated life testing with robust metal contacts



Multilayer Glass Capacitor

Develop electrodes for high-T operation

Develop high temperature dielectric layer

1) **Glass ceramic (PSU and TRS)**
2) **Flat panel display glass (Corning and Schott)**

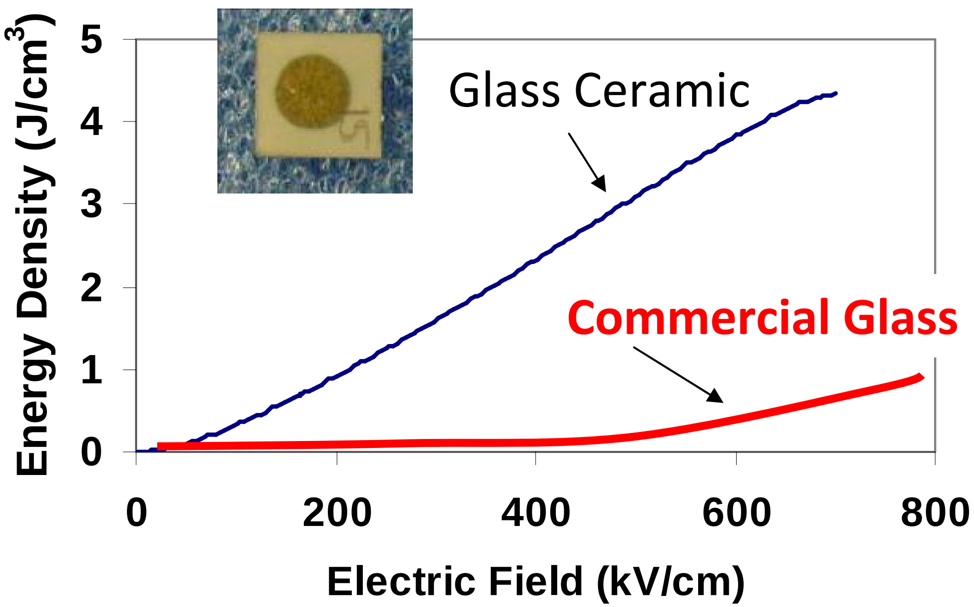
Technical Approach for FY08

Glass Ceramics:

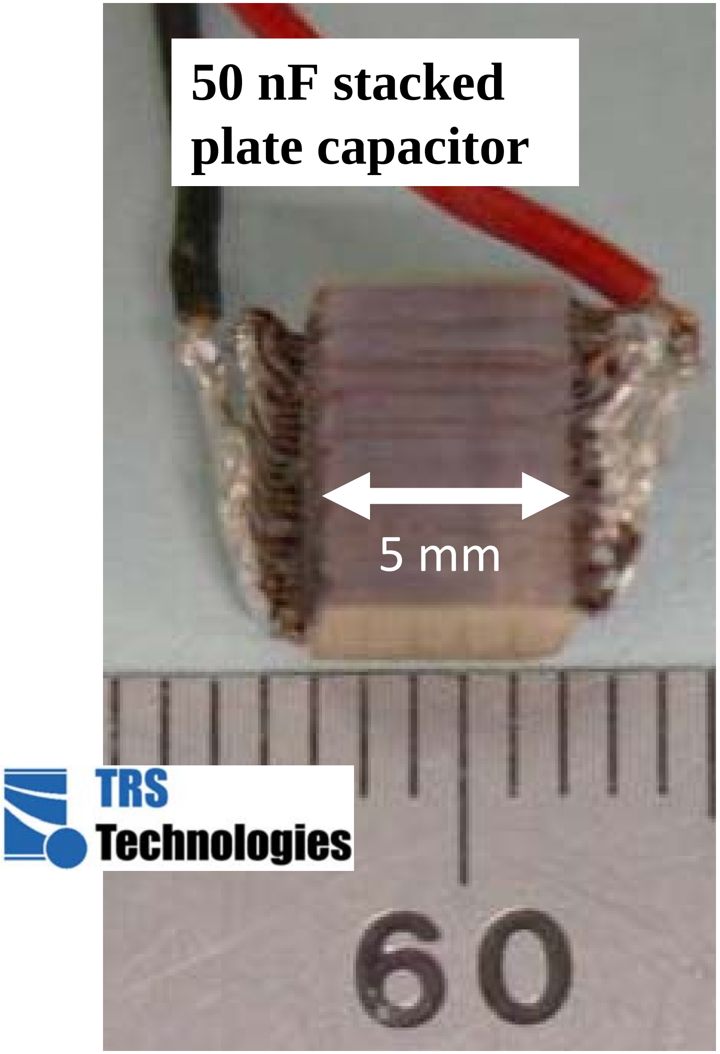
- Demonstrate that commercial display glass is suitable as a high temperature dielectric.
- Establish fabrication technology for glass sheet for DC bus capacitors.
- Develop reliable high-temperature capacitor by highly accelerated life testing and establish benign failure modes in the glass capacitor.

Technical Accomplishments – Glass Ceramics

High Energy Density from
Glass-Ceramic Plate made at Penn State



Glass Ceramic Data from Wes Hackenberger TRS Technologies



Future Work – Glass Ceramics

Glass Ceramics:

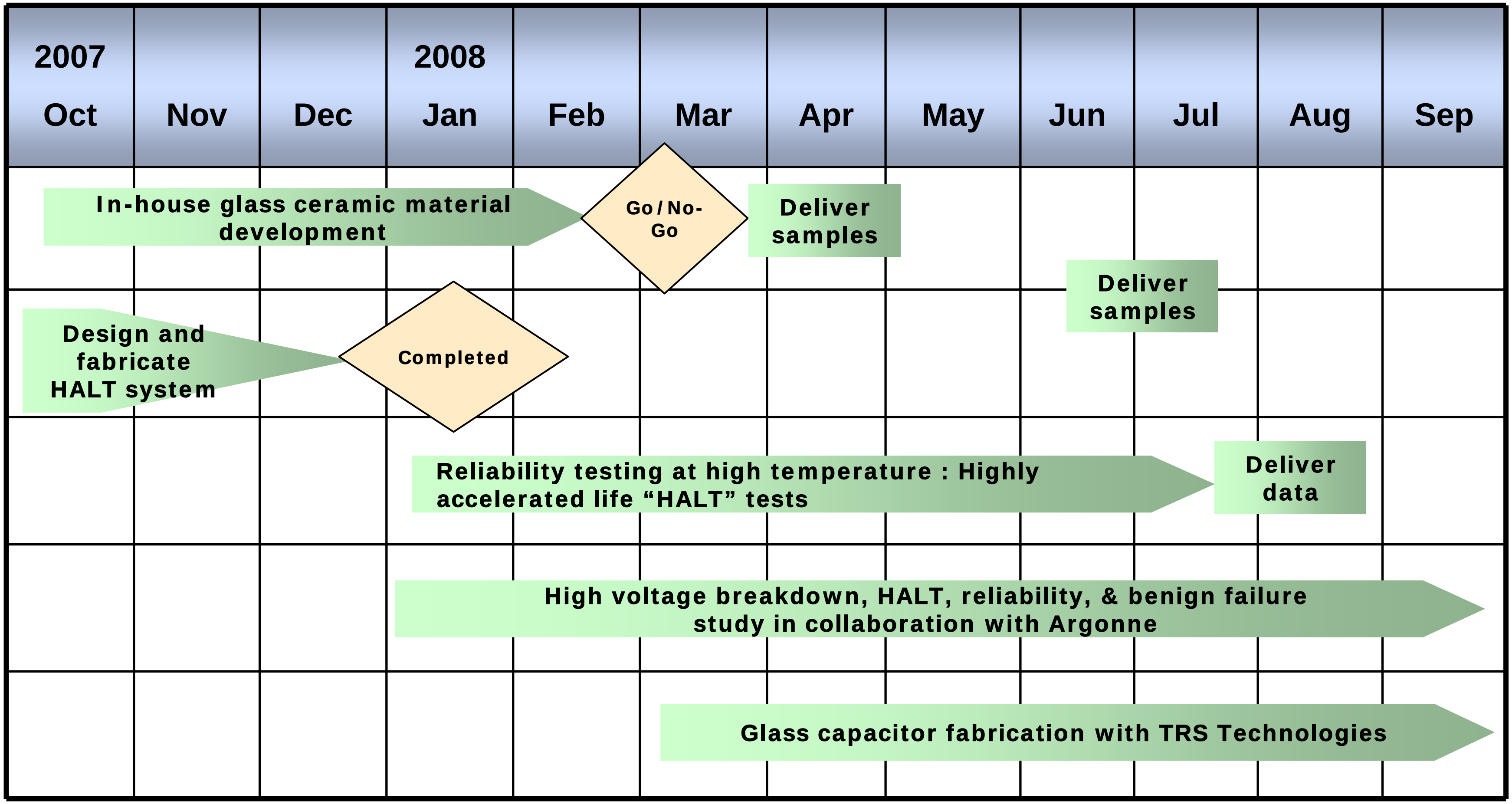
FY09

- Collaborate with glass manufacturers to ensure that 10 micron flat panel display glass has adequate electrical properties.

FY10

- Build and test full multilayer capacitors in collaboration with TRS Technologies.

Timeline for FY 08 – PSU's Glass Capacitor Approach



High Temperature Film Capacitors

Shawn Dirk
Email: smdirk@sandia.gov
Phone:505-844-7835
Organization: Sandia National Laboratories

Project Duration: FY 2006 – FY 2010

FY 2008 Funding: $100K

DOE Vehicle Technologies Program
Advanced Power Electronics and
Electric Machines Projects
2008 DOE OVT Annual Merit Review Meeting

Bethesda North Marriott
Bethesda, MD

February 28, 2008

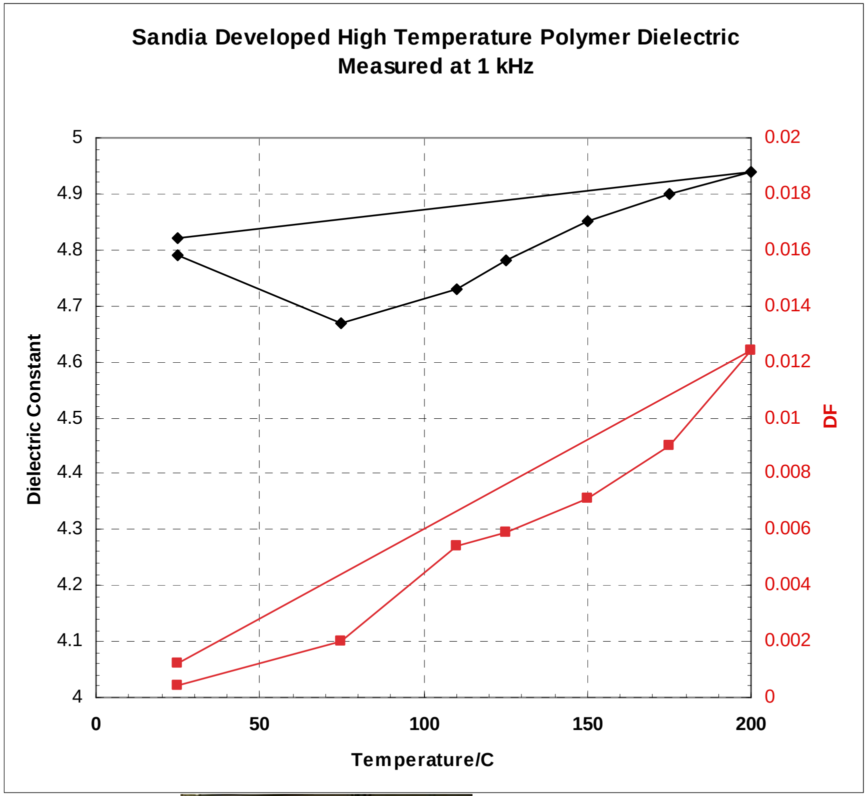
This presentation does not contain any proprietary or confidential information

Uniqueness of Project and Impact – Polymer Films

•Developed a polymer film with k = 5 and DF < 0.01 over a temperature range from RT to 200 °C. Demonstrated the fabrication of large (8.5" x 11") sheets of 2 um thick polymer film.

•Capacitors generated using the Sandia developed material will be ½ to ¼ of the size of the current capacitors used in a HEV inverter. The new capacitors will have a larger operational temperature range (>150 °C)

•Initiated collaboration with Electronic Concepts Inc. (ECI) to produce prototype capacitors



Electrical characterization of a flexible polymer film produced using drawdown technique

Sandia National Laboratories

Electronic Concepts, Inc.

Technology Related Challenges/Barriers

Polymer Film Capacitors:

- An outside synthesis house may be required to generate the Sandia developed polymer depending on the polymer quantity needed to produce prototype capacitors

  - Collaborate with industrial partners (ECI)

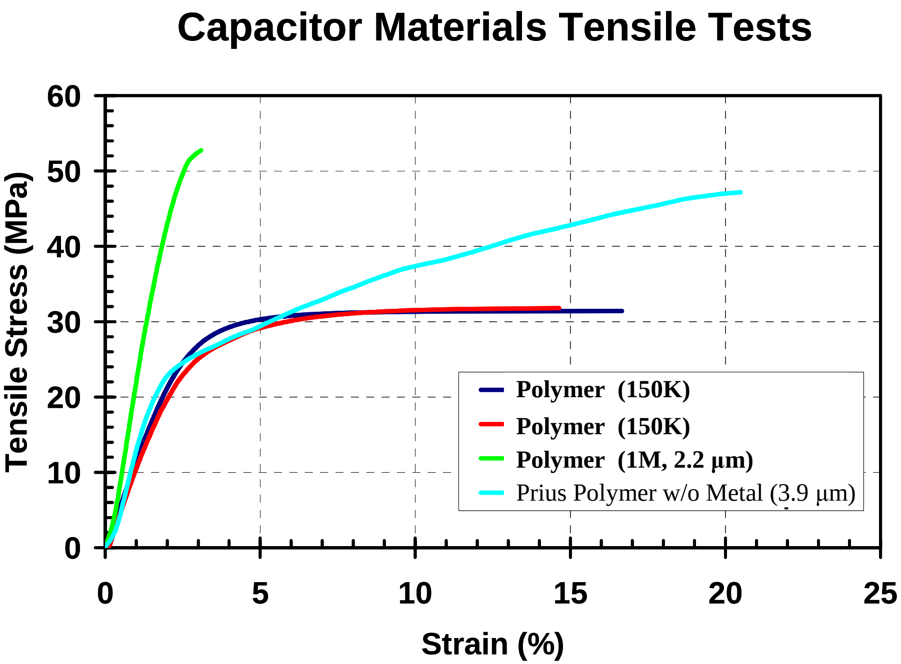
Technical Approach for FY08

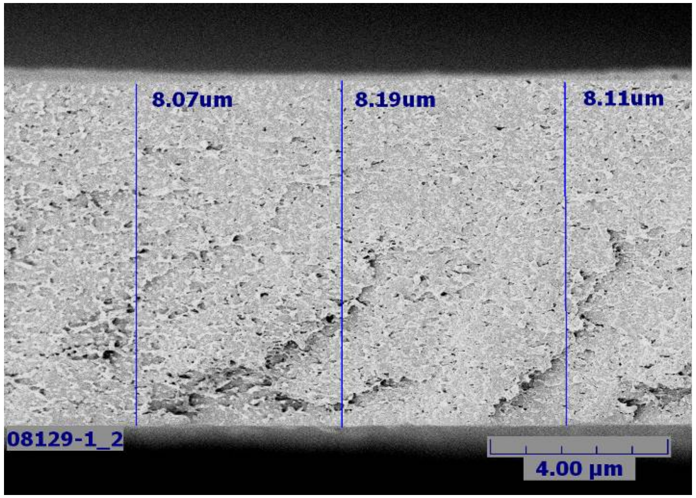
Polymer films:

- **Optimize film stoichiometry, scale up synthesis, and fabricate prototype capacitors.**

Technical Accomplishments – Polymer Films

- Electrical characterization of a free standing Sandia developed polymer from room temperature to 200°C
- Demonstrated lab scale production of polymer films of 2 µm thickness (11” x 16”) using solution casting drawdown techniques
- Evaluated film uniformity and porosity using SEM characterization techniques





- Completed mechanical characterization of a free standing Sandia developed polymer and compared the material to the Toyota Prius® dielectric material
- Sent Samples to the ARL for independent evaluation

Future Work – Polymer Films

Polymer Films:

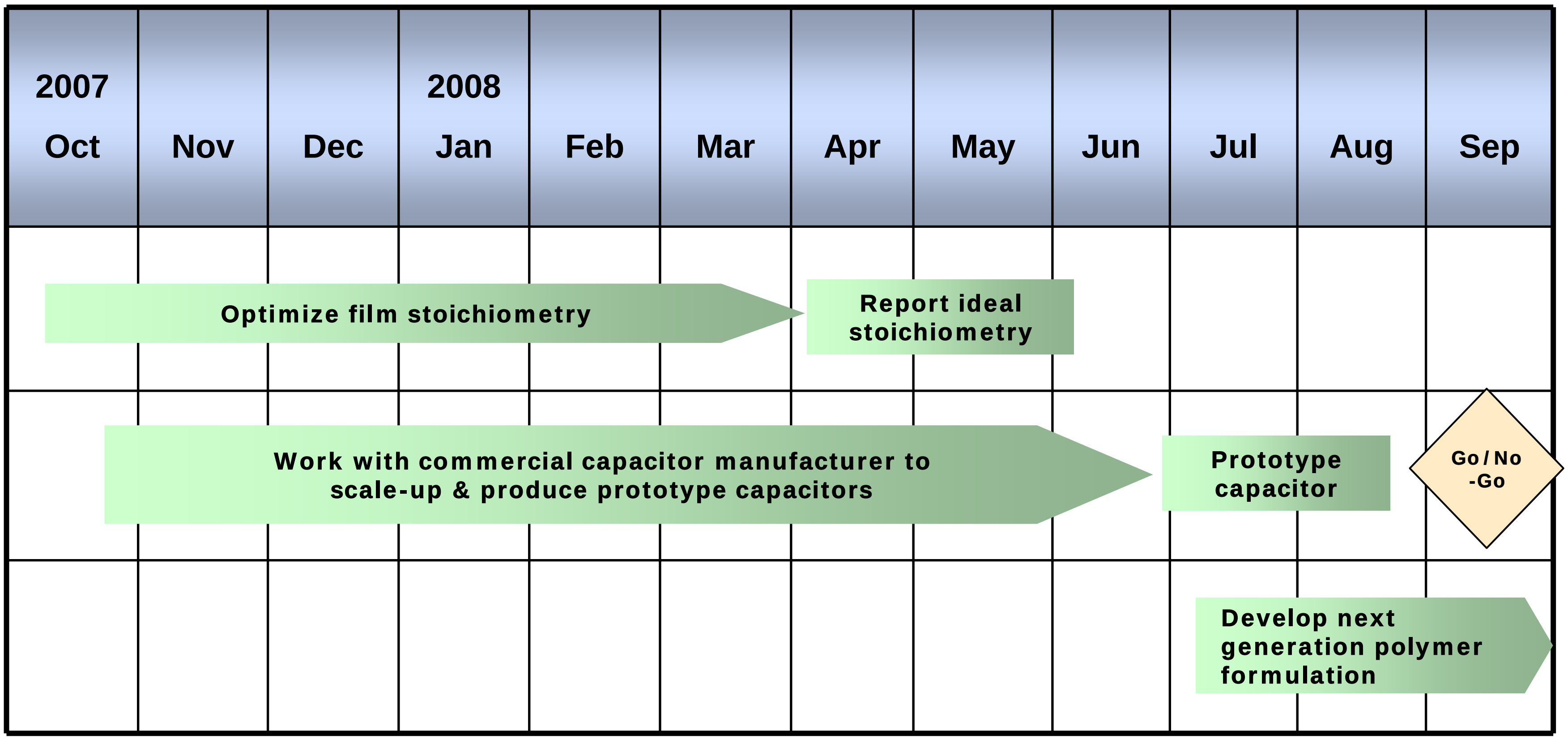
FY09

- Fabricate prototype capacitors with next generation polymer formulations (maintain high dielectric constant value (≈5) and low DF (<0.01) while doubling breakdown voltage), commercialization of current polymer formulation based capacitors.

FY10

- Commercialization of next generation polymer formulation based capacitors.

Timeline for FY 08 – Sandia's Polymer Film Approach



Capacitor R&D Summary

Potential for petroleum displacement:

- Developing new, high performance, economical capacitor technologies for hybrid electric vehicles power electronic systems. Hybrid electric vehicles will help to achieve petroleum displacement requirements.

Approach:

- Three-pronged approach, namely, embedded film-on-foil dielectric, glass ceramic, & polymer film, are followed to reduce size, weight and cost of power electronic capacitors concomitant with increased performance & reliability.

Technical accomplishments:

- Fabricated film-on-foil dielectrics with k = 1400, breakdown field ≈ 2.5 MV/cm, cap density ≈1.5 µF/cm^2, & leakage current < 10^{-6} A/cm^2. Thermally cycled (about 1000 times) between -50°C and +150°C with no measurable degradation in k.

- Fabricated high dielectric constant glass ceramics with excellent flexibility; developed glass coatings for benign failure; loss factor <5% up to 270°C.

- Developed polymer films with k=5 and loss factor <1% up to 200°C; demonstrated fabrication of large (8.5” x 11”) sheets of 2 µm thick polymer film.

Capacitor R&D Summary (cont'd)

Technology Transfer:

- Argonne has established a CRADA with Delphi to develop capacitors for high temperature inverters for HEVs, PHEVs, and FCVs.
- Penn State is collaborating with Corning & Schott Glass to adapt large-scale flat panel display manufacturing to capacitors and with TRS Technologies to build & test multilayer capacitors.
- Sandia is working with ECI to demonstrate and characterize capacitors made with the Sandia developed material.

Plans for next Fiscal Year:

- Fabricate large number of large area film-on-foils defined by the inverter application requirements for embedding into inverter circuit boards.
- Test fabrication methodologies & compositions for enhanced performance.
- Collaborate with glass manufacturers to ensure that 10 μm flat panel display glass has adequate electrical properties.
- Fabricate prototype capacitors with next generation polymer formulations.

Selected Publications, Presentations, Patents

1. Chemical Solution Deposition of Ferroelectric Lead Lanthanum Zirconate Titanate Films on Base-Metal Foils, B. Ma, D. K. Kown, M. Narayanan, and U. Balachandran, J. Electroceram (in press, 2008).
2. Synthesis and Electrical Properties of Stabilized Manganese Dioxide Thin Film Electrodes, D. K. Kown, T. Akiyoshi, H. J. Lee, and M. T. Lanagan, J. Amer. Ceram. Soc., (in press, 2008).
3. Chemical Solution Deposition of $LaNiO_3$ on Ni Metallic Substrate for Ferroelectric $(Pb_{0.92}La_{0.08})(Zr_{0.52}Ti_{0.48})O_3$ Thin Film Capacitors, K. K. Uprety and D. Y. Kaufman, Submitted to Thin Solid Film, 2007.
4. Ferroelectric Thin Films on Base-Metal Foils for Embedded Passives, B. Ma, D. K. Kwon, M. Narayanan, and U. Balachandran, Mater. Res. Soc. 2007 Fall Meeting Symp. Proc.; Boston, MA; Nov 25 - 30, 2007.
5. AntiferroelectricThin Films for Embedded High-Energy Density Capacitors, D. K. Kwon, B. Ma, M. Narayanan, and U. Balachandran, IMAPS Advanced Technology Workshop on Integrated/Embedded Passives, San Jose, CA, Nov. 15-16, 2007.
6. Synthesis of Manganese Oxide Thin Films for Capacitor Electrodes, D. K. Kwon, T. Akiyoshi, and M. T. Lanagan, 31st International Cocoa Beach Conference & Exposition on Advanced Ceramics & Composites, Daytona Beach, Florida, Jan. 12-16, 2007.
7. Preparation and Characterization of Dielectric Glass-Ceramics in Na_2O-PbO-Nb_2O_5-SiO_2, J. Du, B. Jones, and M. T. Lanagan, Mater. Lett., 59, (22), 2821, 2005.
8. Ceramic Capacitor Exhibiting Graceful Failure by Self-Clearing Method for Fabricating Self-Clearing Capacitor, D. Y. Kaufman and S. Saha, U.S. Patent 7,099,141, Aug. 29, 2006

Questions

Back-up slides

Capacitor Challenges

	Future Capacitor Bank Requirements
Capacitance, μF	**2000+/- 10%**
Voltage rating, VDC	**600**
Peak transient voltage for 50 ms	**700**
Leakage current at rated voltage, ma	**1**
Dissipation factor, %	**<1**
ESR, mohm	**<3**
ESL, nH	**<20**
Ripple current, amp rms	**250**
Temperature range of ambient air, ºC	**-40 to +140**
Weight requirement, kg	**0.8**
Volume requirement, L	**0.4**
Cost	**$30**
Failure mode	**Benign**
Life @80% rated voltage	**>10,000 hr, 20 amps rms, +85ºC**

Project Relevance – Problems that this project addresses

Feature	Specification	Capacitor Program Contributions
Weight & Volume	**0.8 Kg/0.4 L**	**Embed into printed circuit board** **High cap density & breakdown voltage**
Voltage	**600 V**	**High breakdown strength**
Capacitance	**2000 μF**	**High dielectric constant materials**
Temperature	**140°C**	**High temperature dielectric materials**
Ripple Current	**250 Amp**	**Low dielectric loss and ESR, high temperature performance**
Failure Mode	**Benign**	**Graceful failure mechanism**
Cost	**$30**	**Low cost materials and processes**

Technical Approach for FY08 - Argonne
(Two parallel approaches)

Continue development of core film-on-foil technology

- **PLZT on Ni foil**
- **LNO buffer layer**
  - **Avoids any parasitic interfacial effects » high κ**
  - **Provides smooth interface » high E_b, low tan δ**
- **Dielectric constant of ~1400 C/A = 1.5 µF/cm^2**
- **Voltage ~600 V E_b= 2.5 MV/cm**
- **Leakage current density <10^{-6} A/cm^2**

- **PLZT on Cu foil**
- **Better compatibility with Printed wire board manufacture process**
- **Low oxygen pressure (pO_2) processing required to avoid oxidation and parasitic interfacial effects**
- **Encouraging initial results**
- **Precursor solution with better compatibility with low pO_2 process**

Justification for Parallel Approaches

Goal: Thin film with excellent dielectric properties in architecture that is compatible with printed circuit board manufacturing processes

PLZT on Ni foil

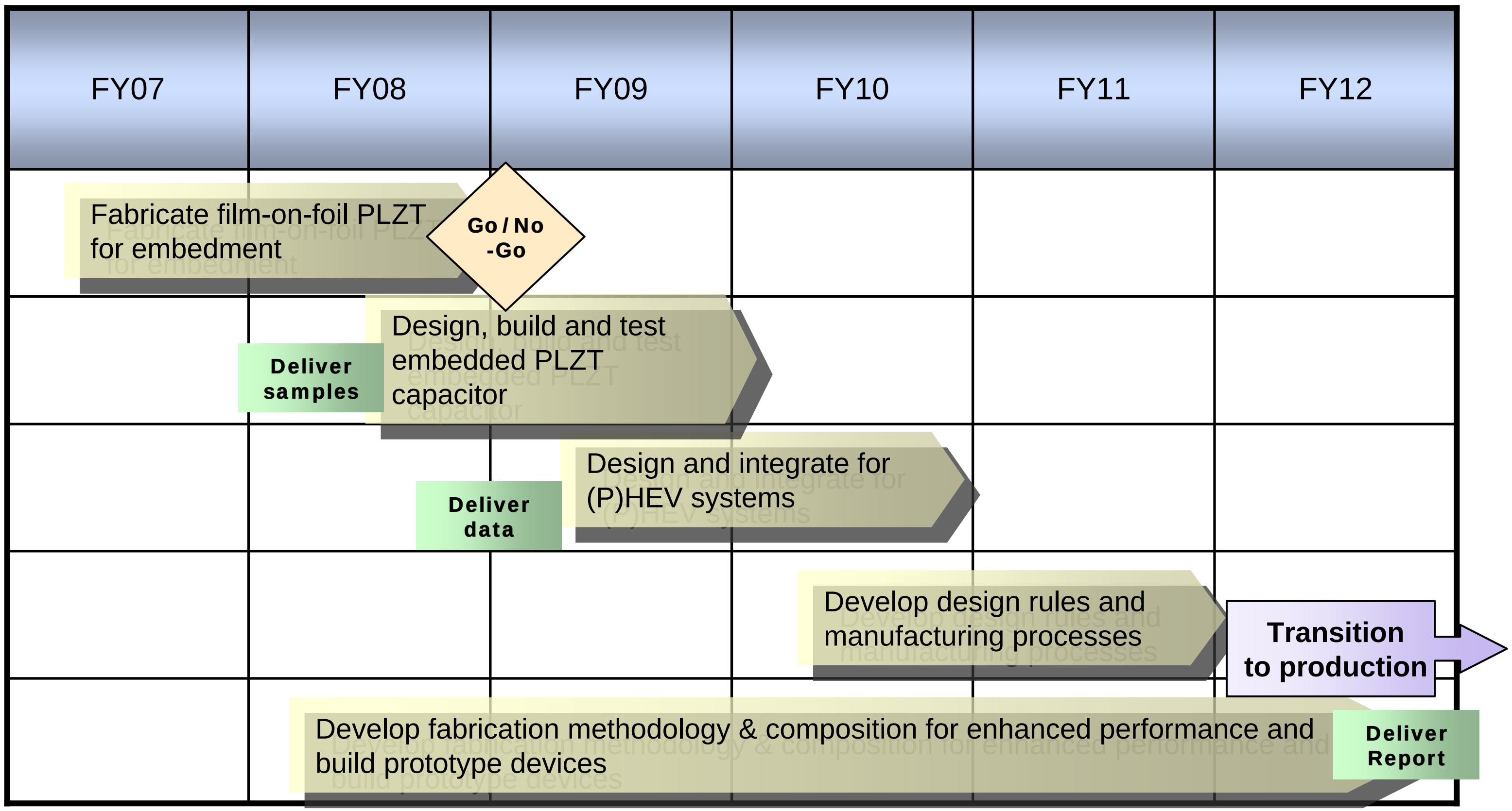
- **Excellent dielectric properties have been demonstrated**
- **Additional processing steps must be developed to ensure its compatibility with printed circuit board manufacturing processes**

PLZT on Cu foil

- **Compatible with printed circuit board manufacturing**
- **Dielectric properties are encouraging but require further development**

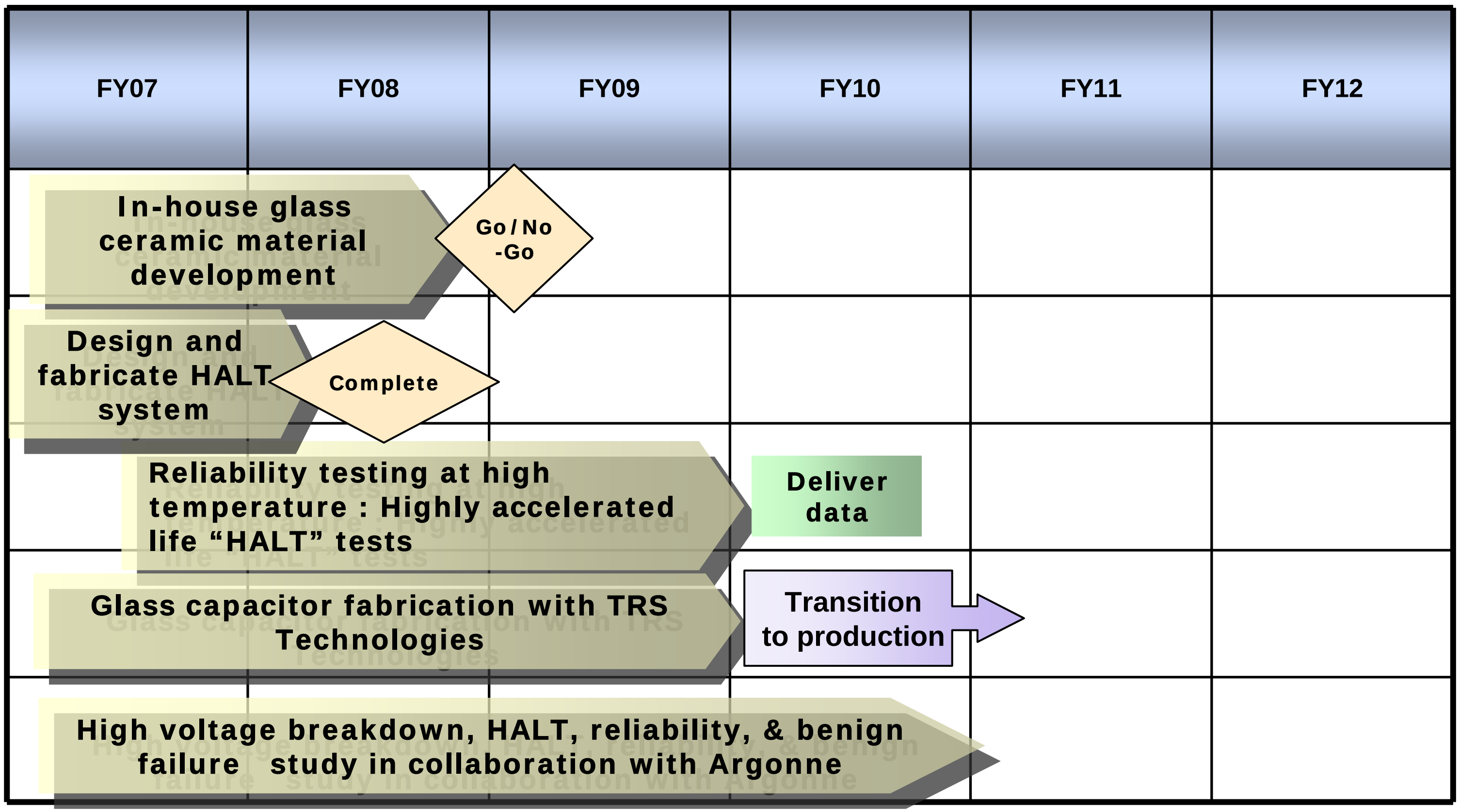
Conclusion: Both architectures are promising but require further development for different reasons. It remains to be seen which approach will ultimately bring us to the goal!

Timeline for Argonne's Embedded Cap Approach



Decision point: Either continue the two-pronged approach, i.e., PLZT/Ni and PLZT/Cu, or down-select one over the other.

Timeline for PSU’s Glass Capacitor Approach



Timeline for Sandia's Polymer Capacitors