Direct-Cooled Power Electronic Substrate

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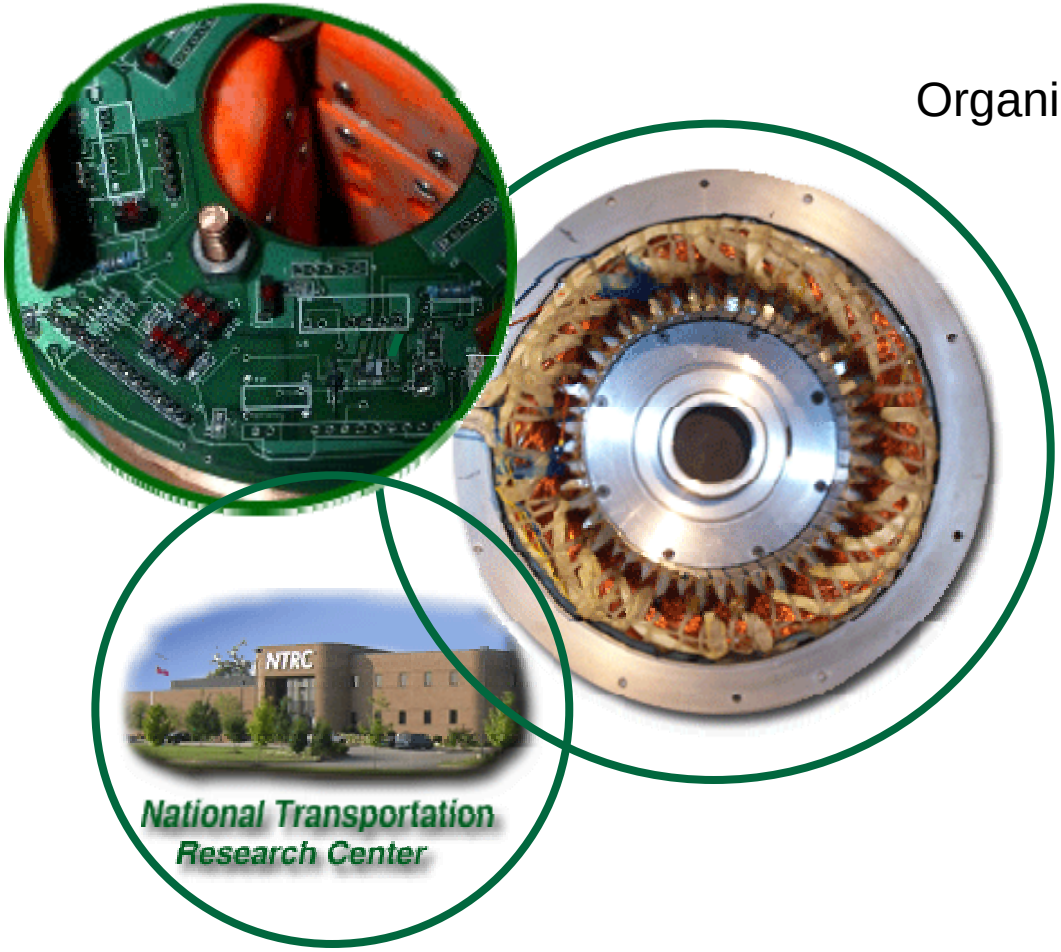


Principal Investigator: Randy Wiles
Agreement: 13296

Project Duration: FY08 to FY10
FY08 Funding: $349K

DOE Vehicle Technologies Program
Overview of DOE VTP APEEM R&D

North Marriott Hotel and Conference Center
Bethesda, Maryland

February 28, 2008

Purpose of Work

- **Develop power electronics substrate that is directly cooled**
  - Reduce size, weight, and cost of PE
  - Use silicon (Si) devices with 105°C coolant

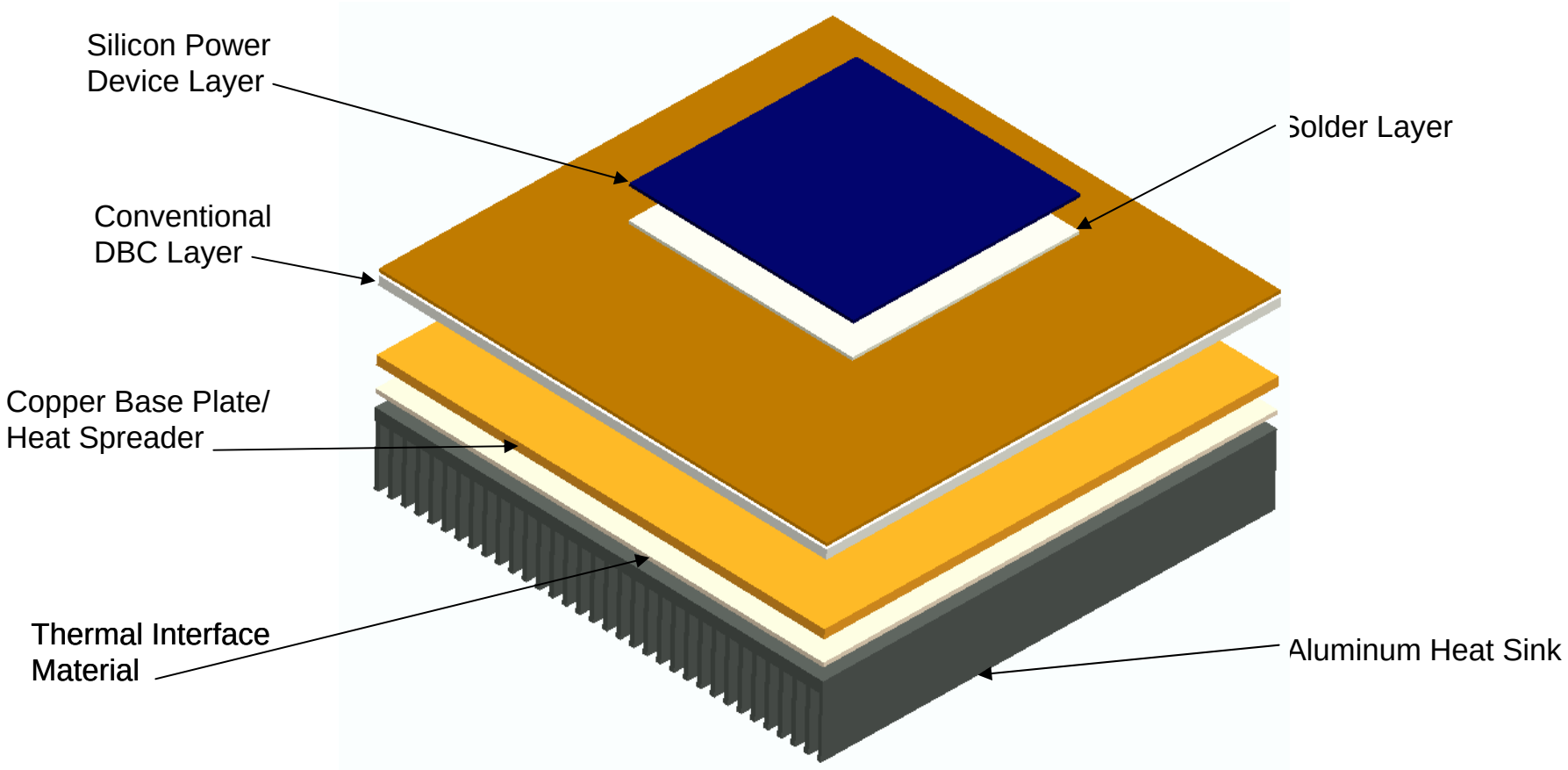
Response to Reviewer's Comments

This is a new start in FY08; no previous review has been conducted

Barriers

VTP Activities Related Challenges

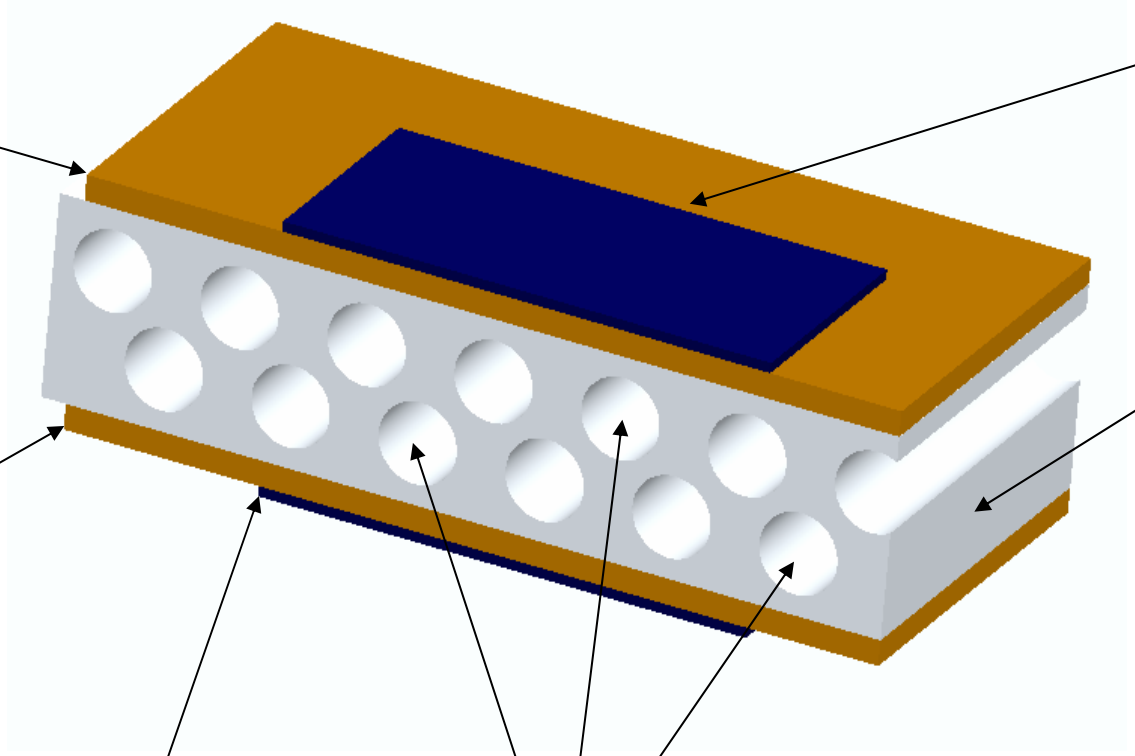
Conventional cooling methods for power electronics are typically based on conduction cooling through solids directly adjacent to the power devices.



The resistive cooling path limits volume, weight, and cost reductions.

Technical Approach

Proposed concept replacing conventional method of inverter heat removal.



Potential power density of >15 kW/L with 105°C coolant using Si devices

Technical Approach - Uniqueness

- Reduction of the heat sink size requirement will reduce the cost, mass, and volume of inverter and greatly simplify manufacturing
- Reduced thermal resistance should enable the use of 105ºC coolant for silicon-based electronics resulting in cost reductions; additional system cost savings of about $175 accrue by eliminating 70ºC standalone cooling loop
- Three dimensional inverter packaging and eliminating the heat exchanger volume by directly cooling the DBC result in compact, light weight design

Barriers

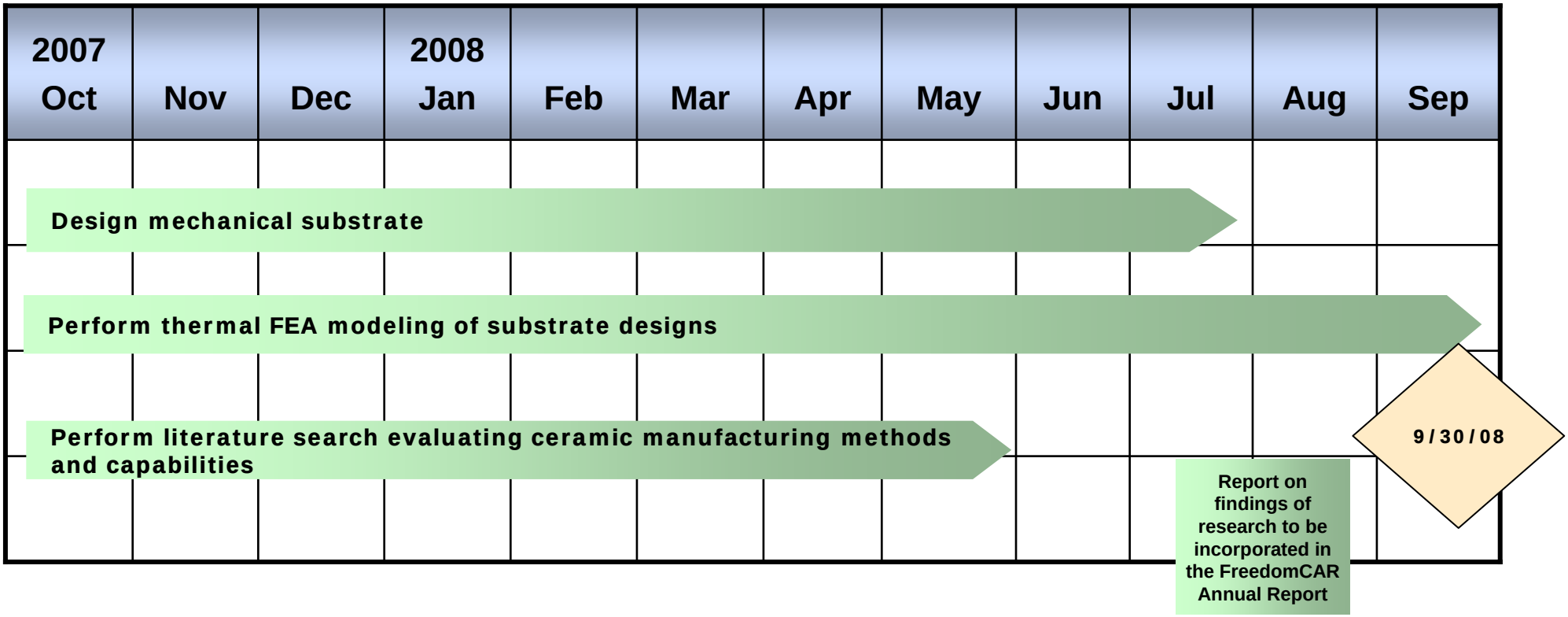
Technology Related Challenges

- Sealing of Substrates – Protection of electronics from coolant paths
- Material Compatibility – Compatibility of the substrate material with water/ethylene glycol
- Thermal Growth – Stress levels inside substrate under thermal load
- Ceramic Manufacturing Techniques – Low-cost ceramic manufacturing for substrate

Technical Approach FY08

- Mechanical modeling of substrate and inverter core designs
- Thermal Finite Element Analysis modeling of the substrate designs
- Research manufacturing capabilities and methods that will support the substrate designs
  - Collaborating with ORNL's Metals & Ceramics Division to determine the compatibility of the material with water/ethylene glycol
  - Researching the thermal issues of the selected substrate material for spalling and how thermal growth of the material impacts the contact bond strength

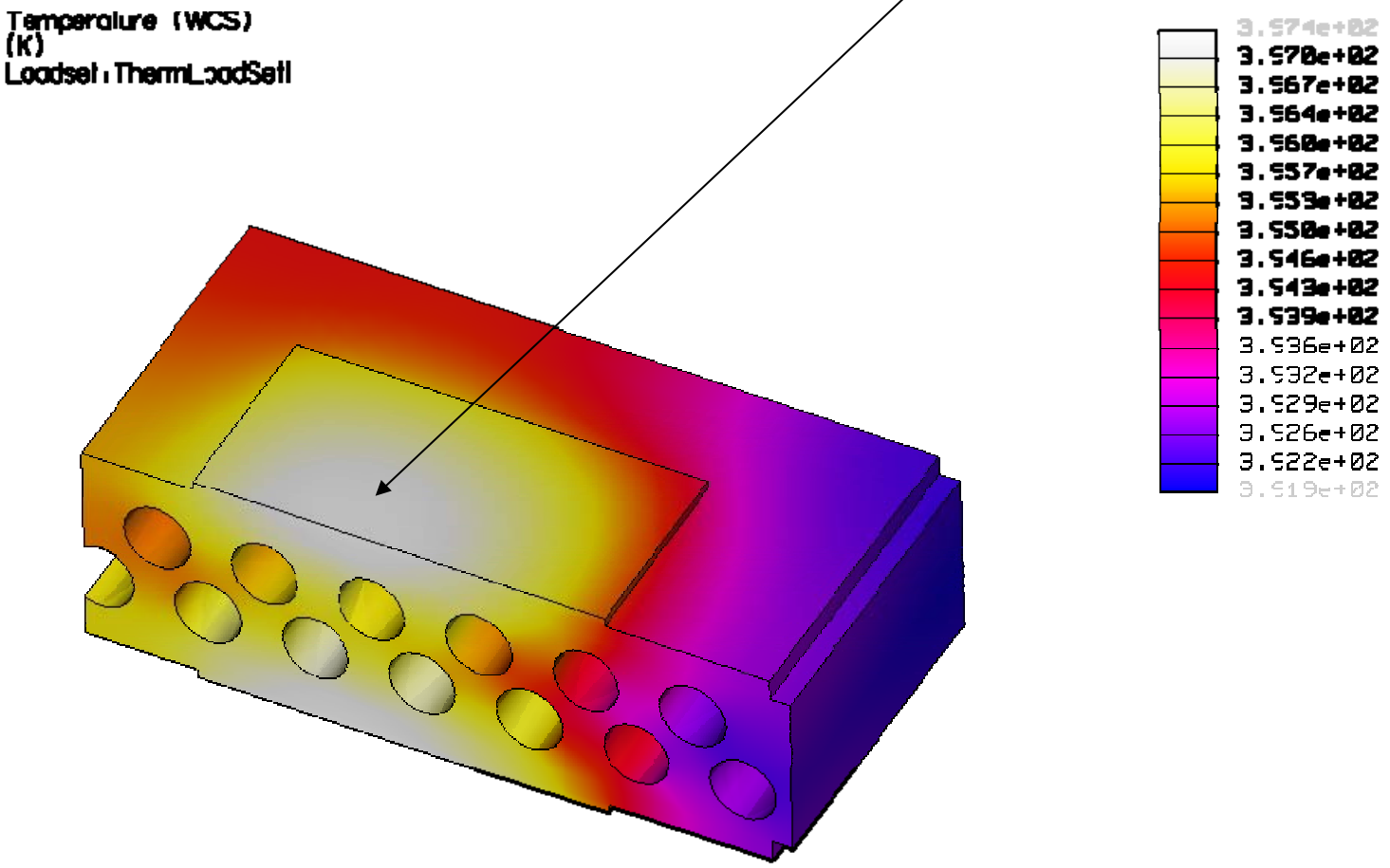
Timeline for FY08



Decision point discussion: If modeling of substrate designs indicated positive results, move forward to prototyping stage (9/30/2008).

Technical Accomplishments FY08

Thermal Model Showing 125°C (397°K) Chip Core Temperature Is Possible



Technical Accomplishments FY08 (cont'd)

- Several design concepts have been generated
- Preliminary thermal analysis indicates maximum chip temperatures well within Si trench IGBT capability
- Performing stress analysis and detailed thermal evaluations
- Preliminary estimates of inverter performance parameters
  - Specific power >20 kW/kg
  - Power density >15 kW/L

Technology Transfer

- This technology would support inverter/converter technology for all transportation applications
- Results are being shared with EETT
- Supplier base will be included once hardware has been demonstrated

Future Work

- FY09
  - Downselect design
  - Fabricate and test to validate performance
- FY10
  - Refine design using FY09 test results
  - Build and test this next generation in an operating inverter prototype

Summary

- A key barrier to achieving PE targets is the ability to remove heat from the power chips
- The direct-cooled substrate concept offers the possibility of using Si power devices with 105°C coolant
- Significant decreases in weight, volume, and cost are potentially possible
- FY08 efforts will establish technical feasibility of the concept; FY09 will focus on fabrication and testing of experimental inverter

Publications, Presentations, Patents

- Randy H. Wiles, “Direct-Cooled Power Electronics Substrate,” presented at DOE FreedomCAR and Vehicle Technologies Program APEEM FY08 Kickoff Meeting, November 8, 2007.

Questions