Development, Test and Demonstration of a Cost-Effective, Compact, Light-Weight, and Scalable High Temperature Inverter for HEVs, PHEVs, and FCVs

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Project Overview

Timeline

- Start: Oct. 2007
- Finish: Mar. 2011
- Approx. 40% complete

Budget

- Total project funding
  - DOE: $4.952M
  - Contractor: $3.258M
- DOE funding to date
  - $2.693M (FY08 & FY09)
  - FY09 shortfall: $350k

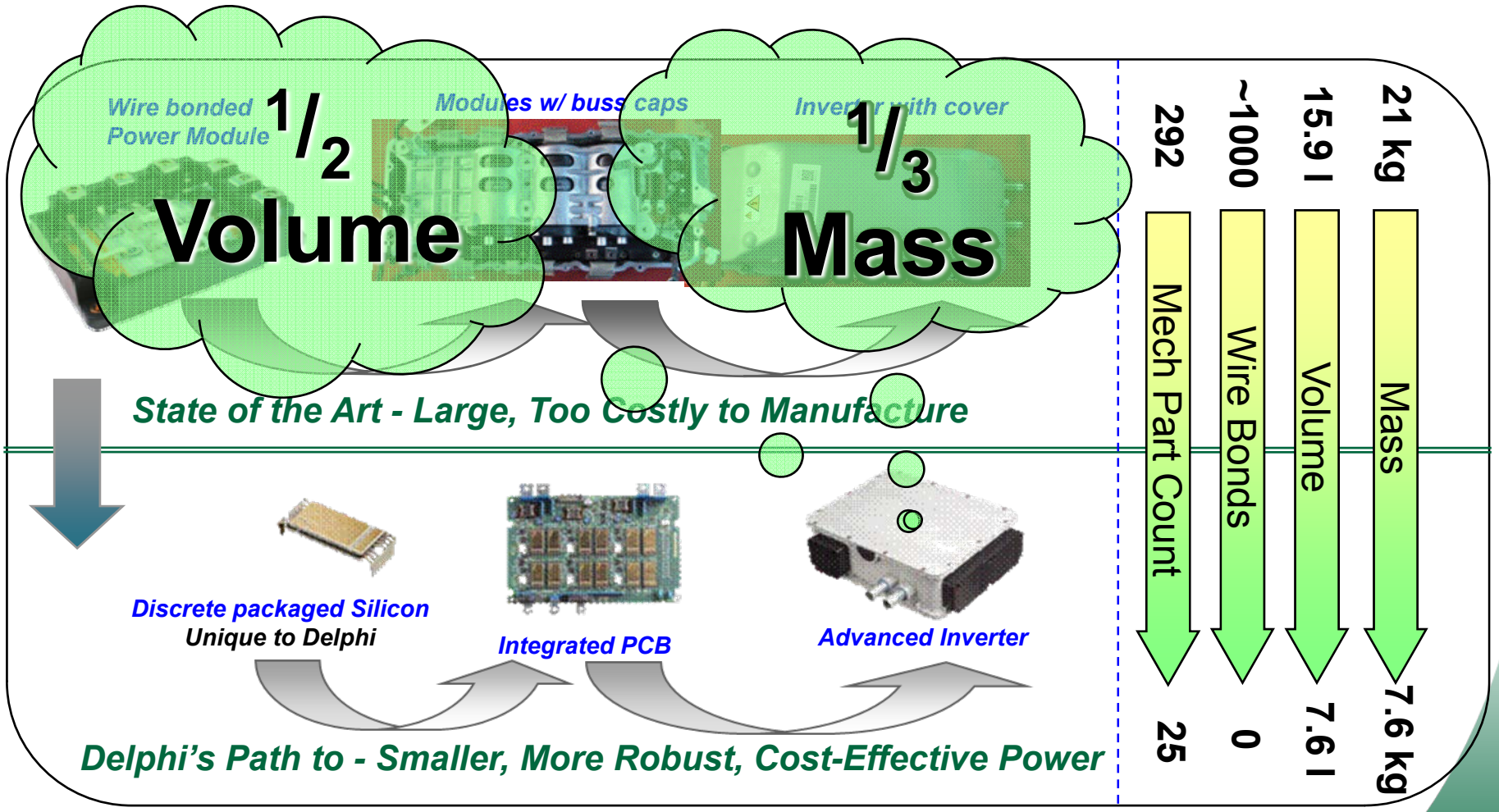
Barriers

- Reduce system cost by 50% ($275)
  - Compatible with engine coolant (105°C), volume manufacturing, and scalable
- Reduce system volume by 50% (4.6 L)
- Reduce system weight by 50% (4.6 kg)

Partners

- Delphi: Project lead
- Dow Corning / GeneSiC: SiC-on-Si power semiconductor devices
- GE: Film capacitors
- Argonne NL: Film-on-foil capacitors
- ORNL: System modeling/simulation, power device characterization, system testing
- NREL: Thermal modeling

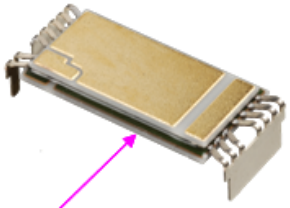
Objective: Reduce Cost, Volume and Mass and be Compatible with High Volume Manufacturing



Milestones for FY08 and FY09

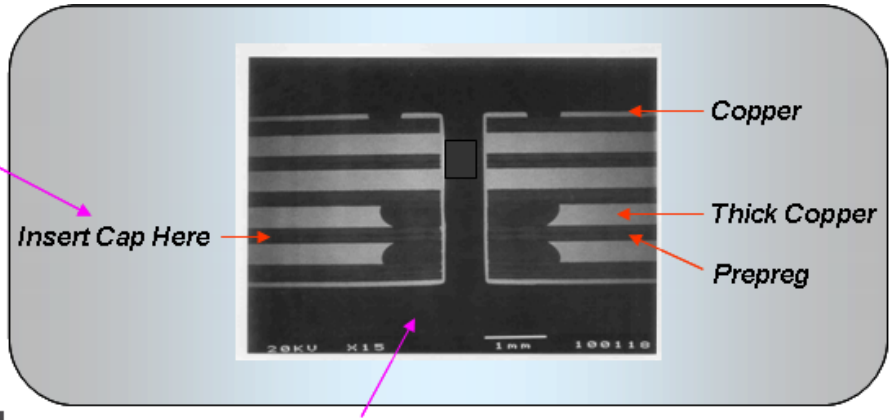
Month/Year	Milestone or Go/No-Go Decision
Dec-08	**Go/No-Go Decision** Key technology concepts identified and tested using a combination of laboratory or virtual testing, evaluated, prioritized, presented to DOE, and finally approved by DOE for development and integration in Phase II.
Jun-09	**Milestone: Mid-Phase IIA progress review** Review of Delphi's Task 4 progress to design, build and test selected component concepts, and to develop inverter concepts. Lab testing of prototype components, process documentation, and updated component performance and cost models will guide Delphi's updating of its inverter system cost and performance projections.
Dec-09	**Milestone: Review with DOE of bench-level testing** Review demonstrates to DOE component concepts capable of meeting DOE requirements when integrated into an inverter in Phase IIB (Budget Period 3).

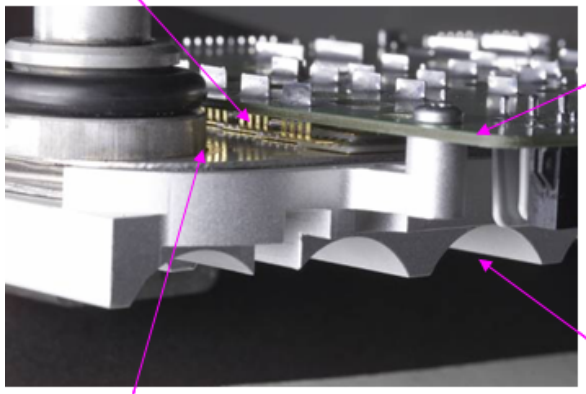
Technical Approach



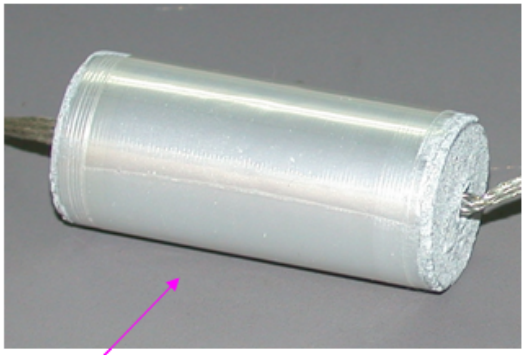
Embedded Cap

Discrete Power Switch Si or SiC





High Current FR4



High Convection Coefficient Heat Exchanger

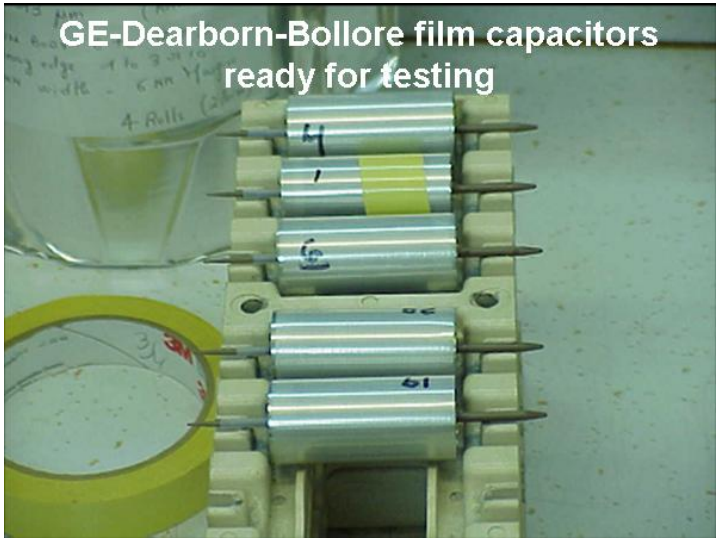
Film Cap

Technical Accomplishments/Progress/Results: Film Capacitors (GE)

- Materials / Processing
  - A laboratory extrusion cast line was designed to prepare thin films of polymeric resins.
    - Line used to make polycarbonate (PC) and polyetherimide (PEI) films of only a few microns thickness. These films showed capacitor-grade properties.
  - PC and PEI resins of high glass transition temperatures were prepared from novel monomers, using straightforward preparation methods.
    - Resins showed a superior dielectric constant compared with similar commercially available materials
    - The high-heat PC resin will be scaled up for more extensive testing. This technology has been previously submitted for patenting
  - Several promising thin film materials have been identified.
    - Several analytical techniques were used to characterize these films for capacitor applications
  - Now optimizing candidate films and processing for low cost, volume production
    - A 6um thick PC film was made using a manufacturing-scale extrusion line. This film showed good properties. It will next be metallized and used to build capacitors.
- Capacitor Testing
  - A laboratory set-up has been assembled to test electrostatic film capacitors at different temperatures (-55°C to 200°C), frequencies (50Hz to 2MHz), and voltages (0V to 600VDC).
  - Equipment used to test several 2mF and 25mF capacitors manufactured from a metallized 13um thick PEI film made using same method developed in lab to stretch polymers into films

Project Objective for FY09:
Film Capacitors (GE)

- **Produce Proof-of-Concept (POC) capacitors with 3um PEI film**
  - **Test to specifications**
- **Verify High Dk, High Temperature Polycarbonate (PC) can be made into a film cost effectively (via extrusion)**
  - **Small scale film trials**
  - **Scale-up to larger scale sufficient for making POC capacitors**
  - **Target is ≤ 6um thickness**
  - **Produce POC capacitors**



Technical Accomplishments/Progress/Results:
Film-on-Foil Capacitors (Argonne)

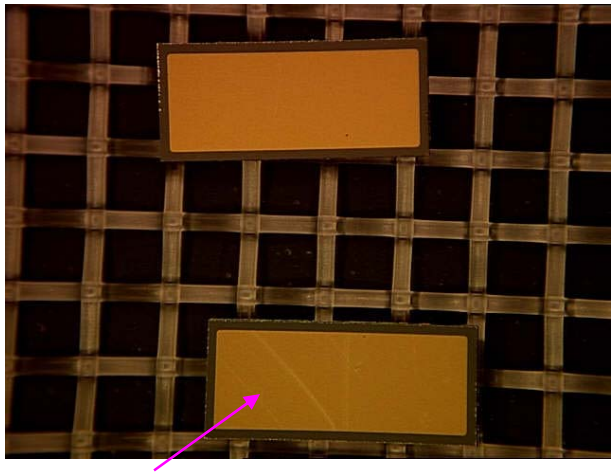
- Process demonstrated shows embedding can be accomplished
- Dielectric constant > 1000 verified
- Benign failure – verified as a single layer cap (with no interconnects)
- Progress made toward forming a large-area capacitor
  - Unable to demonstrate Phase I goal of 1” x 1” cap followed by 2” x 2”
  - Defects partially diagnosed
    - As caps get physically larger, defects increase (pinholes, cracks, contaminates)
    - Many defects seem to originate from the metal foils
    - Process needs a clean room environment and more controls at each step
    - Metal foils need to be polished to reduce pits, cracks, hard inclusions
- Good progress made toward understanding cost (vs. DOE targets)
  - Material cost of PLZT is inexpensive
  - Material cost of Ni substrate – currently too high, due to required polishing
  - Production process – needs clean room environment
- Stress-strain better than expected (possible additional opportunity)

Technical Approach FY09:
Film-on-Foil Capacitors (Argonne)

- **Fabricate larger-area capacitors**
  - **Possibly use semiconductor processes to fabricate capacitor**
    - **Delphi assisting in analysis**
  - **Utilize printed Ni or other metal substrates**
- **Transfer process as it exists today to a clean room environment**
  - **Add process controls: inspect substrate before/after each process step**
- **Lower # of process steps to minimize cost, improve quality control**
  - **Print thicker layers**
    - **Currently spin coating approximately 0.1um/layer**
    - **Target 1um/layer**
- **Consider non-embedded alternatives for film-on-foil approach**
  - **Non-embedded approach may be better near-term approach for earlier commercialization, and important step toward embedded approach**

Technical Accomplishments/Progress/Results: 3C-SiC (Dow Corning)

- **Completed models to direct device designs for 200A / 600V diodes and MOSFETs based on SiC-on-Si**
  - Modeled temp dependent I-V characteristics, switching, T=25-150ºC and supplied data for inverter modeling simulations
  - Completed initial designs for diode and MOSFET
- **New CVD epitaxy system installed and facilitized. Positive early results:**
  - 3C-SiC epitaxy up to 10um thick demonstrated on 100mm Si wafers
  - Demonstrated crystal quality matching prior DCC work on small substrates (1995-2000)
  - Wafer bow reduced to acceptable level of <50um
- **Completed non-functional diode process flow (wafer thinning, metal, pattern, dice) using SiC-on-Si 100mm wafers**
  - Chips delivered for advanced package demonstration
- **Provided mechanical samples of diodes**
  - Fabricated initial diode samples into packages
  - Initial samples look promising, parts solder well
  - Need to mechanically evaluate metallization structure



SiC Diode Mechanical Sample

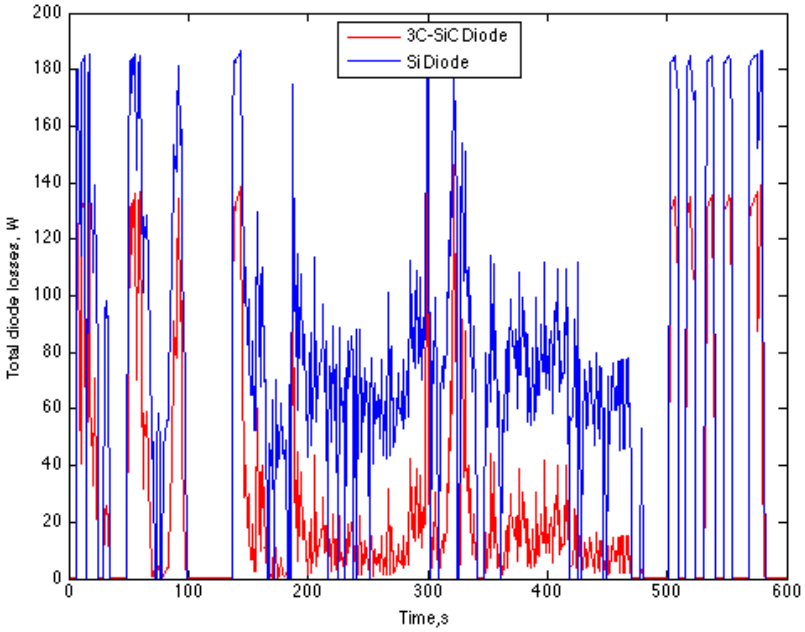
Technical Approach for FY09:
3C-SiC (Dow Corning)

Epitaxy and Device Fabrication/Testing Studies

- **Optimize temperature field and CVD epitaxy nucleation chemistry to suppress stresses incorporated into film during 3C-SiC growth**
- **Conduct studies of 3C-SiC critical properties to assess materials metrics and offsets from model assumptions**
  - Mobility as a function of temperature
  - Oxidation
  - Implant anneal and activation
- **Optimize design and complete first diode lot; test diodes**
- **Develop second generation diode design**

Technical Accomplishments/Progress/Results: Modeling/Simulation (ORNL)

- Completed assessment of inverter topologies to determine most beneficial in terms of cost, complexity and performance for a high temperature application
- Completed behavioral device level models
- Built a PM synchronous machine model
- Integrated inverter and motor model to construct a drive system for simulation analysis of Si and SiC device performance comparison



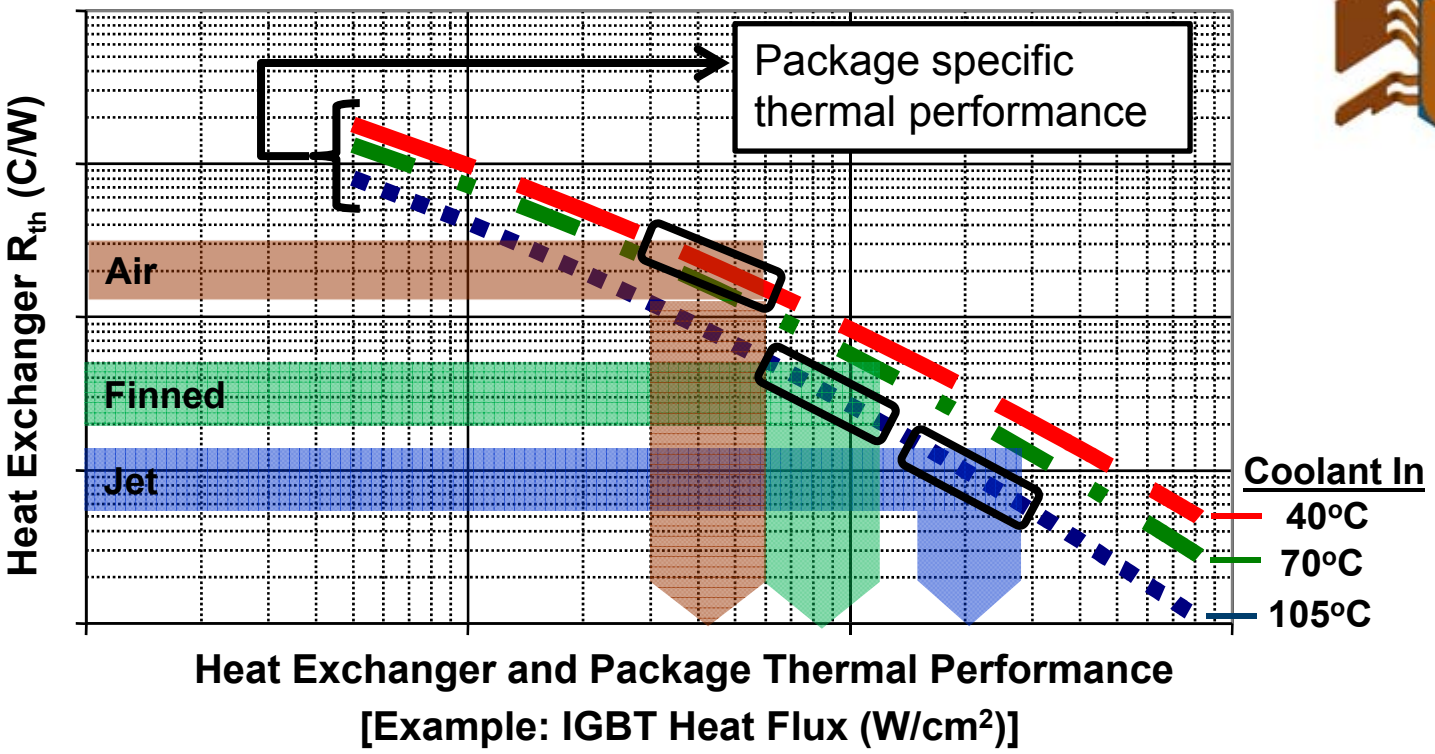
Simulated Diode Losses with Modeled SiC-on-Si vs Advanced Si Diode

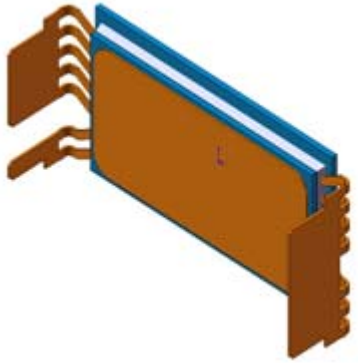
Project Objective for FY09:
SiC-on-Si Device Testing (ORNL)

- Characterization, testing and analysis of proof-of-concept 3C SiC-on-Si diodes
- Perform static testing on supplied 3C-SiC/Si diodes
- Perform dynamic testing on supplied devices, according to customer specification

Technical Accomplishments/Progress/Results:
Packaging and Integration (Delphi / NREL)

- **Delphi partnered with NREL to apply thermal system modeling techniques to advanced industrial design concepts, to assist with technology down-select process**





Project Objective for FY09:
Packaging and Integration (Delphi / NREL)

- **Optimization and robust design of down-selected heat exchanger technologies**
- **Experimental validation of optimized heat exchanger design**

Technical Accomplishments/Progress/Results:
Packaging and Integration (Delphi)

- **Alternative concepts assessed using Pugh Analysis**
  - **Have started the record of invention (ROI), patent process**

Concept #		Baseline	#1	#2	#3	#4	#5	#6	#7	#8	#9	#10	#11	#12	#13	#14	#15
Criteria																	
Quality/Reliability	4	0	1	-1	-1	0	-1	-1	1	-1	0	0	-1	-1	0	0	0
Cost	5	0	0		-1	-1	-1	-1	-1	-1	-1	-1	0	0	-1	1	1
Manufacturability	3.5	0	-1	-1	-1	-1	-1	0	0	-1	-1	-1	0	-1	-1	1	-1
Assembly/Repairability	2.5	0	0	-1	-1	0	-1	-1	0	-1	-1	-1	-1	-1	0	0	0
Thermal Performance	5	0	-1	1	1	-1	0	1	-1	1	-1	1	1	0	1	0	-1
Pressure Drop	2	0	1	0	-1	1	1	0	1	-1	1	0	-1	0	0	0	0
Creepage, Clearance, and	3	0	1	1	1	1	1	1	1	1	1	0	1	1	1	1	1
Size (Volume.)	2	0	-1	1	1	0	0	1	0	1	0	1	1	1	1	1	1
Size (Weight)	2	0	1	1	1	1	1	1	1	1	1	1	1	1	0	1	1
Scalability (building block)	3	0	0	0	0	0	0	-1	-1	-1	-1	-1	0	-1	-1	0	-1
Score		0	0.5	2	-5	-6.5	-8	-2.5	-2	-8	-12	-5	3.5	-6	-1.5	15.5	0.5

- **Worked with suppliers to develop world class Si IGBTs and diodes with solderable frontside and backside connections**
  - **Promising test results utilizing entire die surface for heat transfer**

Project Objective for FY09:
Packaging and Integration (Delphi)

- **Design, build, test selected component concepts & develop inverter concepts**
  - Design, build and test selected component concepts for power switches, DC buss capacitors, interconnects, high efficiency cooling subsystem, and mechanical packaging
  - Update inverter simulations and models with empirical component data
  - Develop and evaluate alternative design concepts for high temperature inverter
- **Test and evaluate various silicon power die for the DOE inverter application**

Accomplishments to Date: Summary

- **System**
  - Targets for inverter and components provided and agreed upon with all partners
  - Substantial progress achieved by Delphi and all partners toward demonstrating potential to achieve DOE performance and cost targets
- **Power Semiconductors**
  - SiC-on-Silicon (Dow Corning - GeneSiC)
    - Demonstrated SiC film grown on Si, using Dow Corning's SiC-on-Si CVD process
    - Provided mechanical sample devices for Delphi's novel packaging solution
  - Silicon (Delphi)
    - Worked with preferred suppliers to deliver silicon IGBTs and diodes for Delphi's novel packaging solution
- **Capacitors**
  - Film (GE)
    - Several promising thin film materials identified; optimizing candidate films for low cost and volume production
  - Film-on-Foil (Argonne)
    - Process for embedding caps demonstrated; Many capacitors fabricated, analyzed and tested; Inventions recorded (3), patent applications for cap processing and manufacture (Argonne / Delphi)
- **Packaging & Integration**
  - Various system topologies evaluated (Delphi / ORNL)
  - System model constructed to evaluate SiC-on-Si potential advantages (Delphi / DCC-GeneSiC / ORNL)
  - System and thermal modeling/simulation conducted on various topologies and packaging concepts (Delphi / ORNL)
  - Many thermal management concepts evaluated and analyzed; several invention records written for submission and patent applications being prepared

Future Work

- **FY 2010-11 (Complete Phase II)**
  - **Complete the evaluation of alternative inverter concepts and down-select to a preferred concept for Phase IIB**
  - **Using the technologies developed in Phase IIA in conjunction with our building block inverter technologies, design, build and test an inverter to meet the DOE requirements.**

Summary

- Meeting the cost, size and weight as well as application requirements for inverters will help the automotive industry expand the market for energy efficient and alternative energy compatible HEVs, PHEVs, and FCVs
  - ***This will help to reduce U.S. dependence on foreign oil and reduce greenhouse gas emissions***
- To support this project, Delphi has assembled a cross-functional engineering team of experts in power electronics/inverter design, systems engineering, mechanical engineering, passive components, and controls engineering.
- Our partners Dow Corning / GeneSiC, GE, Argonne, ORNL, and NREL are providing new discrete power devices, capacitor technology, system modeling/simulation & testing, and thermal modeling expertise to help Delphi develop a low cost, compact, light-weight, high-temperature inverter that meets the DOE targets.
- Delphi is developing this technology with commercialization in mind.
- During 2008, Delphi with its partners accomplished its Phase I objectives, and are working effectively as a team toward achieving the 2009 objectives for Phase IIA.