U.S. DEPARTMENT OF ENERGY

OAK RIDGE NATIONAL LABORATORY
MANAGED BY UT-BATTELLE FOR THE DEPARTMENT OF ENERGY

High-Temperature, High-Voltage Fully Integrated Gate Driver Circuit

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Project ID: APE003

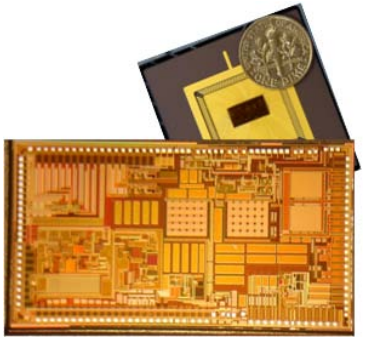
Overview

Timeline

- Start Date: Oct. 2008
- End Date: Sept. 2010
- 80% Complete

Budget

- DOE Share – 100%
- FY09 received: $367K
- FY10 received: $330K



Barriers

- Achieving high-temperature capability with silicon IC platform
- Achieving universal gate drive solution capable with emerging WBG power switches
- Achieving highly integrated gate drive solution with high output current drive
- High-temperature solutions require high-temperature gate drives

Partners

- Development: The University of Tennessee
- Field Testing: GM ATV

Objective

- Develop a highly reliable, integrated gate drive circuit that is capable of operating at high temperatures with high drive current while driving GaN or SiC JFETs or MOSFETs.
- FY10: Refine and add capability to universal gate driver chip.
  - Design, fabricate and test a silicon on insulator (SOI) chip that is robust over wide temperature range (up to 200° C ambient).
  - Incorporate additional protection features.
  - Add input isolation test circuitry.
  - Enable 100% duty cycle.

Milestone

- **August 2009: Successfully demonstrate that the fabricated SOI gate drive chip (3G) can act as a gate driver over a wide temperature range for prototype SiC MOSFETs and JFETs obtained from suppliers.**
  - *Go/No Go - Ability of SOI chip to drive SiC FET over wide temperature range (−40° C to 175° C)*

- **August 2010: Demonstrate *Corinth (4G)* SOI gate drive IC functioning as a gate driver over a wide temperature range (up to 200° C) driving prototype SiC MOSFETs and JFETs. Verify chip features including protection circuits and input isolation test circuitry, and characterize the gate driver operation.**

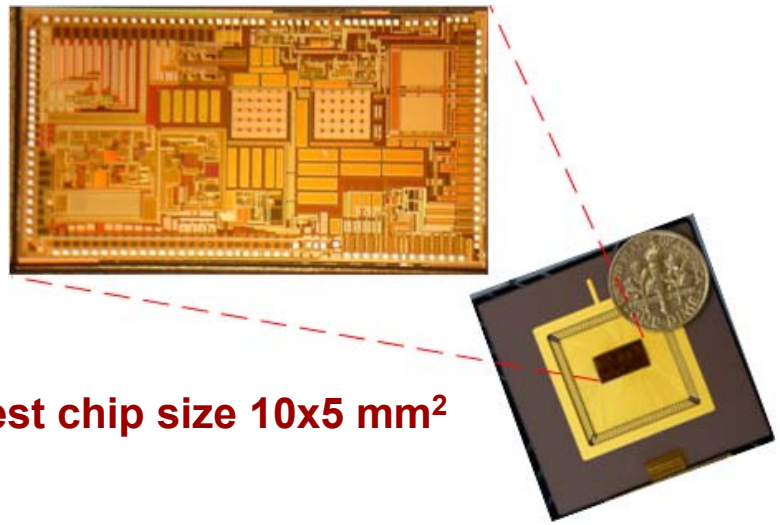
Approach

- SOI-based high-temperature, high-voltage gate driver will be developed that can work up to 200° C ambient.
- Improve circuit topology for reliable and repeatable performance at elevated temperatures.
- Test prototypes to support a variety of SiC-based or GaN-based power switches (JFETs and MOSFETs) as they become available. Driver designed as a "universal gate drive" to meet various FET specs.
- Provide additional protection features, such as de-saturation protection and gate current monitoring to enhance robustness and incorporate "smart" drive capabilities.
- Successful execution of this research combined with commercially available WBG-based power switches will help realize high-temperature DC-DC converters and traction drive systems (inverters) for HEVs.

Approach (cont'd): Description of Silicon-on-Insulator (SOI) Technology

- **Develop high-temperature, high-voltage fully integrated gate driver utilizing Bipolar-CMOS-DMOS on Silicon-on-Insulator (BCD on SOI) technology**
  - **SOI offers inherently low leakage current and latch-up immunity, thus enabling circuits to operate at higher temperature than their bulk Si-based counterparts.**
- **Novel circuit design approach to provide gate driver circuit performance insensitive to temperature variation**

FY09 Technical Accomplishments



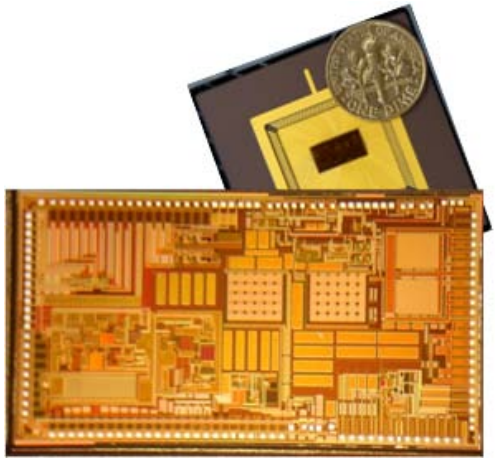
Test chip size 10x5 mm^2

High-temperature polyimide test board

- 3G prototype of a high-temperature, high-voltage integrated circuit gate driver designed and fabricated using a BCD-on-SOI process from Telefunken Semiconductor.
- Successfully tested with SiC MOSFETs and JFETs (both normally on and normally off) at 200° C without any heat sink and cooling mechanism.

FY09 Technical Accomplishments: Prominent Features of SOI Chip

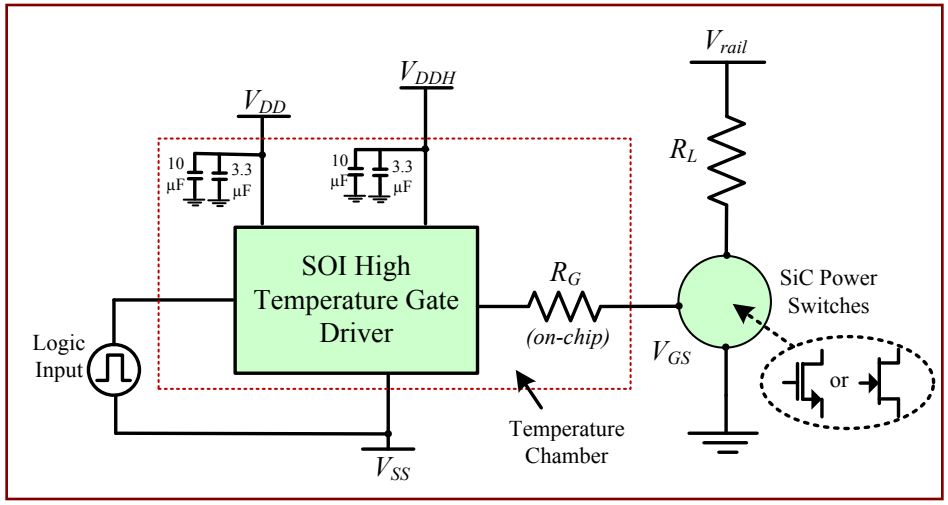
- High source and sink current capability: peak 2.9 A @ 27° C and 2.2 A @ 200° C ambient
- Gate drive supply range from 10 V to 30 V p-p
- High operating temperature: 200° C ambient without any cooling mechanism
- High capacitive load drive capability: 10 nF in < 100ns @ 200° C



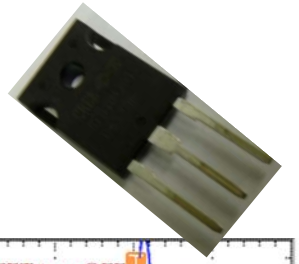
Chip size 10x5 mm^2

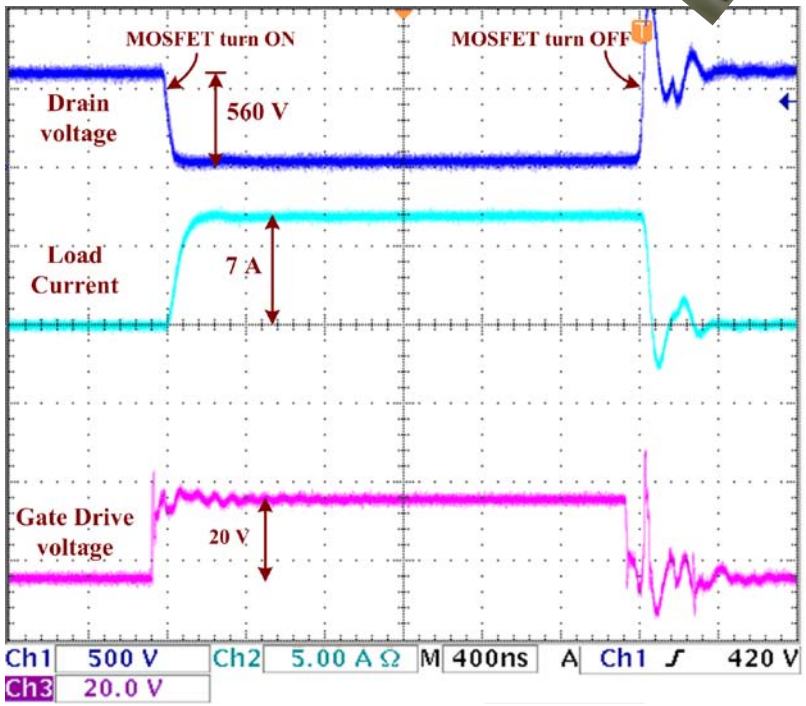
- Die area of 10 x 5 mm^2 for fully functional test chip, including the core gate driver circuit, 5-V on-chip voltage regulator, short-circuit protection, undervoltage lockout, bootstrap capacitor, dead time controller and temperature sensor
- 0.8-micron, 2-poly and 3-metal BCD on SOI process from Telefunken has been used

FY09 Technical Accomplishments: Prototype Driving SiC MOSFET



1200-V, 10-A Cree MOSFET

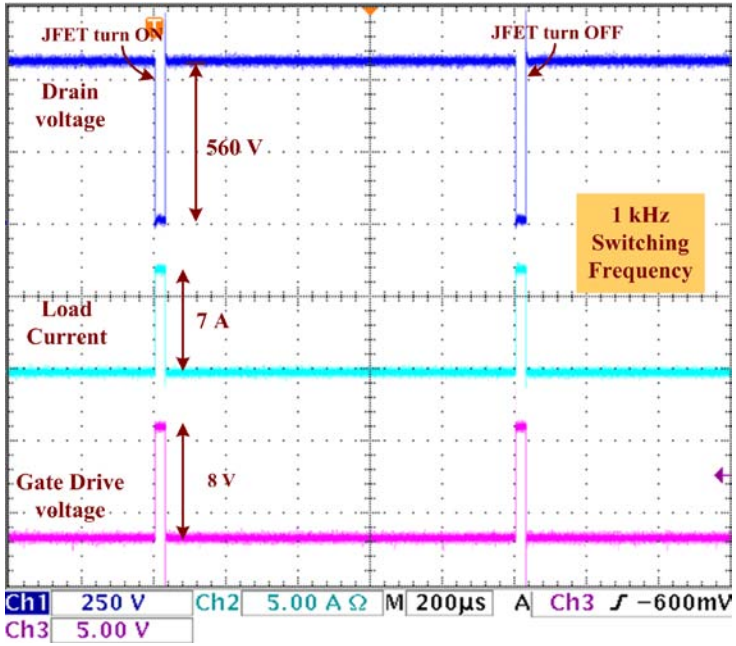


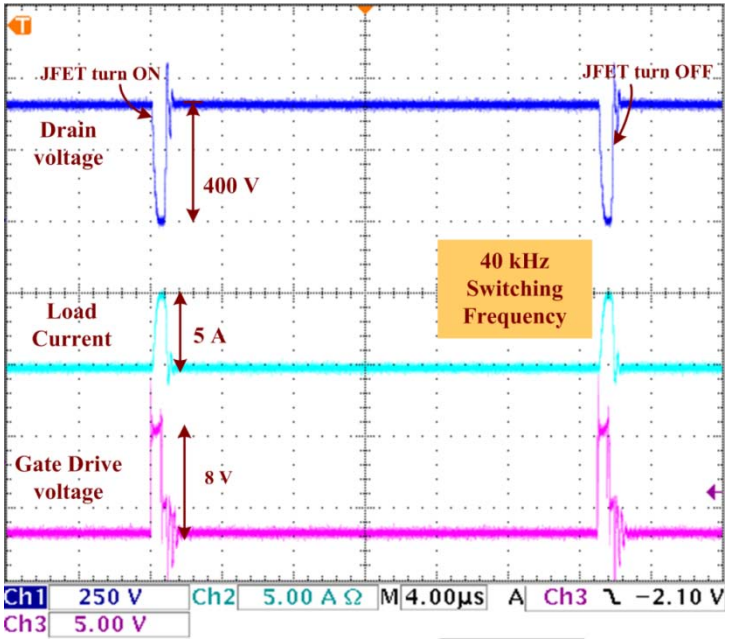


1200-V, 10-A SiC MOSFET driven at 200° C ambient temperature (R_G=4.3 Ω @ 200° C)

Ambient Temp. (° C)	Drain voltage (V_{DS})		Gate voltage (V_{GS})	
	t_{rise} (ns)	t_{fall} (ns)	t_{rise} (ns)	t_{fall} (ns)
27	15.7	33.4	2.8	3.6
125	15.7	35.1	3.1	4
200	20.2	41.0	4	5.6

FY09 Technical Accomplishments: Prototype Driving SiC JFET



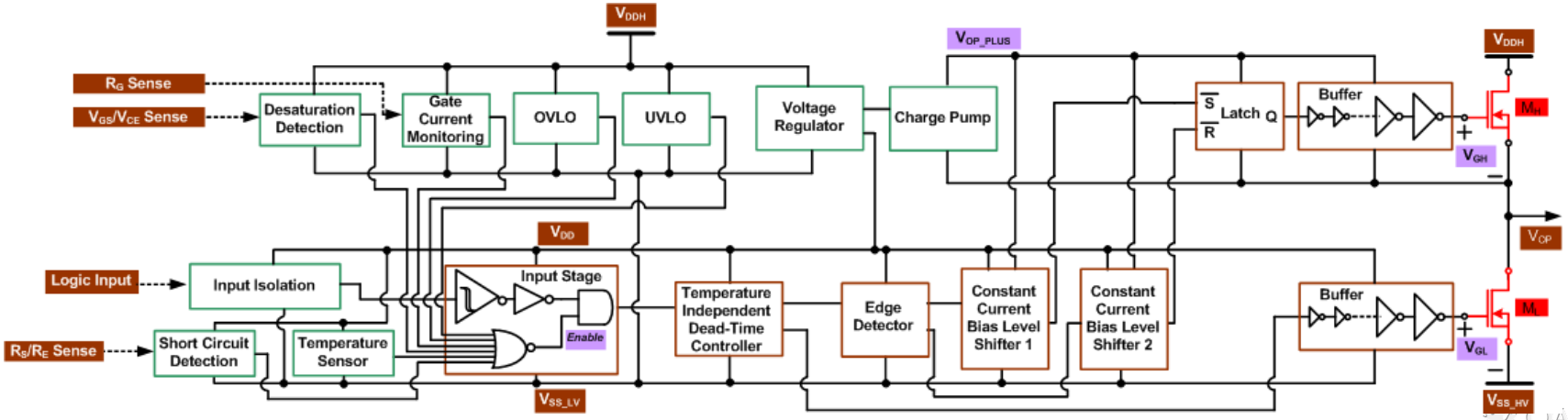


1200-V, 50-A SiC JFET (Microsemi/SemiSouth) module driven at 200° C ambient temperature (R_G = 4.3 Ω @ 200° C)

Ambient Temperature (° C)	Drain voltage (V_{DS})		Gate voltage (V_{GS})	
	t_{rise} (ns)	t_{fall} (ns)	t_{rise} (ns)	t_{fall} (ns)
85	83	202	2.8	3.2
125	85	207	3.0	4.0
200	97	242	3.2	4.1

FY10 Technical Accomplishments

- The next gate driver chip design (4G), *Corinth*, is in progress.
  - Proposed features include test structures for high-temperature capable input isolation to protect logic generator and allow for use in bridge configurations without external isolation hardware.
  - On-chip charge pump replacing the bootstrap diode/capacitor to provide 0-to-100% duty cycle operation.
  - Additional protection circuitry including de-saturation detection.
  - Preliminary gate current monitoring circuitry (toward *smart gate drive*[1]).
  - Core gate driver optimized for smaller area.
  - Revising 3G designs including UVLO, Zener-based voltage regulator, short-circuit current monitoring, and increase maximum output current to 5 A.
  - Low-voltage differential signaling (LVDS) input to better support testing.



[1]*Lihua Chen; Peng, F.Z.; Dong Cao, "A smart gate drive with self-diagnosis for power MOSFETs and IGBTs," Applied Power Electronics Conference and Exposition, 2008. APEC 2008. Twenty-Third Annual IEEE , vol., no., pp.1602-1607, 24-28 Feb. 2008*

Collaborations

- University of Tennessee
  - Gate drive design and testing
- General Motors
  - Gate driver testing with power modules

Future Work – FY10

- Finish *Corinth* (4G) and send out for fabrication.
- Fabricate and populate polymide high temperature test board.
- Receive fabricated and packaged SOI chips – expected late June/July 2010.
- Measurement and characterization of *Corinth* prototype circuits with SiC power MOSFETs and JFETs.

Future Work – FY11 and beyond

- Project Ends FY10

Summary

- A highly integrated, high temperature gate drive is being developed for use with future wide bandgap (silicon carbide and gallium nitride) switching devices.
- Universal drive that is capable of driving a wide variety of devices including MOSFETs, JFETs, and IGBTs.
- Gate drive will be an enabling technology for using power electronics at higher temperatures.