U.S. DEPARTMENT OF ENERGY

OAK RIDGE NATIONAL LABORATORY
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A Segmented Drive Inverter Topology with a Small DC Bus Capacitor

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Project ID: APE004

2010 DOE Hydrogen Program and Vehicle Technologies AMR

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Overview

Timeline

- Start – Oct. 2008
- Finish – Sept. 2011
- 45% complete

Budget

- Total project funding
  - DOE share – 100%
- Funding received for FY09
  - $376K
- Funding for FY10
  - $735K

Barriers

- The DC bus capacitor presents significant barriers to meet the targets of cost, volume and weight for inverters. Currently, it contributes
  - Cost and weight, up to 23% of an inverter
  - Volume, up to 30% of an inverter
- Ability of film capacitors to operate at higher temperature deteriorates rapidly, leading to significant increases in cost, weight and volume
- Vehicle technology program targets
  - 2015 targets: $5/kW, 12 kW/kg, 12 kW/l

Partners

- Powerex – IGBT modules

Objective

- Develop a 55 kW segmented inverter prototype that can reduce the bus capacitance by at least 60%

- Objective for FY09
  - Perform a simulation study to assess the effect of various PWM schemes on the reduction of ripple current
  - Complete a conceptual design for a 55 kW prototype

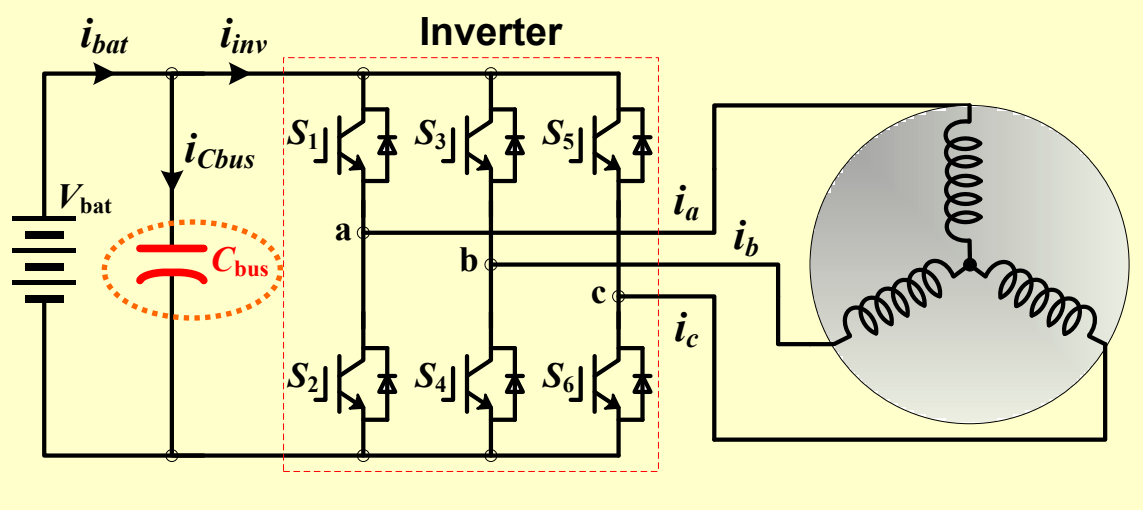
- Objective for FY10
  - Design, build, and test a 55 kW segmented inverter prototype for operating with a 70ºC coolant

Milestones

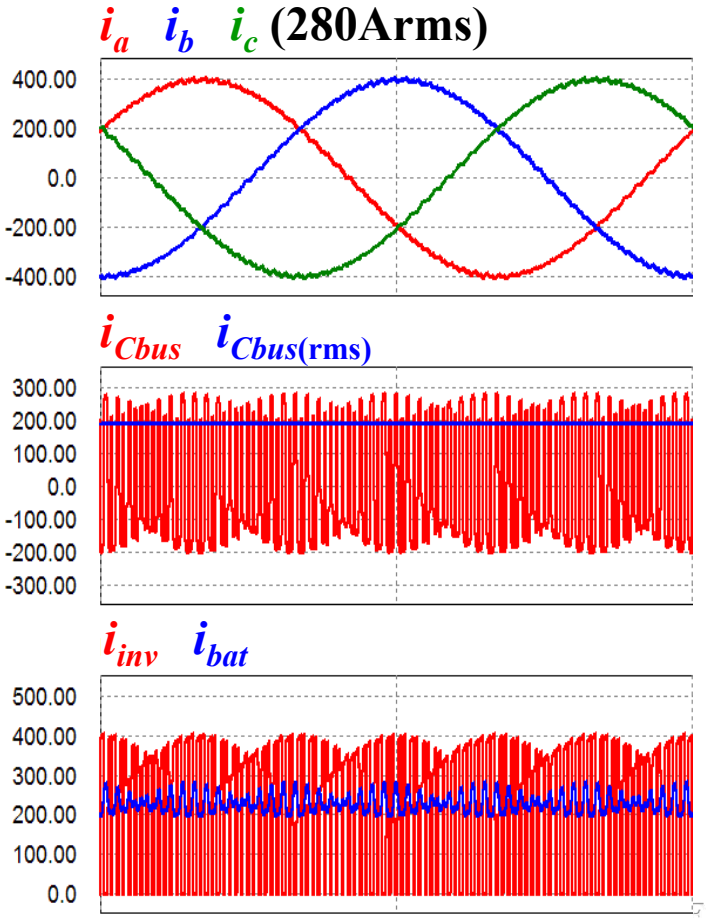
Month/Year	Milestone or Go/No-Go Decision
Jun-2009	Milestone: Completed simulation study of various PWM schemes on the impact of capacitor ripple current.
Sept-2009	Milestone: Completed a conceptual design for a 55 kW prototype. Go/No-Go Decision: Meeting the goal of > 60 % reduction in capacitor ripple current.
May-2010	Milestone: Complete fabrication of a 55 kW segmented inverter prototype
Sept-2010	Go/No-Go Decision: Experimentally demonstrate a 55 kW segmented inverter prototype with a dc bus capacitor of 400 μF (reduced from 1000 μF for a baseline inverter)

Approach

- A typical 55 kW inverter requires a large dc bus capacitor of 1000~2000 µF to handle large ripple currents (~250 Arms).
- Increasing switching frequency has little impact on the magnitude of the bus capacitor ripple current.
- Film capacitor ripple current and voltage capability decreases rapidly with temperature.

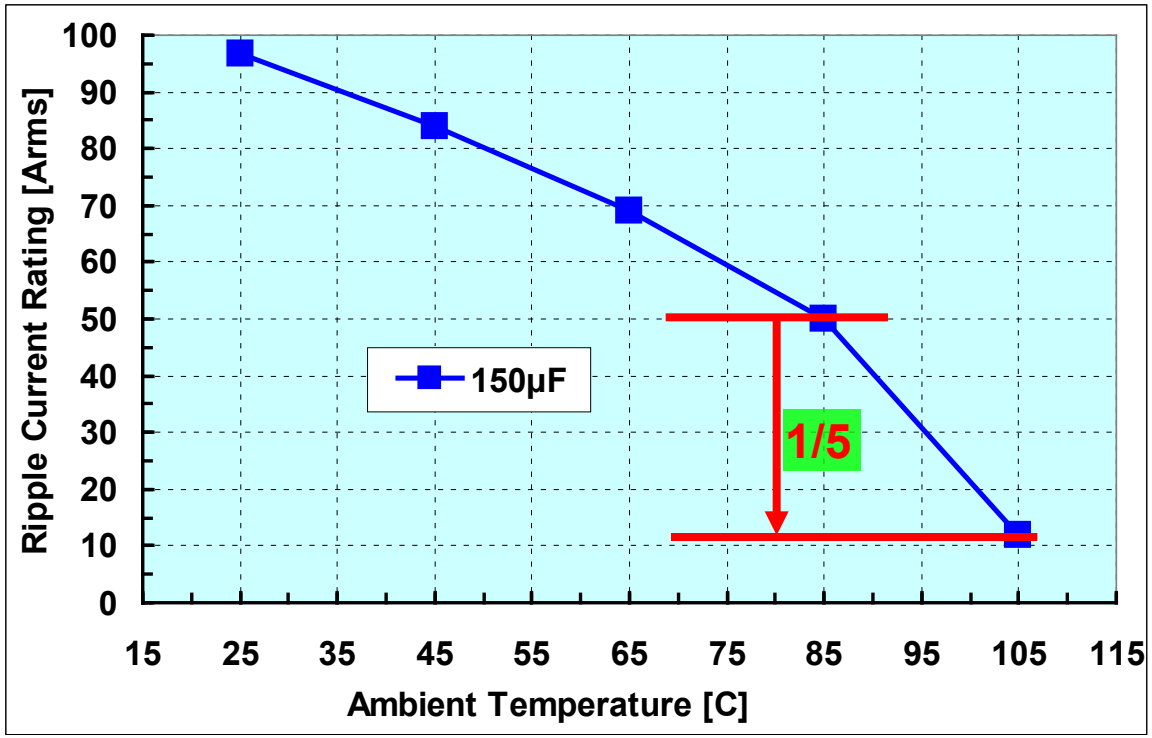


Standard VSI Topology (above)
Simulated Waveforms (right)



Approach (contd.)

- High temperature operation challenge for the bus capacitor
  - Film capacitor ripple current and voltage capability decreases rapidly with temperature
    - 50% linear voltage derating from 85ºC to 105ºC
  - Non-benign failure modes are concerns for ceramic capacitors



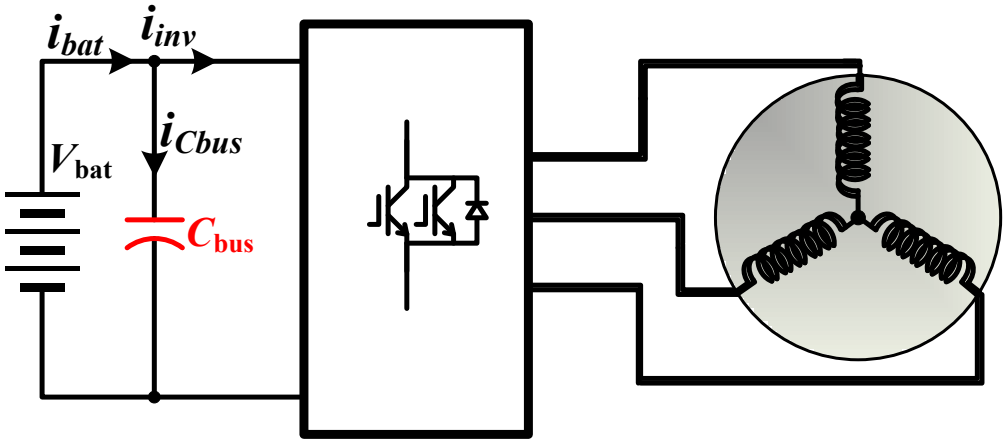
Electronic Concepts
UL31 Series, 600 V
Diameter: 83.3 mm

For example, as temperature rises from 85 to 105°C, weight, volume and cost of capacitors could increase by a factor of 5

Source: http://www.eci-capacitors.com/product_details.asp?productid=29

Approach (contd.)

- Use a segmented drive system topology that
  - does not need additional switches or passive components but can significantly reduce
    - the dc link ripple current, and
    - the capacitance



Approach (contd.)

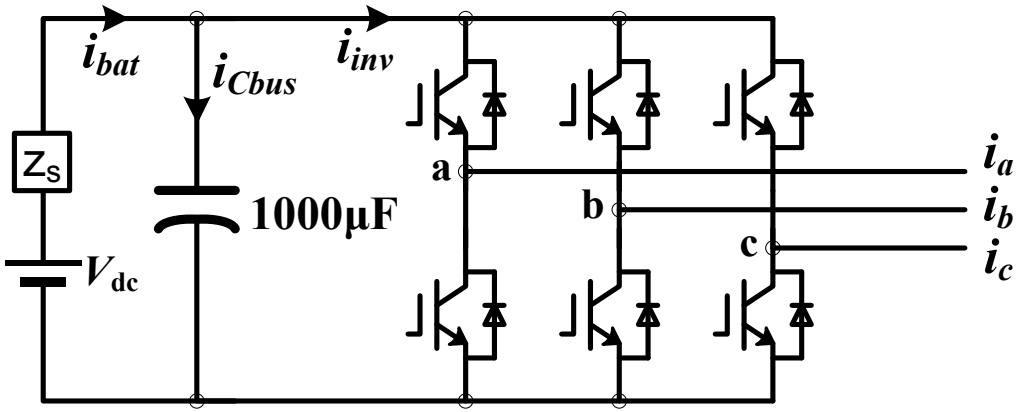
- Perform simulation study of various PWM schemes
  - Various carrier-based and space-vector PWM techniques will be simulated using PSIM to assess their impact on the capacitor ripple current
- Build and test a 55 kW inverter prototype to experimentally validate the simulation study
- Build and test a 55 kW prototype of an integrated segmented inverter-motor drive system
  - Custom IGBT modules
  - Integrated drive packaging

Technical Accomplishments and Progress - Overall

- Completed a simulation study; results proved the concept.
- Assessed the impact of various carrier-based & space-vector PWM techniques on the capacitor ripple current and down-selected an optimal method that maximizes the reduction of the ripple current.
- Achieved a reduction of the capacitor ripple current of 66% compared to the standard VSI, and
  - 80% reduction in battery ripple current
  - 70% reduction in DC bus ripple voltage
  - 50% reduction in motor ripple current
- Completed a hardware design for a 55 kW prototype and prototype fabrication almost completed.

Technical Accomplishments and Progress – FY09 (contd.)

- **Simulation study for**
  - (a) Standard VSI: Triangle-sine comparison PWM (base line)
  - (b) Segmented drive: PWM 1
  - (c) Segmented drive: PWM 2
  - (d) Segmented drive: Optimized PWM

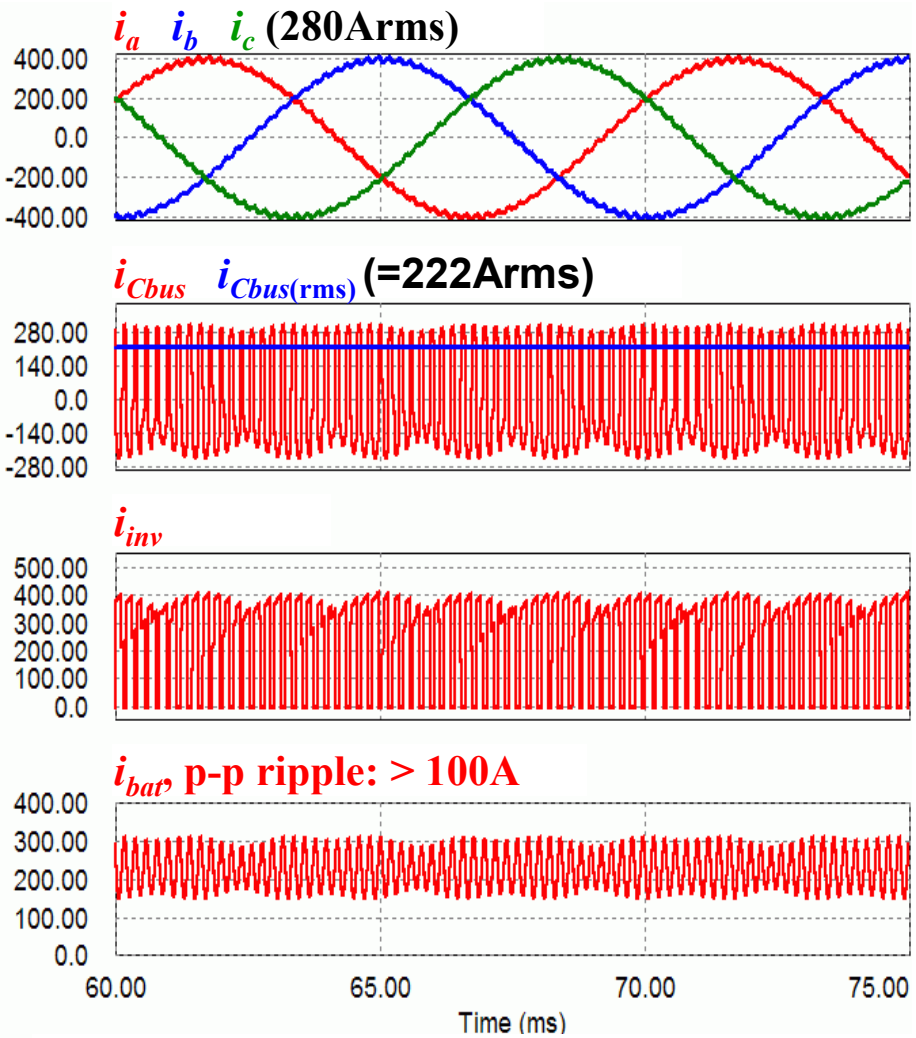


Base line inverter

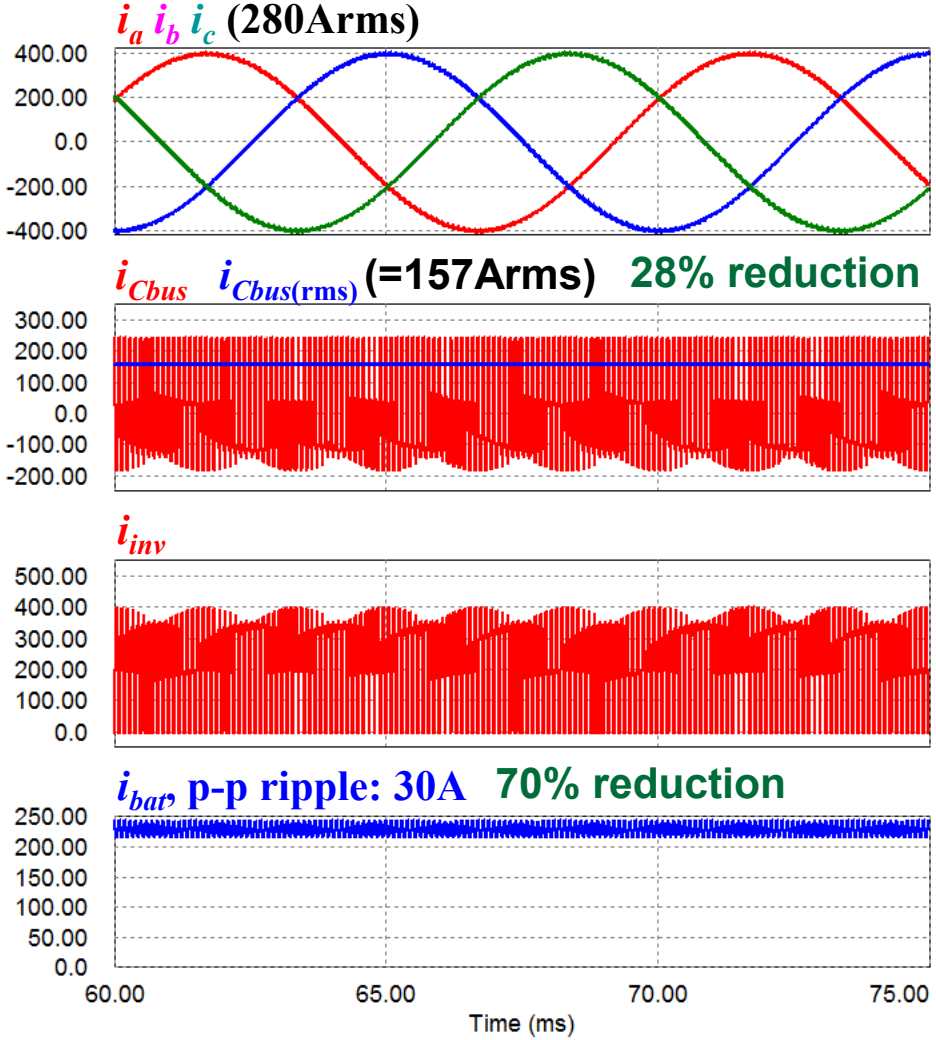
A point of notice:
Reduction ratios of ripple current and capacitance by the segmented drive inverter do not change with the dc bus capacitance.

Technical Accomplishments and Progress – FY09 (contd.)

- Simulated waveforms



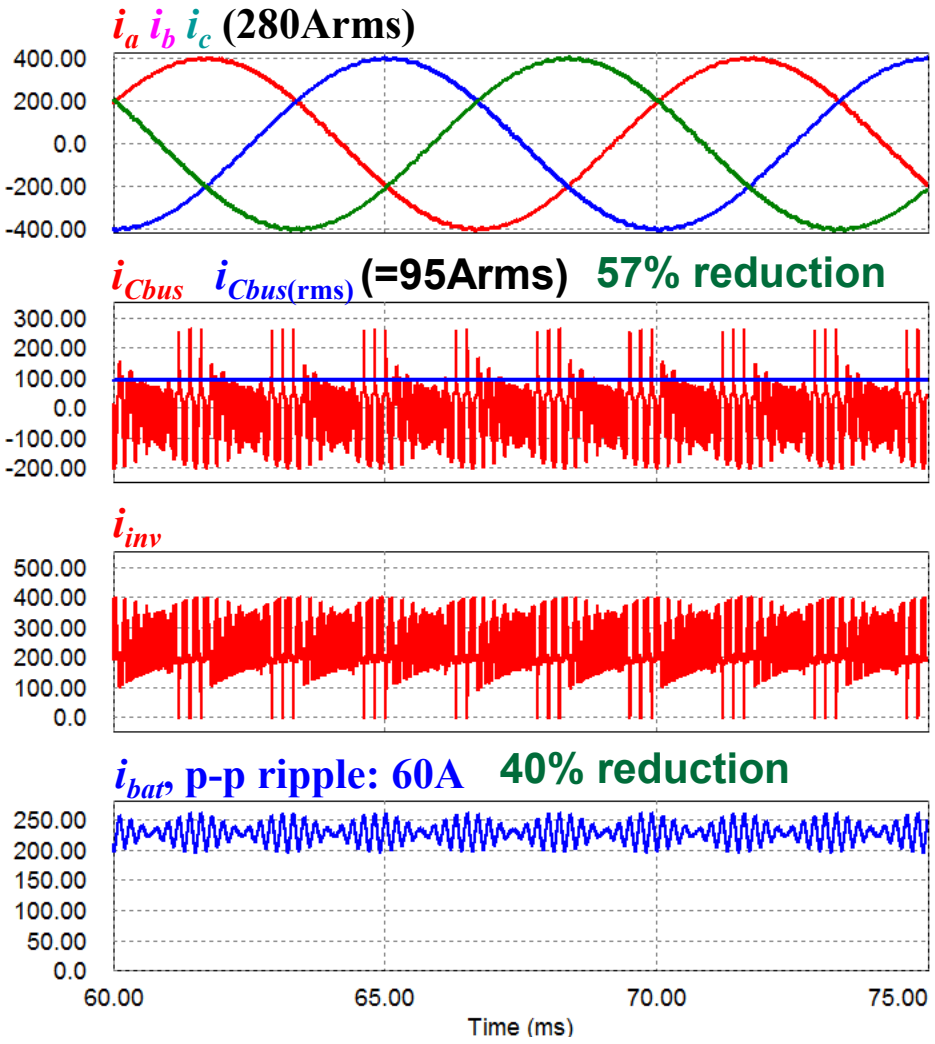
(a) Standard VSI w/ Triangle-Sine Comparison (base line)



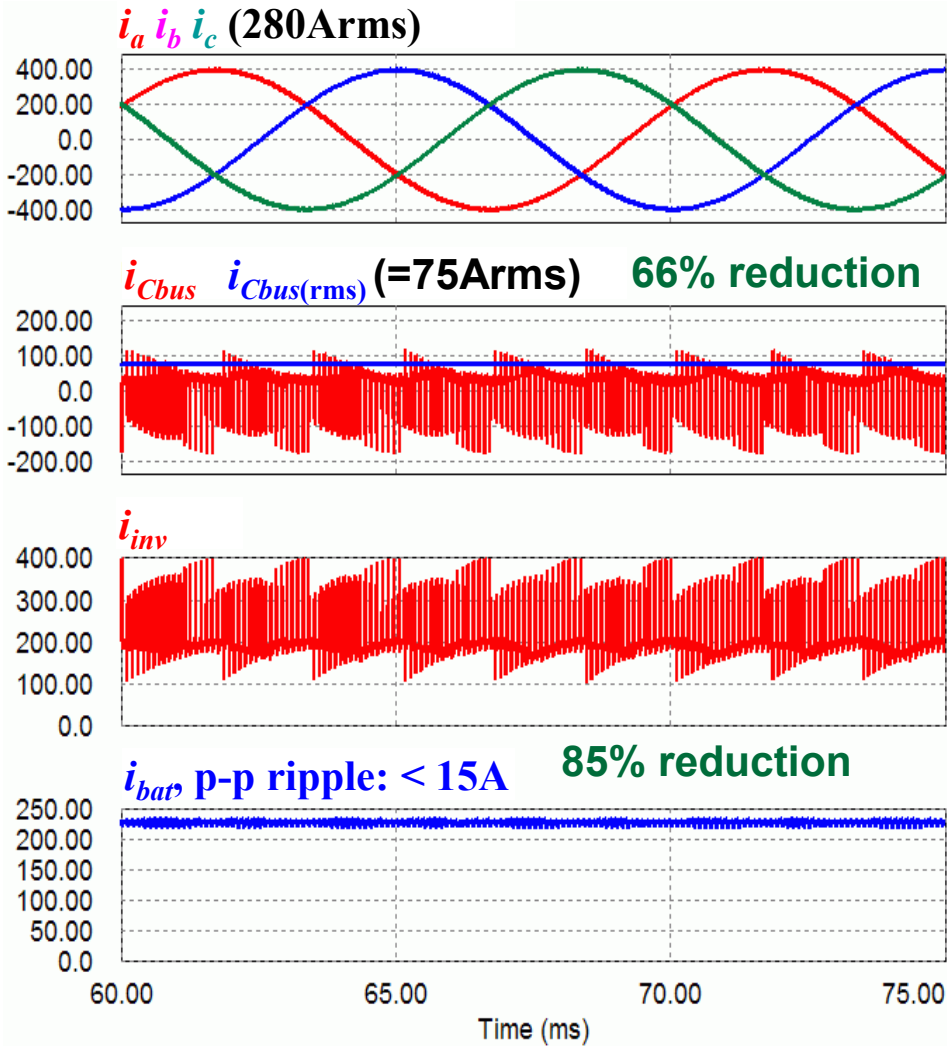
(b) Segmented Drive w/ PWM1

Technical Accomplishments and Progress – FY09 (contd.)

- Simulated waveforms



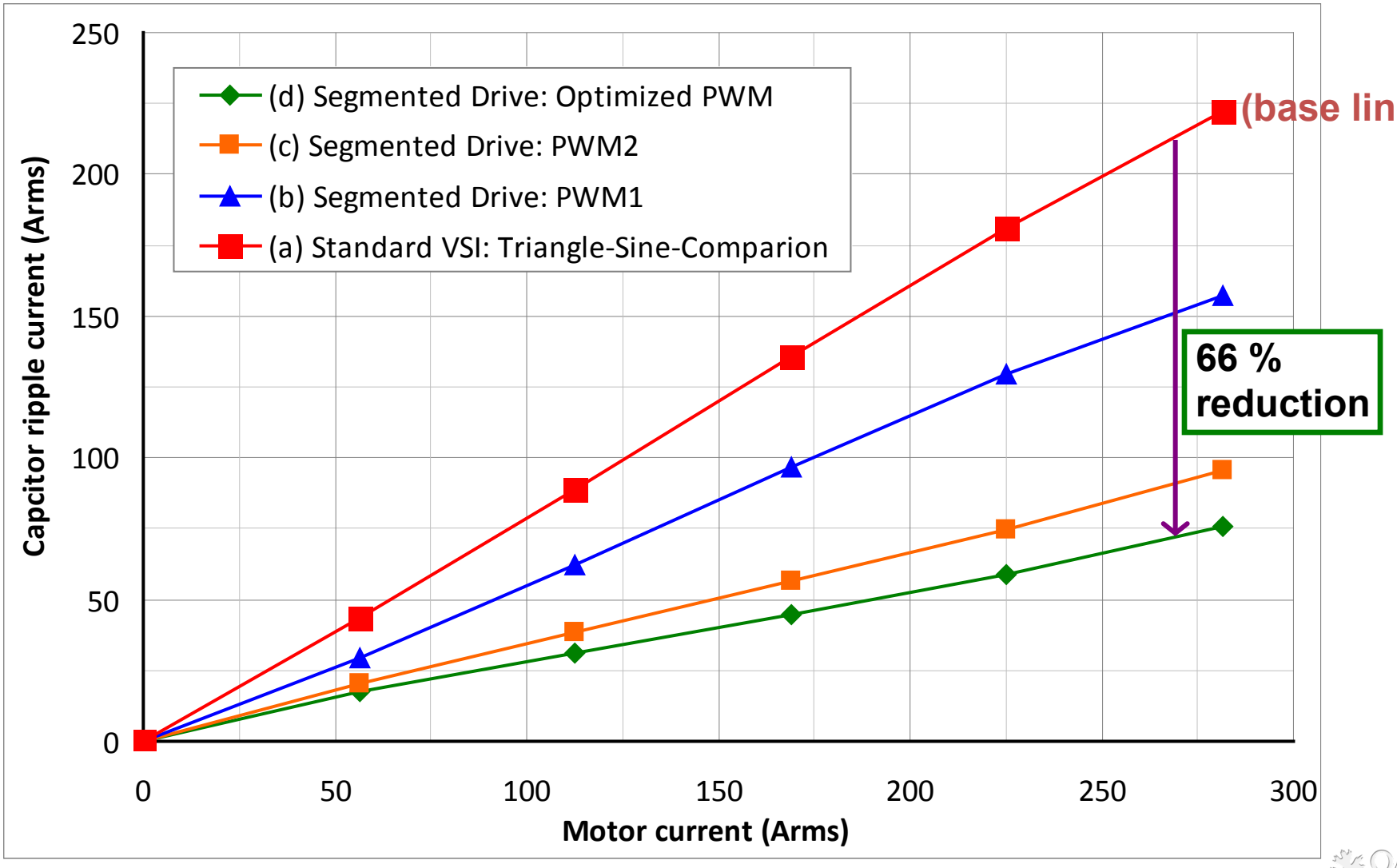
(c) Segmented Drive w/ PWM2



(d) Segmented Drive w/ Optimized PWM

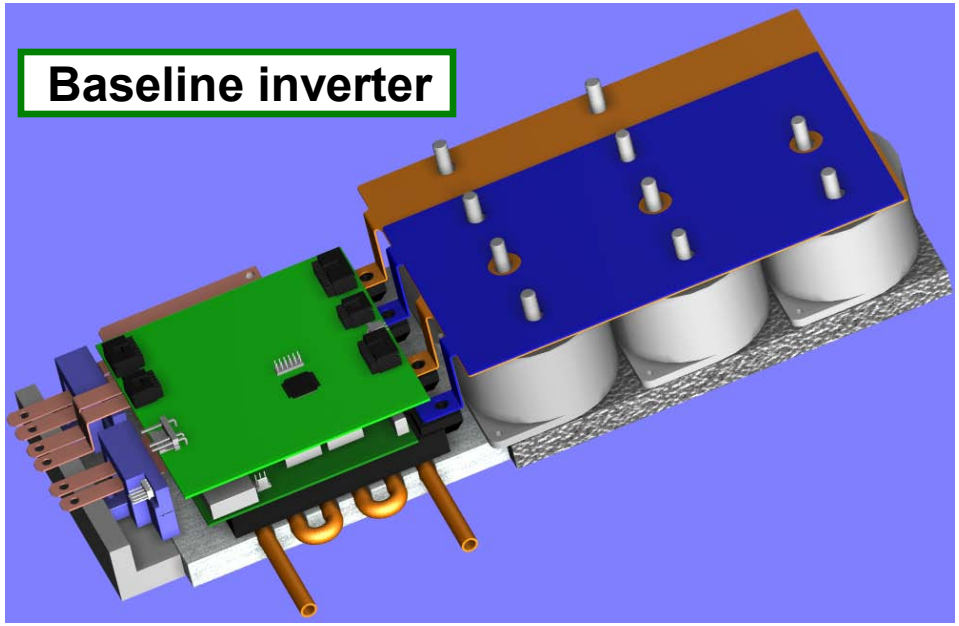
Technical Accomplishments and Progress – FY09 (contd.)

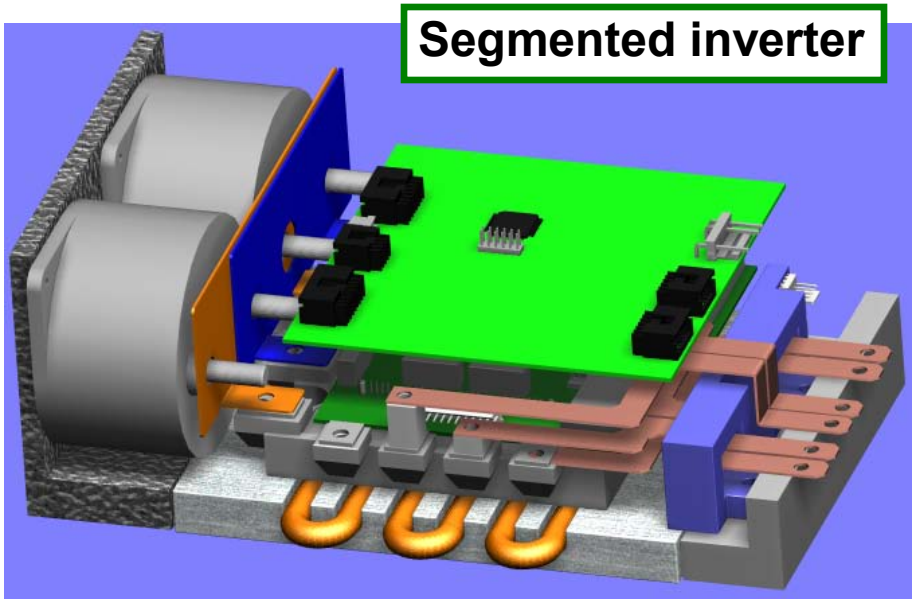
- Comparison of cap. ripple current vs. motor current



Technical Accomplishments and Progress – FY10 (contd.)

- **Hardware design for 55 kW prototypes**
  - Two capacitors for segmented inverter, each rated at 500V/200μF
  - Five capacitors for baseline inverter, each rated at 500V/200μF

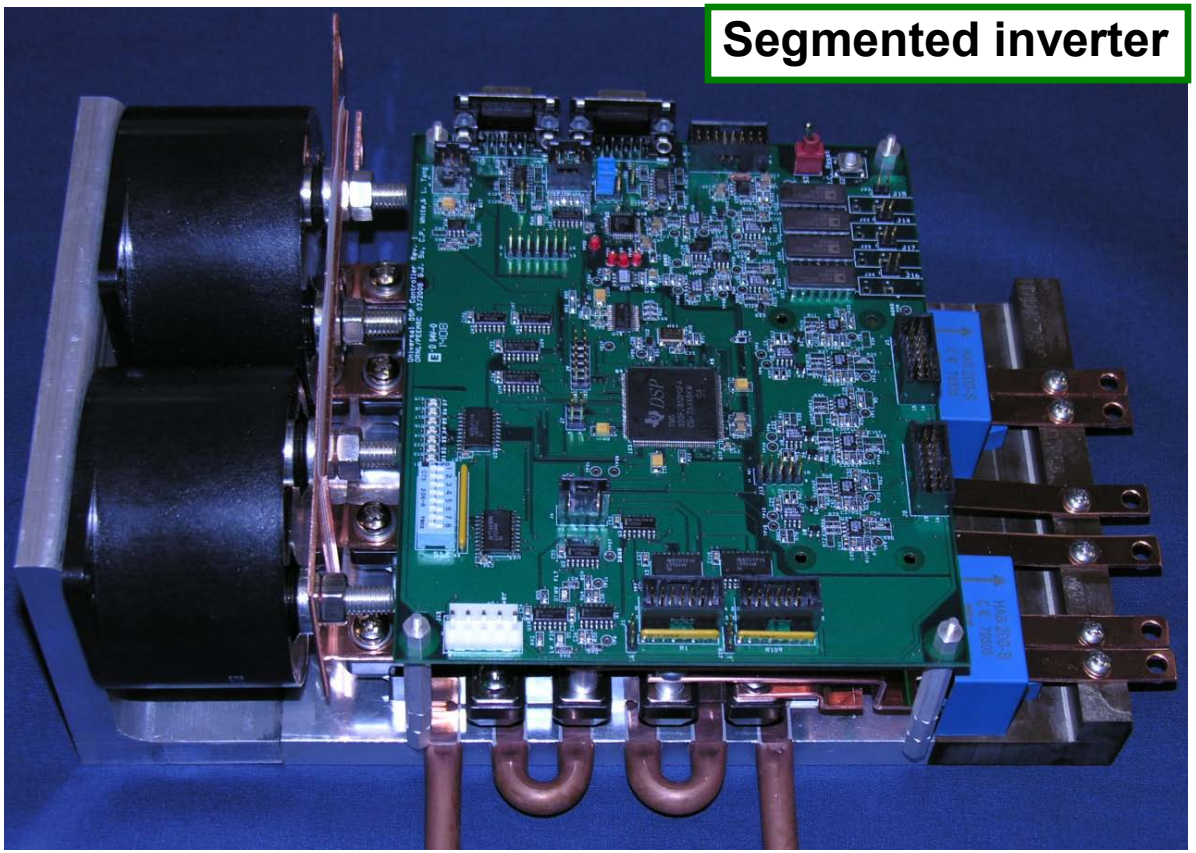




	Baseline	Segmented
Heat sink footprint	6”x7”+ 6.6”x9.6”	6”x7”+ 6.6”x2.2”
Cap. volume	1.39L	0.56L ➡ a 60 % reduction

Technical Accomplishments and Progress – FY10 (contd.)

- **55 kW Segmented inverter prototype fabrication**
  - **90 % complete**
  - **Use TI's 32bit DSP chip, TMS320F28335**



Future Work

- Reminder of FY10
  - Complete the 55 kW inverter prototype fabrication
  - Implement the PWM techniques in real-time control DSP code
  - Test and characterize the 55 kW inverter prototype
- FY11
  - Design and build a 55 kW prototype of an integrated segmented inverter-motor drive
- FY12
  - Test and characterize the 55 kW integrated segmented inverter-motor drive prototype developed in FY11
  - Refine the integrated inverter/motor package

Collaborations

- After experimental validation of the topology in FY10, collaborations will be sought for our proposed work on an integrated inverter-motor drive system in FY11 with industry, academic and other national lab partners on
  - Custom IGBT modules
  - Custom Capacitors
  - Thermal management
  - Packaging technologies

Summary

- The proposed technology involves modifying the standard drive topology and optimizing the PWM scheme to significantly reduce the ripple current flowing into the capacitor
  - *without* additional silicon or passive (L or C) components
  - *without* additional sensors
  - *without* control complexity
- Impacts
  - Substantially reduce the bus capacitance (at least 60%) and thus inverter volume and cost
  - Reduce battery losses and improve battery operating conditions by reducing battery ripple current
  - Significantly reduce the motor torque ripples (up to 50%), or reduce switching losses by 50%
  - Increase inverter reliability
- Simulation results have shown a significant reduction of ripple current of 66%
- Prototype fabrication and test work are progressing as planned