High-Dielectric-Constant Capacitors for Power Electronic Systems*

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Project ID# APE-008

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Overview

Timeline

- Project start date: FY05
- Project end date: FY12
- Project continuation & direction determined annually by DOE
- Percent complete: 60

Budget

- Total project funding
  - DOE share: 100%
- Funding received in FY09: $985K
- Funding for FY10: $1800K

Barriers addressed

- Overall size and cost of inverters

  Capacitors are a significant fraction of the inverter volume (≈35%), weight (≈23%), and cost (≈23%).
- High-temperature operation

  The performance and lifetime of presently available capacitors degrade rapidly with increasing temperature (coolant temperature of 105°C).

Partners

- Penn State University
- Delphi Electronics
- Project Lead: Argonne National Laboratory

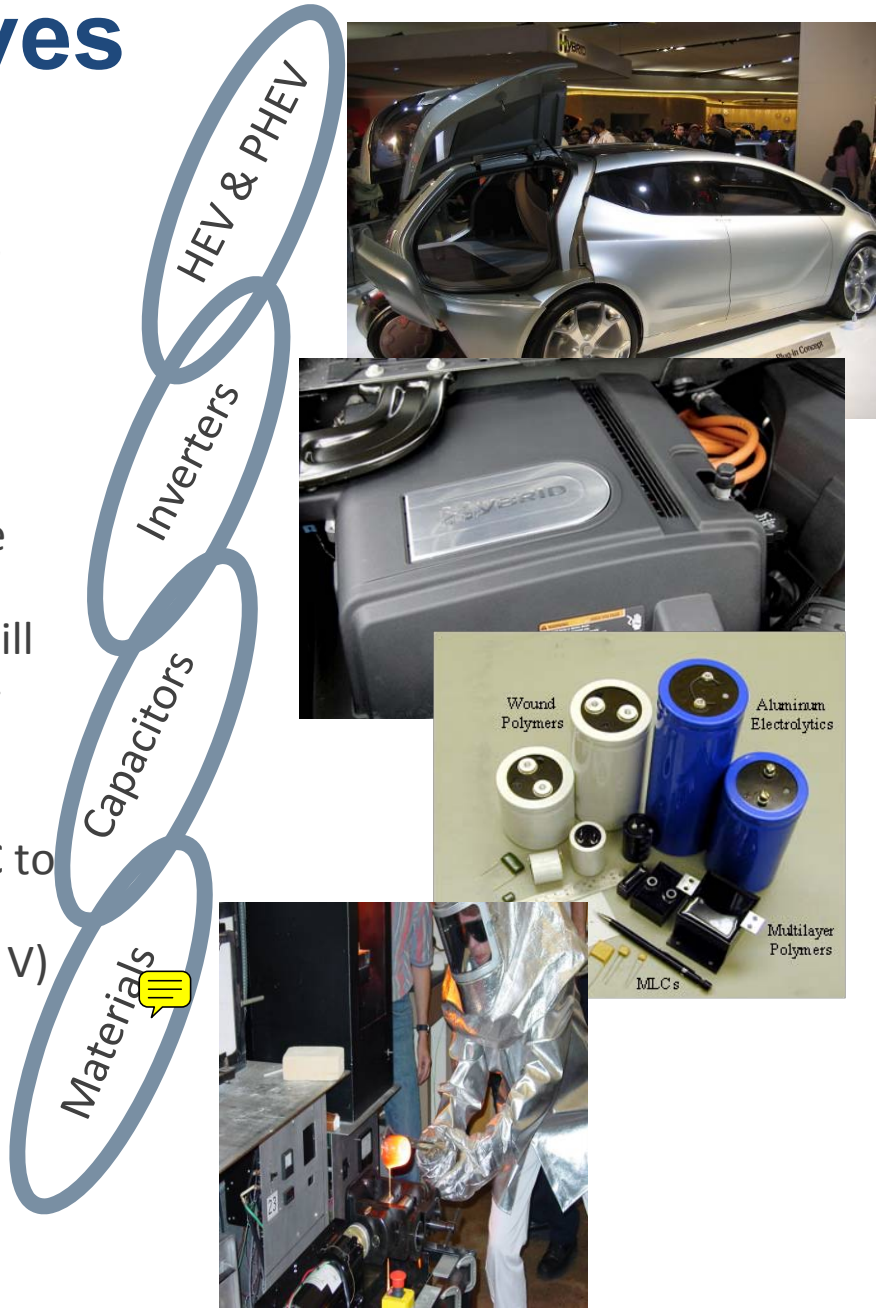
Objectives

- Overall objective is to develop technology for fabricating high performance, economical, capacitors for power electronic systems in HEVs, PHEVs, and FCVs.

  DC bus capacitors for inverters

  – *(450 V, 1000 µF, <3 mΩ ESR, 100 A ripple current,140°C, benign failure)*

- Objective for May '09 – May '10 was to fabricate and characterize high-voltage-capable 1" x 1" dielectric films on Ni foils ("film-on-foils") that will have the potential, upon scale-up, to meet DOE-APEEM goals.
- Dielectric films will have:
  – An operational temperature range of -50°C to +140°C
  – 450 V DC bus capability (peak transient 600 V)
  – High k (>1000) and E_b (≈2 MV/cm) to meet weight & volume target

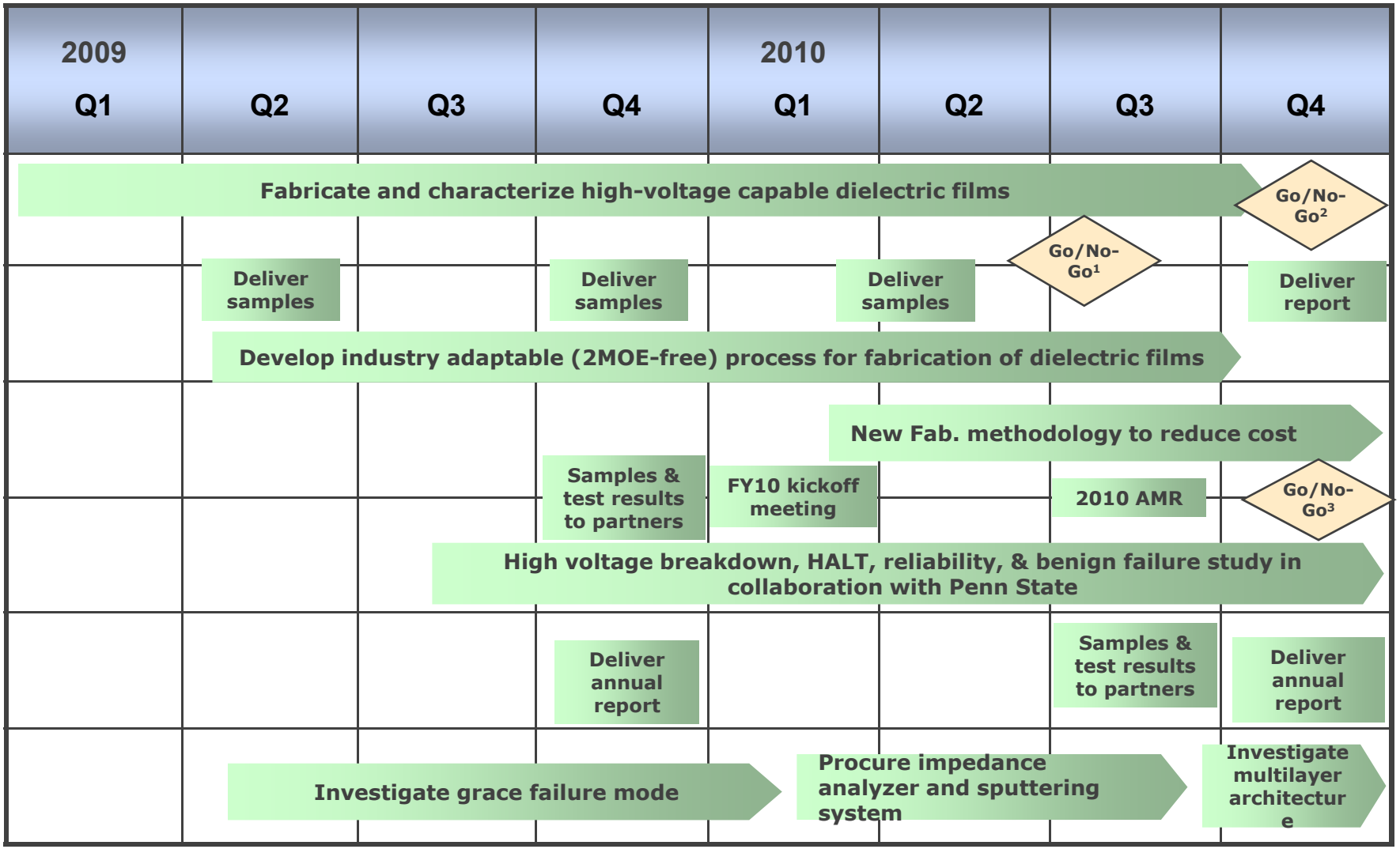


Relevance to Overall DOE Objectives of Petroleum Displacement

- Advanced inverters are essential for electric traction operations in HEVs, PHEVs, and FCVs.
- Future availability of advanced high-temperature (together with lower cost, weight, & volume) inverters will advance the marketplace application of highly fuel efficient & environmentally beneficial hybrid vehicles.
- Capacitors have direct impact on overall size, cost, & performance of inverters. Current polymer capacitors have temperature limitation.
- Capacitor development will reduce the size & increase the temperature of operation of one of the largest components in the inverter: the DC bus capacitor.
- We have fabricated & tested 1” x 1” film with uniform properties; a factor of 6400X larger in capacitor area compared to 2009 AMR data.

This project is developing dielectric films that has potential to reduce size, weight, and cost, concomitant with increased capacitance density & high temperature operation, for capacitors in inverters.

Milestones



Go/No-Go Decisions: 1. down-select the buffer layer (SRO vs. LNO)
2. down-select the substrate/quality for scale-up
3. down-select the fabrication methodology for future work

Technical Approach

- Develop ferroelectric (PLZT) dielectric film-on-foils that are either stacked on or embedded directly into the printed wire board.
- Integration of base-metal electrodes provides a cost advantage over noble metals used in conventional multilayer capacitors.
- Ferroelectrics possess high dielectric constants, breakdown fields, and insulation resistance. With their ability to withstand high temperatures, they can tolerate high ripple currents at under-the-hood conditions.
- Stacked and/or embedded capacitors significantly reduce component footprint, improve device performance, achieve high volumetric and gravimetric efficiency, and offer an economic advantage.
- Our approach focuses on fabricating films by chemical solution deposition, developing a fundamental understanding of processing effects on properties, and arriving at robust processing strategies.
- VT program focuses on three approaches, namely, ceramic films (Argonne), polymer (Sandia), and glass dielectric (Penn State). Fabrication and characterization efforts are coordinated within the three capacitor projects.

Argonne's project addresses the technology gap in an innovative manner

Uniqueness of Project and Impact
(caps embedded directly into PWB – caps are "invisible")

Basic Element

Metal foil coated with thin film PLZT dielectric

- PLZT/Ni Film-on-Foil
- PLZT/Cu Film-on-Foil

Component

Stack on or embed coated foils directly into printed wire circuit board for power electronics in (P)HEV

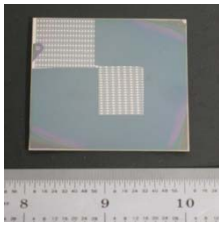
Advantages

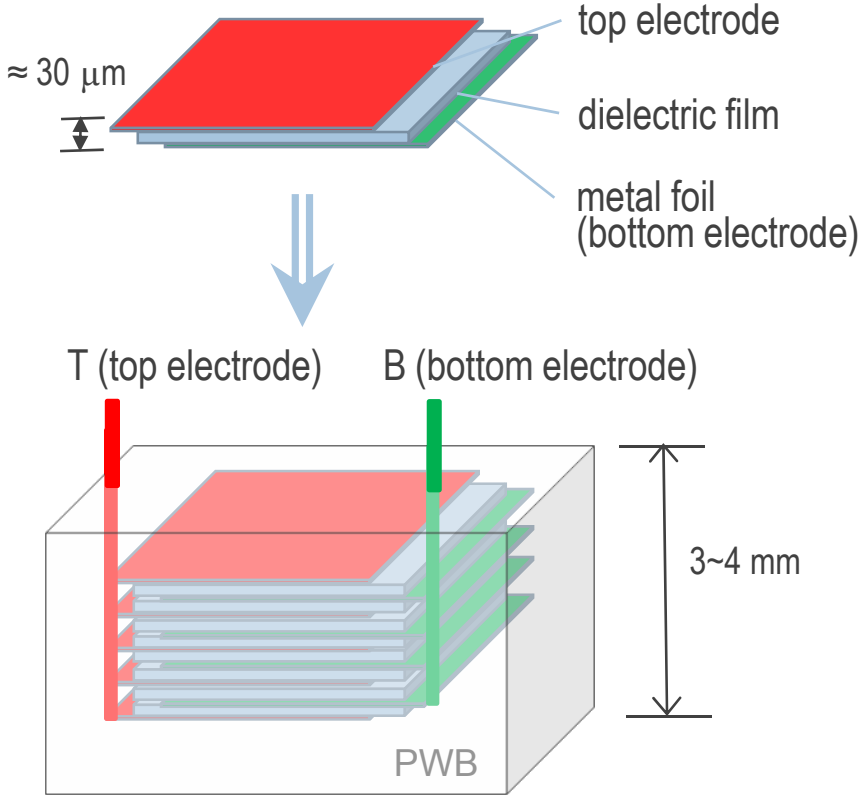
Reduces component footprint

Shortens interconnect lengths

Reduces parasitic inductive losses & electromagnetic interference

Film-on-foil capacitor



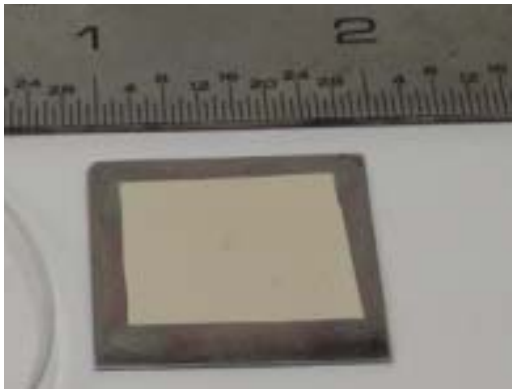


PWB Embedded capacitor with interconnections

Reliability is improved because the number & size of interconnections are reduced. Solder joints that are most susceptible to failure are no longer needed.

Technical Accomplishments/Results

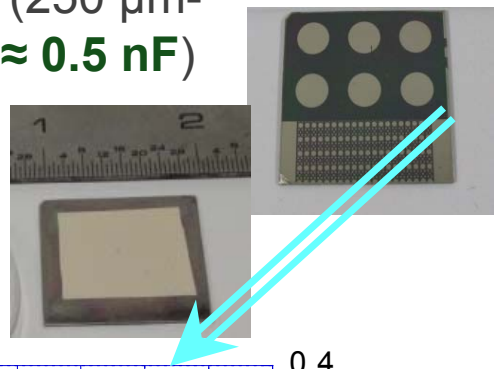
- Fabricated & measured ≈3.6 cm^2 film-on-foil (≈2.4 μm-thick PLZT) with capacitance of 1.6 μF (small area sample with ≈0.5 nF was reported at the 2009 AMR meeting).
- Demonstrated film-on-foil dielectrics with k >1300 and breakdown field > 2 MV/cm.
- Measured k ≈210 at 300 V & ≈115 at 600 V bias on a ≈3.0 μm-thick film.
- Preliminary high temperature measurement predicted mean time to failure of ≈4000 hrs at 100°C (under DC field of 260 kV/cm).
- Dielectric films are thermally cycled (about 1000 cycles) between -50°C and +150°C with no measurable degradation in k.
- Demonstrated graceful failure mode by self-clearing method in single layer film-on-foil dielectrics.
- Thin ceramic dielectric on relatively thick Ni substrate is quite strain tolerant (measured at ORNL by Andy Wereszczak).
- A CRADA with Delphi has been established (January 2008); samples have been provided to Delphi for testing.
- Over 35 publications and presentations have been made. One patent was issued & two Patent Applications were filed.

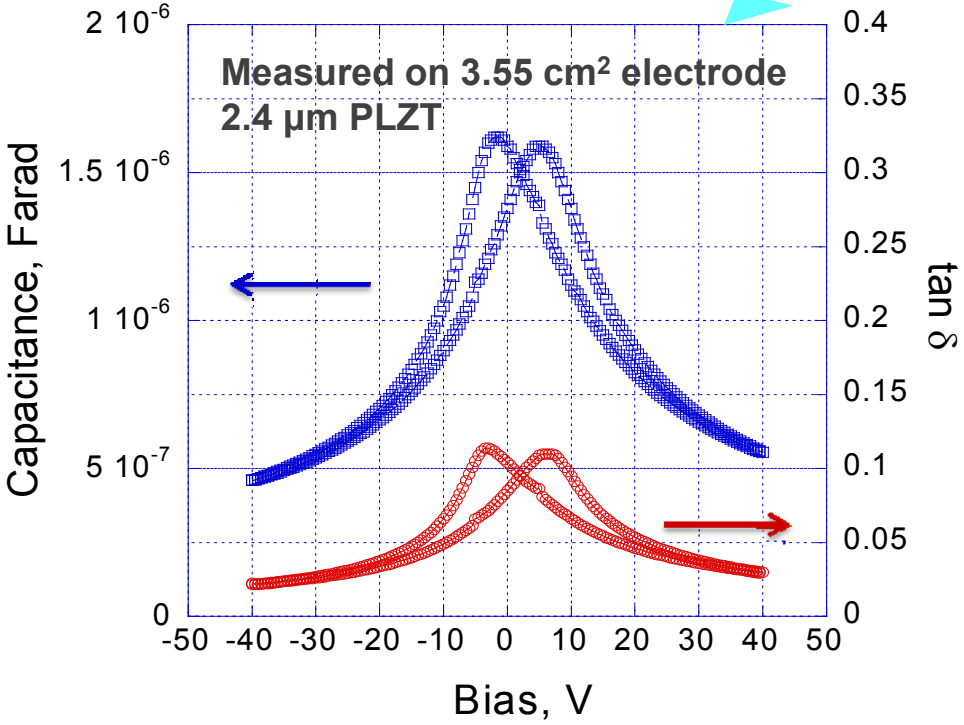


Technical Accomplishments/Results (Contd.)

Results @ '09 AMR Meeting (5/21/09)

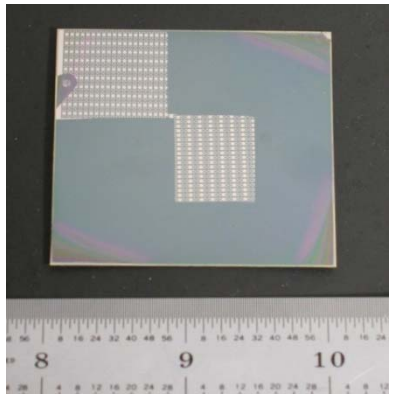
- Results on small areas (250 μm-dia.) of dielectric films (**≈ 0.5 nF**)
- ≈1 μm thick PLZT films

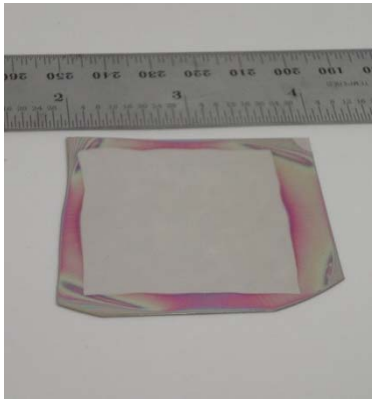




Results @'10 AMR Meeting (6/10/10)

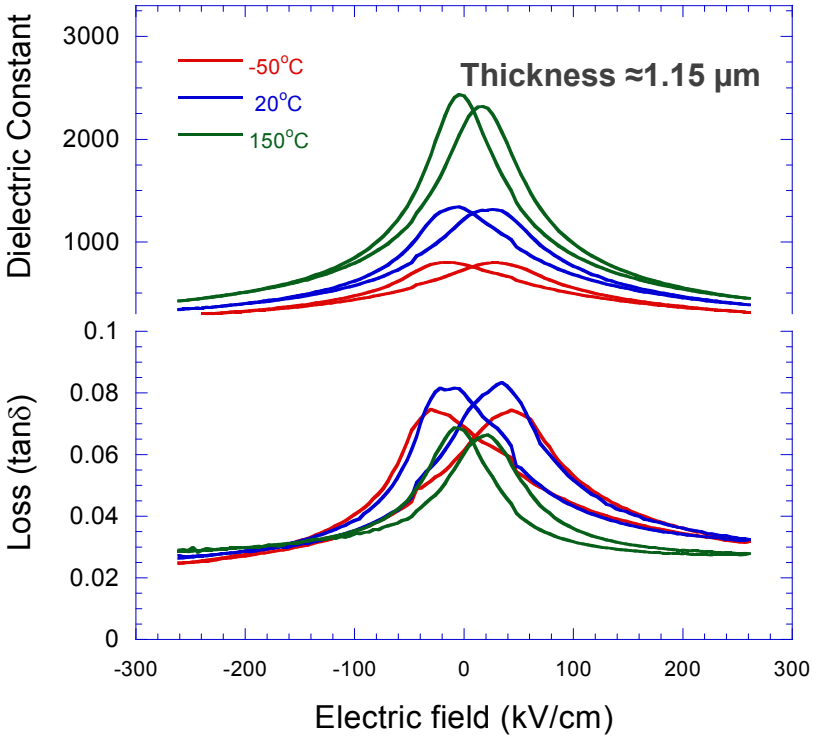
- Results on larger area (3.6 cm².; 6400X increase in area) of dielectric films with capacitance of **≈1.6 μF**
- Fabricated ≈3 μm thick PLZT film (withstood >1000 V)
- Fabricated 2" x 2" film-on-foils with large electrodes

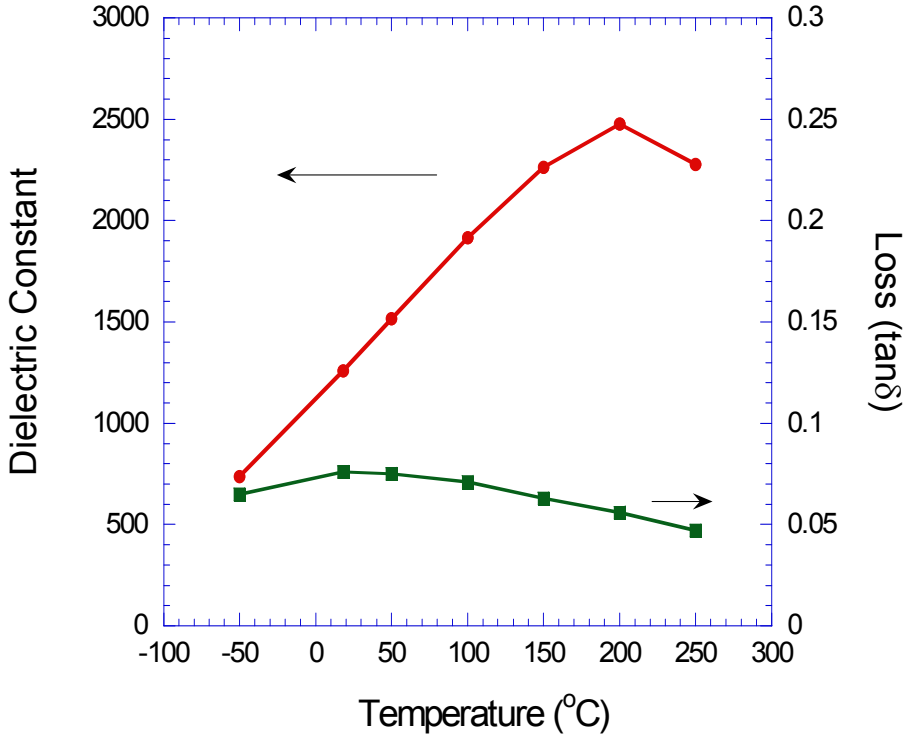




Technical Accomplishments/Results (Contd.)

Temperature dependent properties - PLZT/Ni

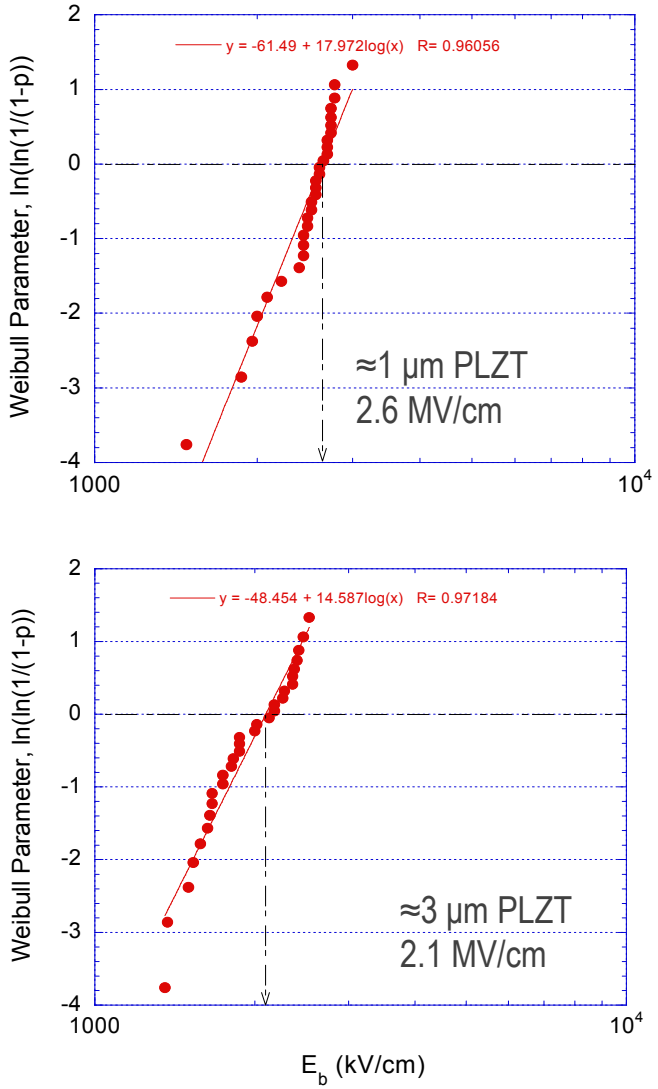




- Fabricated PLZT on Ni foils with k ≈700 & DF ≈0.07 @ -50°C; k ≈1300 & DF ≈0.08 @ room temperature; and k≈2200 & DF ≈0.06 @ 150°C; mean breakdown strength >2.0 MV/cm.
- Ferroelectric films have nonlinear dielectric constant (k) with bias field, but the k is much larger than current polymer films (k ≈6).

Technical Accomplishments/Results (Contd.)

Breakdown strength of PLZT on Ni foil – Weibull analysis

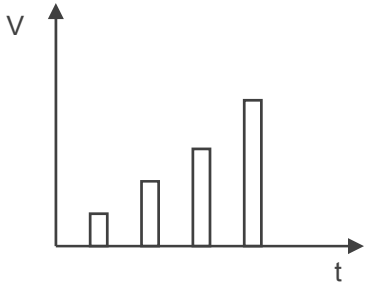


Test condition:

voltage: 100~1000V

step time: 0.5 sec

zero time: 1 sec

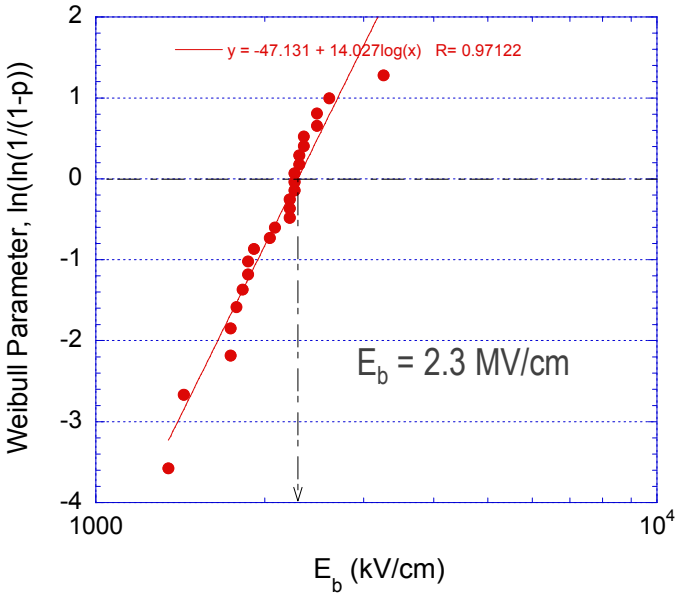


- **Higher E_b increases capacitance density and reduces dielectric layer thickness & cost of the capacitors for inverter applications.**

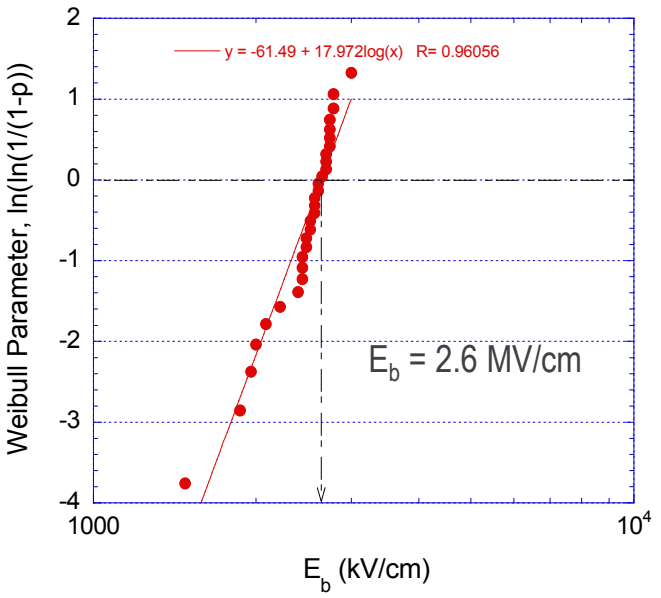
Technical Accomplishments/Results (Contd.)

Breakdown strength of PLZT films – Weibull analysis

≈1 μm PLZT on Pt/Si



≈1 μm PLZT on LNO/Ni

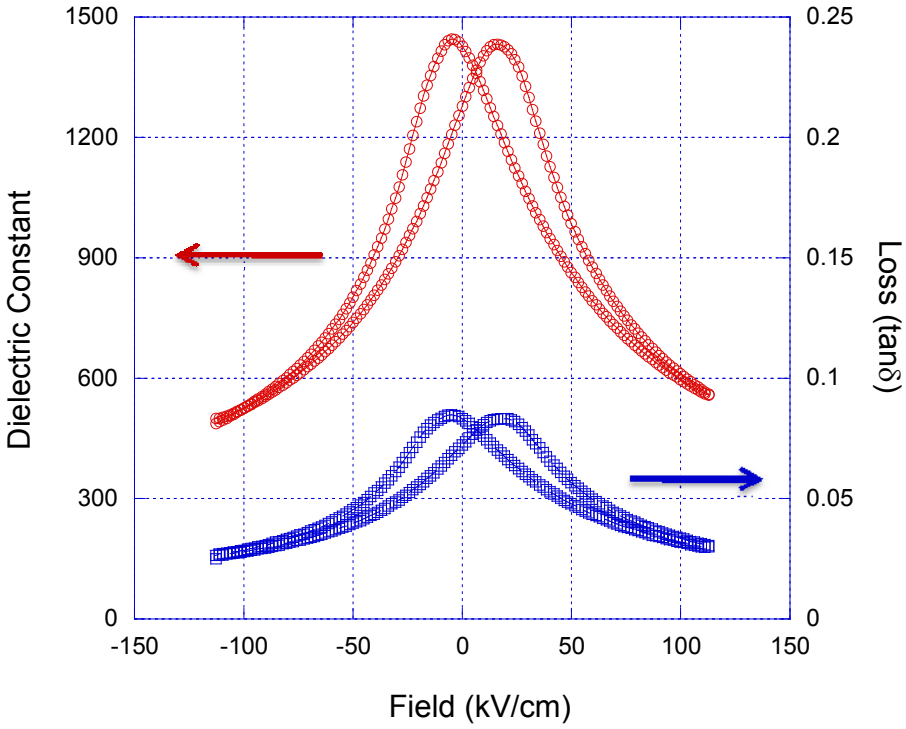


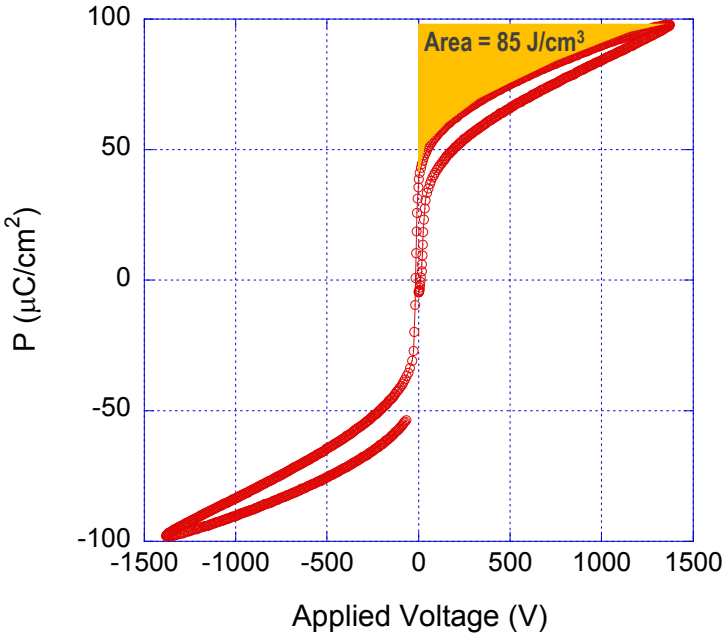
- In response to reviewer's comment last year, we measured breakdown strengths for PLZT films grown on Ni and Pt/Si substrates. The breakdown strengths are comparable.

Technical Accomplishments/Results (Contd.)

(Properties of ≈3-µm-thick PLZT film on Ni)

Measured with 750 µm electrode





Dielectric constant ≈1400 at zero bias; ≈210 @ 300 V; ≈120 @ 600 V

Measured energy density ≈ 85 J/cm³ @ 1400 V ; ≈ 15 J/cm³ @ 600 V

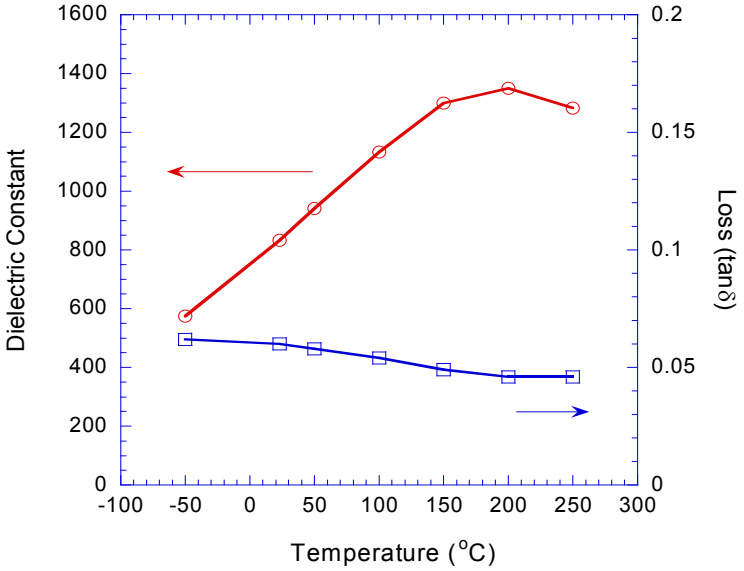
Accomplished by:

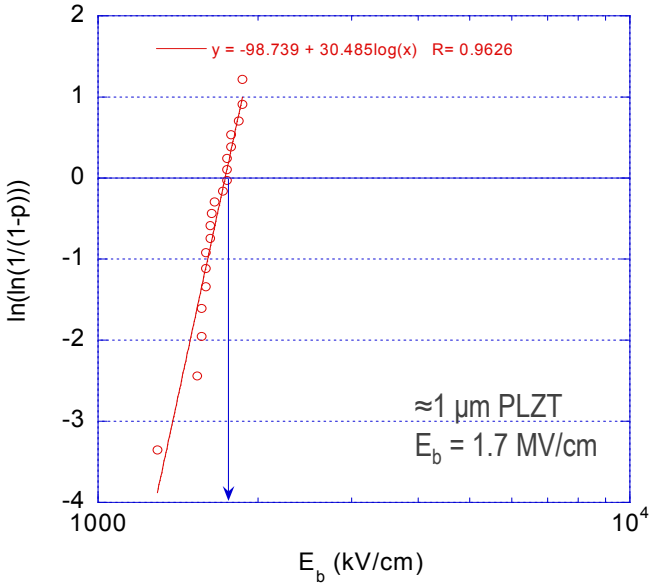
- **Control of processing temps**
- **Quality of substrates**
- **Cleanliness of surrounding area**

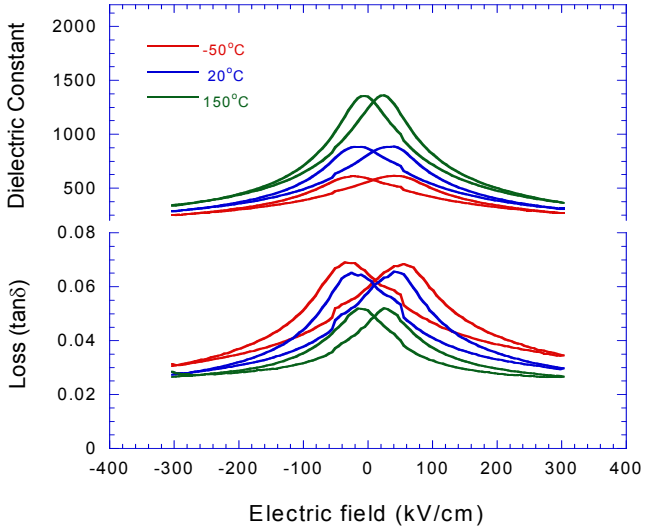
The dielectric film withstood applied voltage >1000V

Technical Accomplishments/Results (Contd.)

New solution chemistry for adaption by industry - 2MOE free



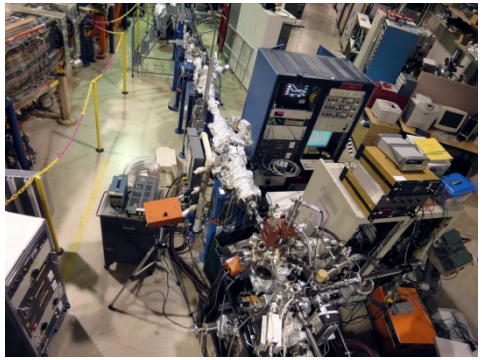
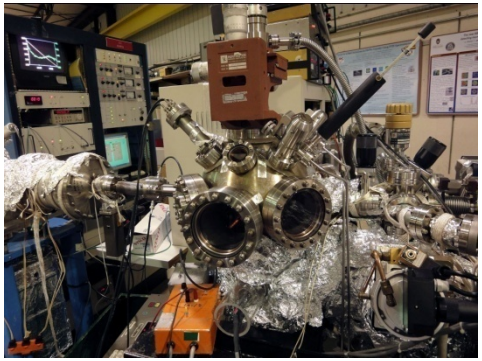




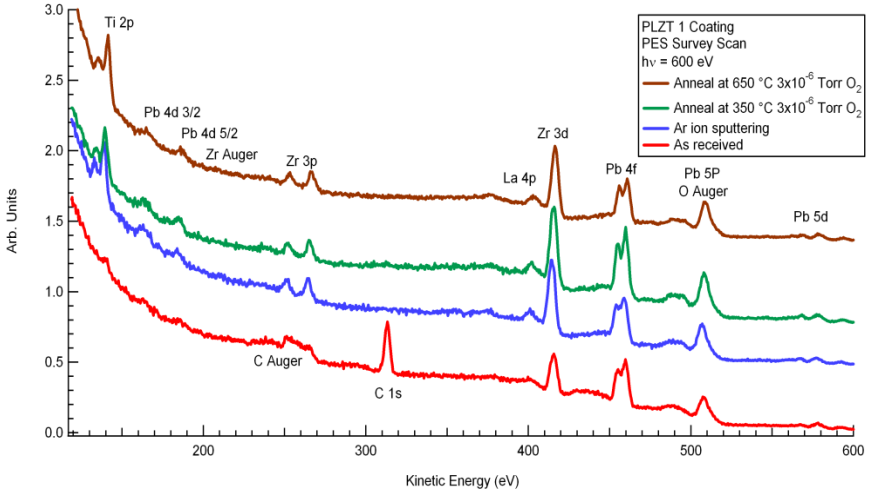
- k ≈600 & DF ≈0.06 @ -50°C; k ≈900 & DF ≈0.06 @ room temperature; and k≈1300 & DF ≈0.05 @ 150°C
- Leak current density <1x10^{-8} A/cm^2
- Mean E_b ≈1.7 MV/cm measured
- Results are comparable to 2MOE processed samples

Technical Accomplishments/Results (Contd.)

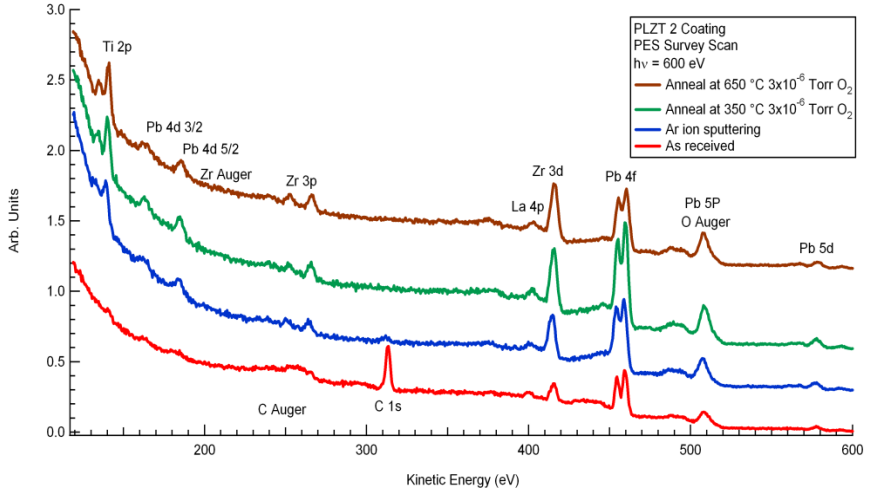
X-ray Photoemission Spectroscopy (XPS)


1 coating of PLZT grown on Pt/Si



2 coatings of PLZT grown on Pt/Si



XPS data indicate a more conductive PLZT surface layer which is Ti-deficient. This could lead to higher dissipation factor and reduced breakdown strength.

Collaboration and coordination with other institutions

Penn State University	Electrode deposition Dielectric characterization Cap. goals & test protocol
Delphi Electronics and Safety	Industry partner/CRADA
Purdue University	Nano-tech center to fabricate films
Sandia National Laboratories	Cap. goals & test protocol
Oak Ridge National Laboratory	Strain tolerance of film-on-foils
Synchrotron Radiation Center U. of Wisconsin-Madison	Synchrotron radiation experiments to understand dielectric properties
Illinois Institute of Technology	Synchrotron radiation study

Future Work

The primary emphasis for rest of FY10 and FY11 is toward advancing the proven laboratory scale film-on-foil technology and fabricating ≈10 µF, high-voltage (operating voltage 450 V) capable capacitors.

- Optimize processing conditions to produce high-voltage capable film-on-foils
  - Cleaner environment
  - Better quality substrate
  - Temperature uniformity of processing furnace/ovens
  - New solution chemistry for adaptation by capacitor industry
- Stack film-on-foils and produce ≈10 µF, 450 V capacitor
- Characterize the dielectric properties & high temperature reliability
- Identify new fabrication methodology (dip-coating, aerosol deposition, tape casting) to reduce the capacitor cost
- Investigate electrode material & architecture to achieve benign failure in multilayers (demonstrated benign failure in single layers)
- Identify industrial partner to manufacture multilayer capacitors

Summary

Developing dielectric films that has potential to reduce size, weight, and cost, concomitant with increased capacitance density & high temperature operation, for capacitors in inverters in electric vehicles.

- Demonstrated dielectric films with k >1300, E_b >2 MV/cm, and $J_{leakage}$ <10^{-8} A/cm^2.
- Measured dielectric properties in the temperature range between -50°C and 150°C. Dielectric constant increased and loss factor slightly decreased when temperature increased from -50°C to 150°C, both causing ESR to decrease.
- Fabricated ≈3.6 cm^2 area film with capacitance of ≈1.6 µF.
- Measured energy density ≈85 J/cm^3 in a ≈3 µm-thick PLZT film-on-foil; dielectric film withstood voltage >1000 V.
- Solution chemistry suitable for adaption by industry has been explored.
- Demonstrated graceful failure by self-clearing method in single layer dielectric films.
- Film-on-foil dielectrics were thermally cycled (≈1000 cycles) between -50°C and +150°C with no measurable degradation in k.
- A CRADA with Delphi was established to further develop and commercialize this technology.
- Over 35 publications and presentations have been made.