



Electro-thermal-mechanical Simulation and Reliability for Plug-in Vehicle Converters and Inverters

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Project ID # APE 026

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Overview

Timeline

- October 2009
- October 2012
- 50% Complete

Budget

- Total project funding
 - DOE - \$200K
- Funding received in FY09
 - \$ 100K
- Funding for FY10
 - \$ 100K

Barriers

Need electro-thermal-mechanical modeling, characterization, and simulation of advanced technologies to:

- Improve electrical efficiency and package thermal performance
- Permit 105 °C coolant operation
- Reduce converter cost and increase reliability.

Partners

- NIST- Electro-thermal modeling
- UMD/CALCE – Reliability modeling
- VA Tech – Soft switching module
- Delphi – High current density module
- NREL – Cooling technology
- Azure Dynamics – System Integration



Objectives of the Study



Objective: Provide theoretical foundation, measurement methods, data, and simulation models necessary to optimize power module electrical, thermal, and reliability performance for Plug-in Vehicle inverters and converters.

For FY 10:

- Validate Semiconductor Models for Soft Switching Module to improve electrical efficiency and reliability while reducing cost
- Validate Thermal Model for Low Thermal Impedance Soft Switching Module to improve package thermal performance while reducing cost.
- PoF Model and Accelerated Test Protocol Development to permit reliable operation with 105°C coolant and reduce testing cost.



The Problem



- Advanced component, package, and cooling system technologies result in complex tradeoffs that must be optimized to achieve cost, performance, and reliability goals.
- Dynamic electro-thermal simulations using physics based models are required to determine:
 - Temperatures at which the devices are functioning
 - Heating and cooling cycles within the package that can lead to package and device degradation
 - Optimal component selections and safe operating conditions
- Accelerated stress and monitoring procedures are needed to develop failure models used to predict converter life.



Uniqueness and Impacts



- **Coordinated with multiple advanced technology programs:**
 - Soft Switching Power Module being developed by Virginia Tech
 - High Current Density IGBT Package being developed by Delphi
 - Advanced cooling technologies being developed by NREL
- **Dynamic electro-thermal simulation methodology predicts detailed interactions between advanced device, package, and cooling technologies for various converter use conditions and fault conditions.**
- **Physics-based models permit dimensions, materials, and interconnections of components, packages, and cooling systems to be readily interchanged enabling optimization of complex trade-offs.**
- **Mean time to failure prediction enabled by combining:**
 - electro-thermal simulation of internal heating/cooling conditions
 - latest reliability modeling and characterization



Milestones/Decision Points



Month/Year	Milestone or Go/No-Go Decision
Jan 10	Milestone: Validate Semiconductor Models for Soft Switching Module
Mar 10	Milestone: Validate Thermal Model for Low Thermal Impedance Soft Switching Module
Apr 10	Milestone: Provide an accelerated qualification test protocol to assess empirically the effects of package degradation on electro-thermal performance of a generic module.
May 10	Go/No Go Decision: Receive Soft Switching and High Current Density IGBT modules
Jun 10	Milestone: Provide models for thermal stress related degradation and fatigue in a form that permits incorporation into dynamic electro-thermal models.
Jul 10	Go/No Go Decision: Incorporate thermal stress modeling into dynamic electro-thermal models
Aug 10	Milestone: Demonstrate Dynamic Electro-thermal Model for High Current Density IGBT Package
Sep 10	Milestone: Demonstrate Soft Switching Module Optimization
Oct 10	Milestone: Identify maximum safe current density vs. use and fault conditions in High Current Density IGBT Package
Oct 10	Milestone: Document a series of metrics for in-situ monitoring in test and in the field that can be used to quantify the effects of the package degradation on the thermal and electrical performance of a generic module.



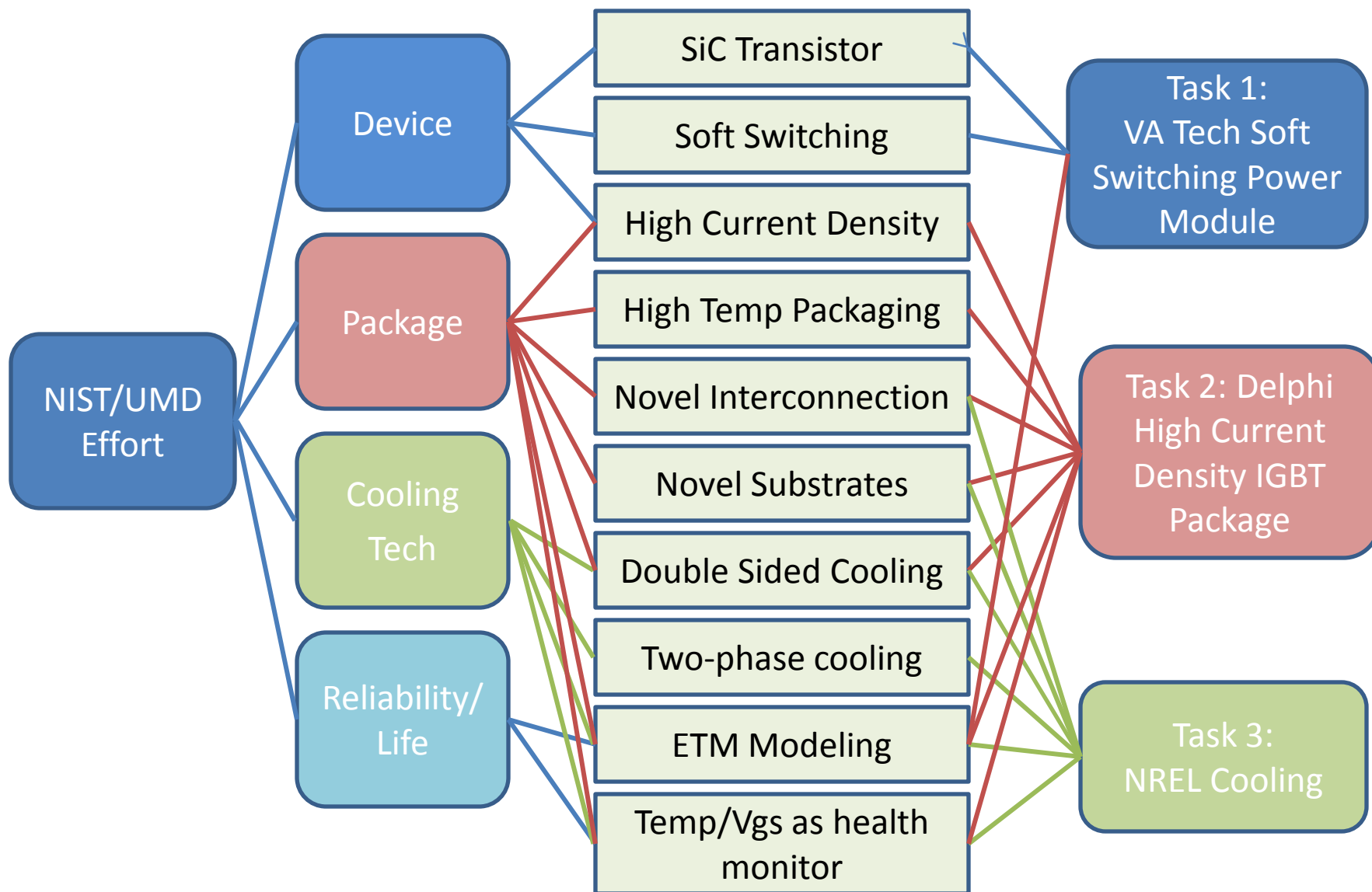
Approach

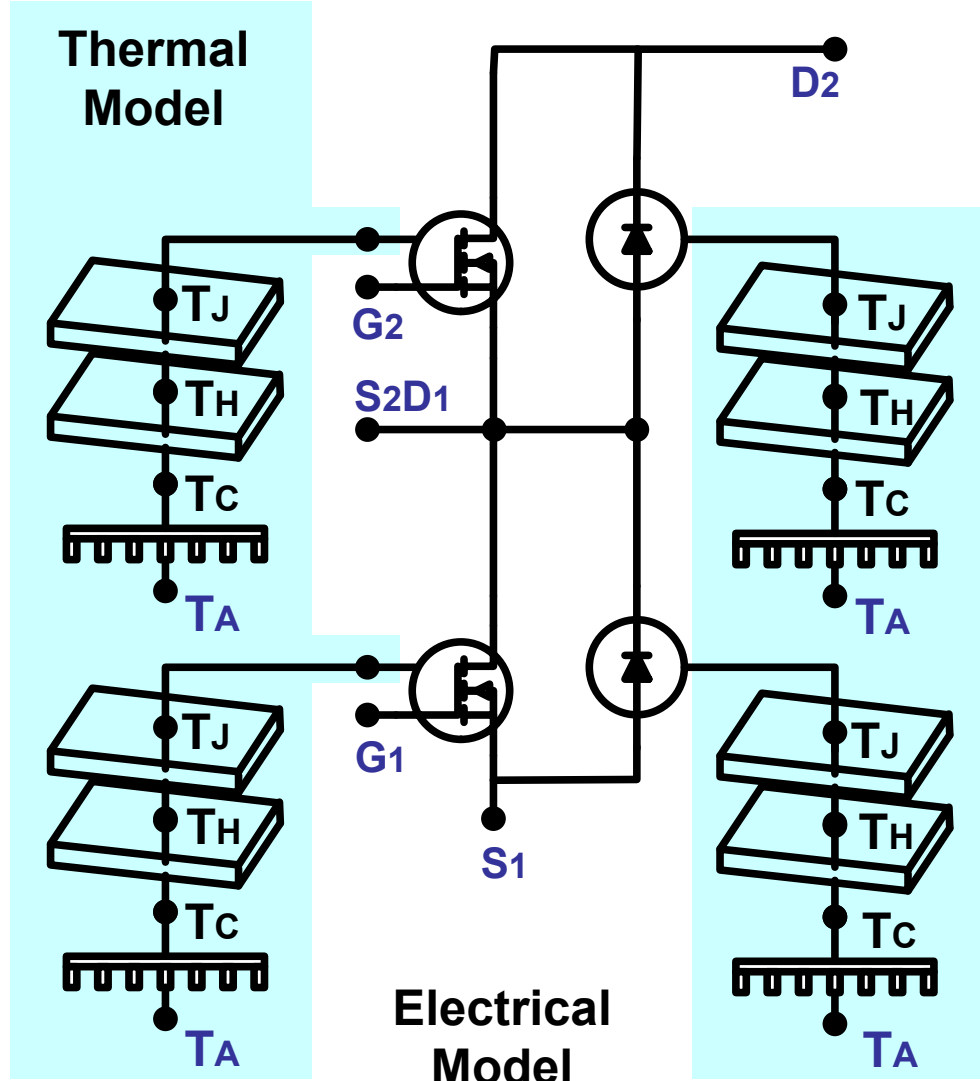


- Develop dynamic electro-thermal Saber models, perform parameter extractions, and demonstrate validity of models for:
 - Silicon IGBTs and PiN Diodes
 - Silicon MOSFETs and CoolMOSFETs
 - SiC Junction Barrier Schottky (JBS) Diodes
- Develop electro-thermal network component models and validate models using transient thermal imaging (TTI) and high speed temperature sensitive parameter (TSP) measurements to improve electrical efficiency and thermal performance while reducing cost. The following test vehicles will be used:
 - Virginia Tech low thermal impedance, hybrid soft-switching module
 - Delphi high current density IGBT package
- Perform stress and monitoring experiments and develop degradation models and accelerated testing protocols for Plug-in Vehicle package technologies to permit reliable operation with 105°C coolant and reduce testing cost:
 - Stress types include thermal cycling, thermal shock, power cycling
 - Degradation monitoring includes TTI and TSP
- Perform simulations to demonstrate utility of models in optimizing electrical and thermal performance and in predicting and monitoring converter life.



Approach: Novel Power Electronics Concepts Explored



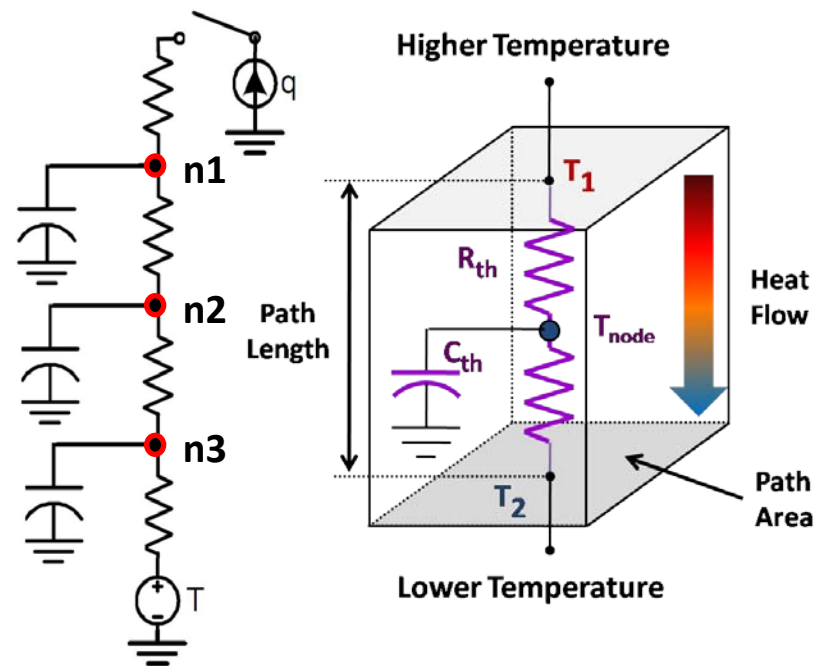
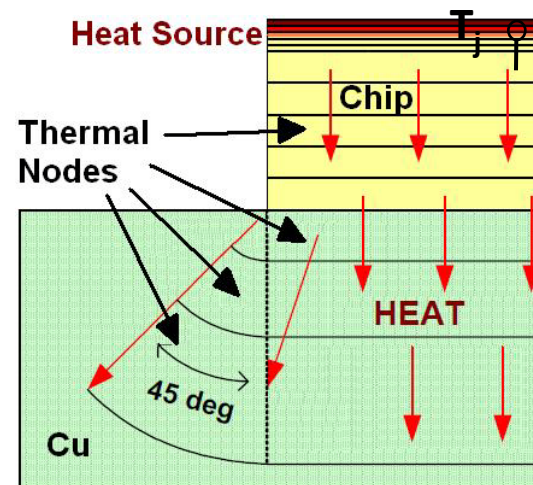
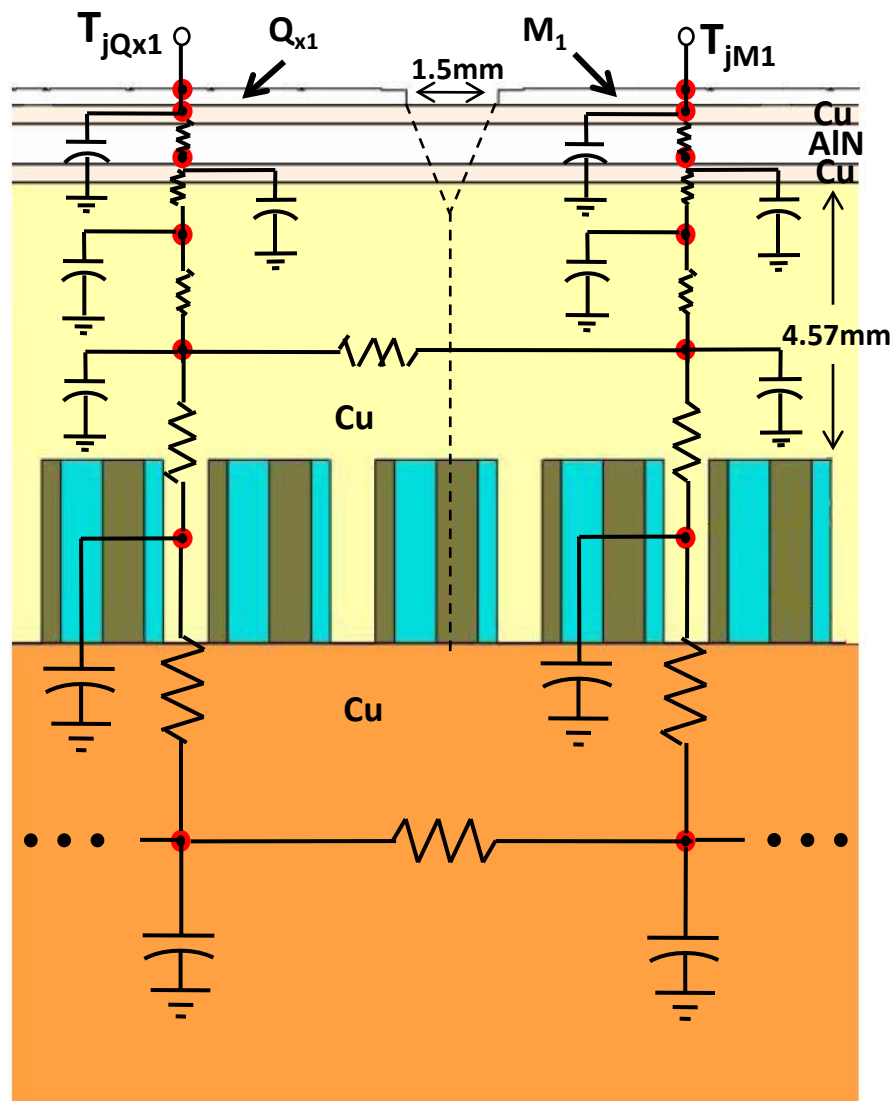


- Electrical and thermal templates for each component are developed and interconnected.

- Electrical
 - Si IGBTs
 - Si MOSFETs
 - Si PiN Diodes
- Thermal
 - Die
 - Die Attach
 - DBC Layers
 - Baseplate
 - Ambient

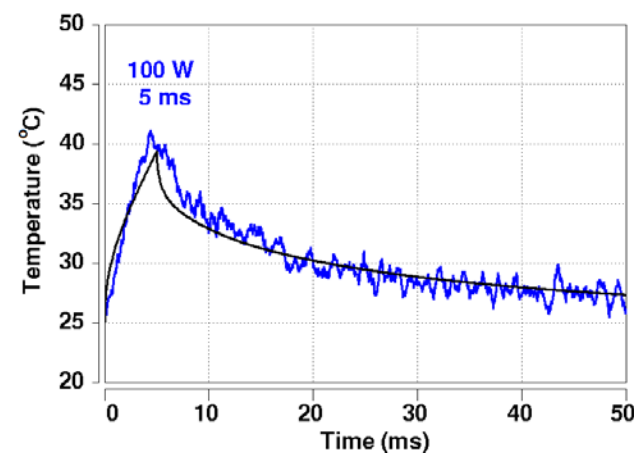
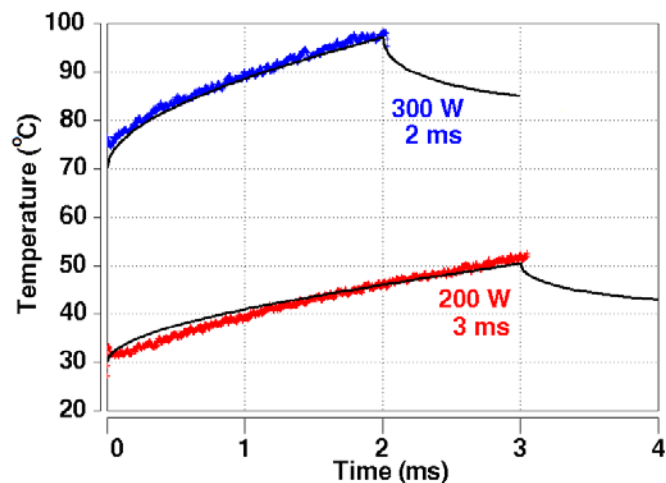
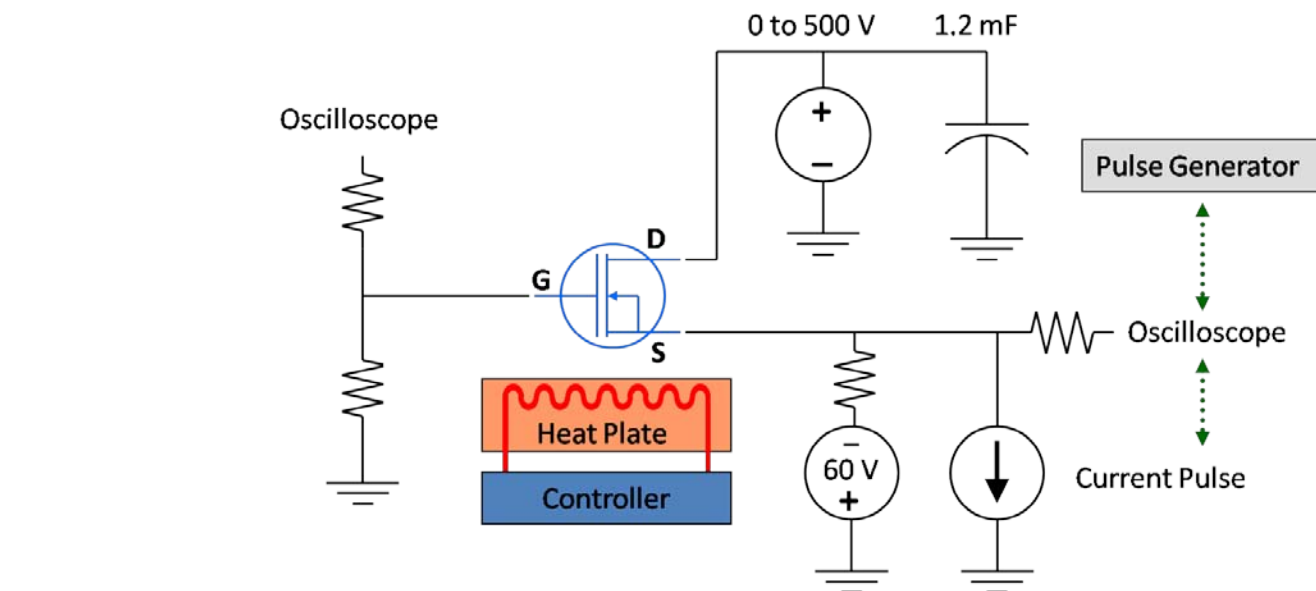
- The power dissipation in the electrical components will provide the heat for the thermal template input nodes.
- Thermal models are validated using NIST high speed transient thermal imaging (TTI) and high speed temperature sensitive parameter (TSP) measurement technologies.

Thermal Network Component Modeling Approach



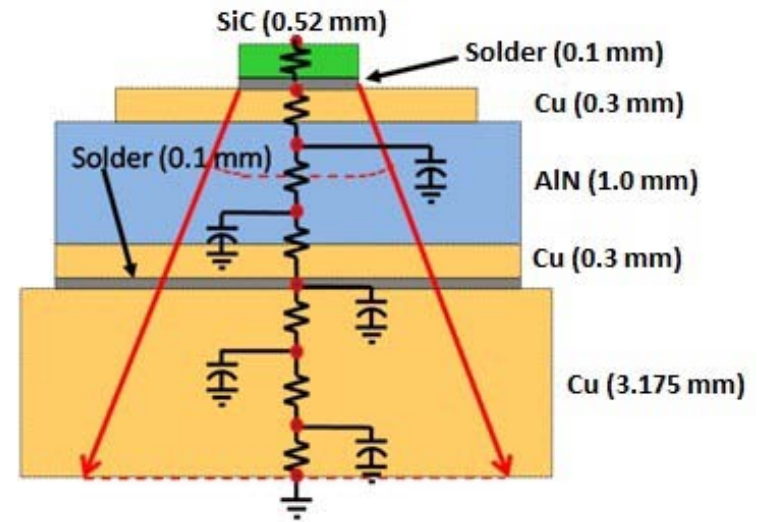


High Speed Temperature Sensitive Parameter Measurement Method



Approach: Electro-thermal-mechanical model of a generic IGBT module

- An electrothermal model is created of the IGBT module which is used to determine the heating and cooling of the device during power cycling.
- Thermomechanical stress modeling is conducted using University of Maryland physics-of-failure models to assess degradation in the package structure (die attach, DBC substrate) as a function of cycling. This degradation manifests as an increase in the thermal resistance of the damaged layer.
- The simulated junction temperature rise resulting from increased thermal resistance will be validated against actual junction temperatures measured after temperature cycling using unique NIST variable speed thermal stress and monitoring measurements. Also C-SAM, SEM, and X-ray images of the package will be used to correlate the physical attach damage to the measured temperature increase.
- The higher junction temperature rise will then be used to determine the heating and cooling of the device as well as to serve as a monitor for the health of the packaged device.



Approach: Physics of Failure Models for Power Electronic Module Degradation

- Wirebonds – primary failure site for power cycling
 - Wire flexure fatigue

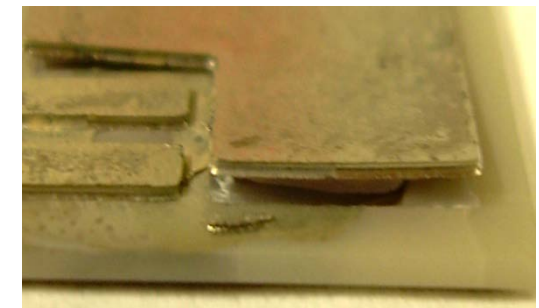
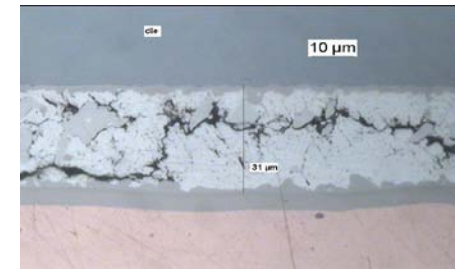
$$\varepsilon = \frac{(R - \rho_f)d\psi}{\rho_i\psi_i} \approx \frac{(\bar{r} - \rho_f)d\psi}{\rho_i\psi_i} = \frac{r(\psi_i - \psi_f)}{\rho_i\psi_i} = r(\kappa_i - \kappa_f) \quad [1]$$

- Die attach – primary failure site for narrow temperature range thermal cycling
 - Attach fracture and fatigue

$$Energy = U_e + W_p + W_c = U_{e0}N_{fe}^b + W_{p0}N_{fp}^c + W_{c0}N_{fc}^d \quad [2]$$

- Substrate – primary failure site for wide temperature range thermal cycling
 - Substrate fracture and fatigue
 - Copper delamination

$$\frac{da}{dN} = A(\Delta K)^n$$

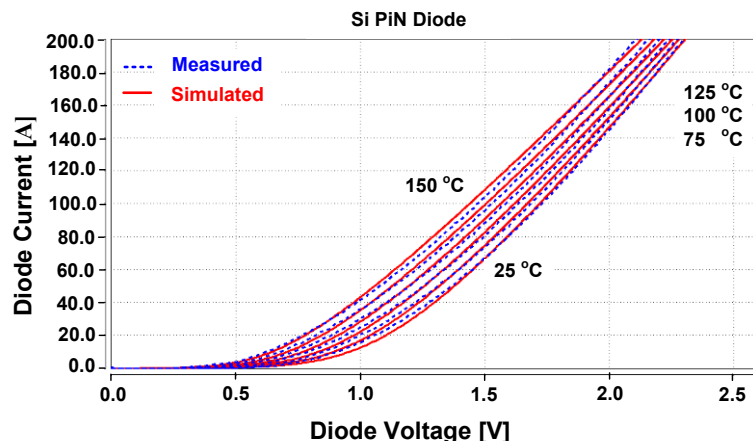




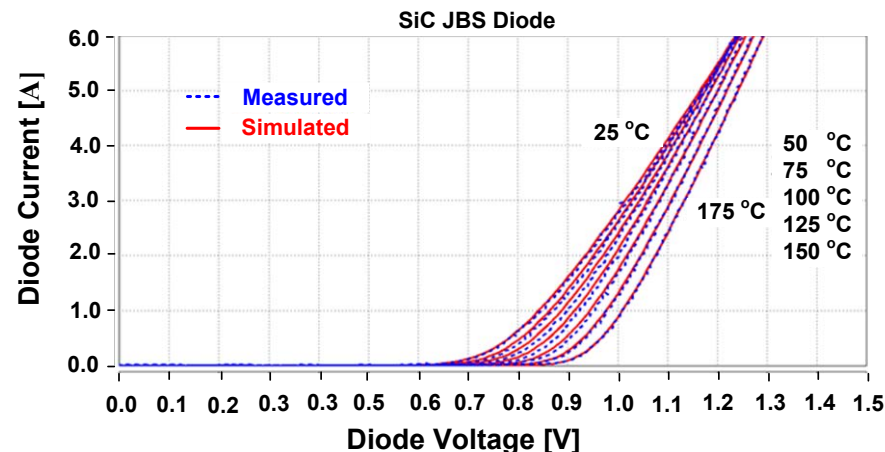
FY 10 Accomplishments



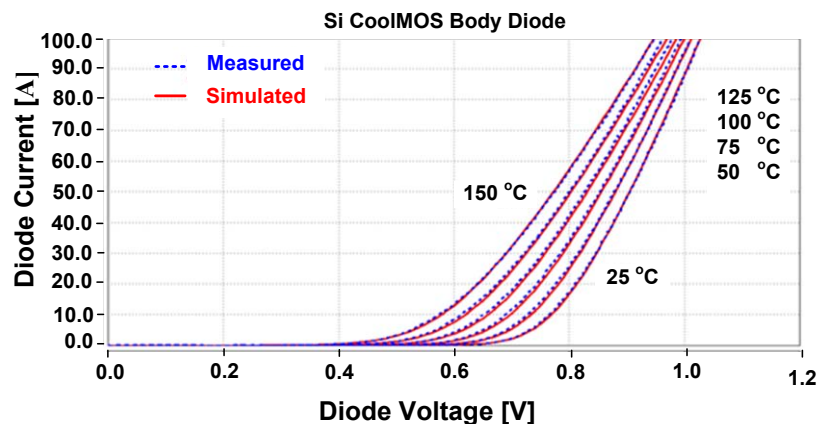
- Task 1:
 - Semiconductor Models Developed for IGBT Soft Switching devices.
 - Electro-thermal Models Developed for IGBT Soft Switching package.
- Task 2:
 - NDA signed with Delphi in March 2010.
 - Electro-thermal modeling of Delphi module initiated.
- Task 3:
 - Physics-of-failure models identified.
 - Initial time to failure calculations for attach completed.
 - Accelerated testing protocol developed.
 - Model validation underway.
 - Demonstrated ability to use TSP to monitor damage
 - Demonstrated failure in same time frame as simulation
 - Demonstrated calibration of junction temperature rise to packaging damage



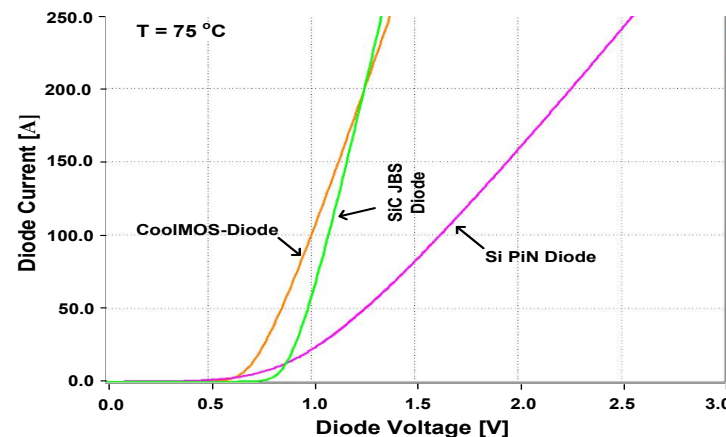
Comparison of measured (dashed) simulated (solid) output characteristics at 25 °C, 50 °C, 75 °C, 100 °C, 125 °C, and 150 °C for a 600 V, 200 A Si PiN diode.



Comparison of measured (dashed) simulated (solid) output characteristics at 25 °C, 50 °C, 75 °C, 100 °C, 125 °C, 150 °C and 175 °C for a 600 V, 6 A Si PiN diode.

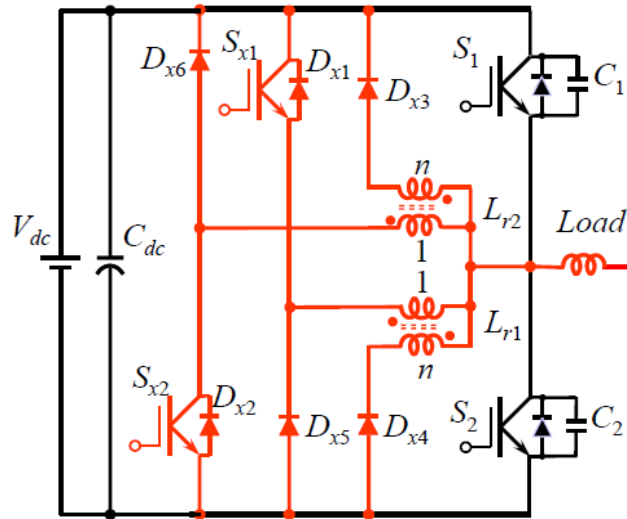


Comparison of measured (dashed) simulated (solid) output characteristics at 25 °C, 50 °C, 75 °C, 100 °C, 125 °C, 150 °C and 175 °C for the body diode of a 650 V, 60 A SiCoolMOS.

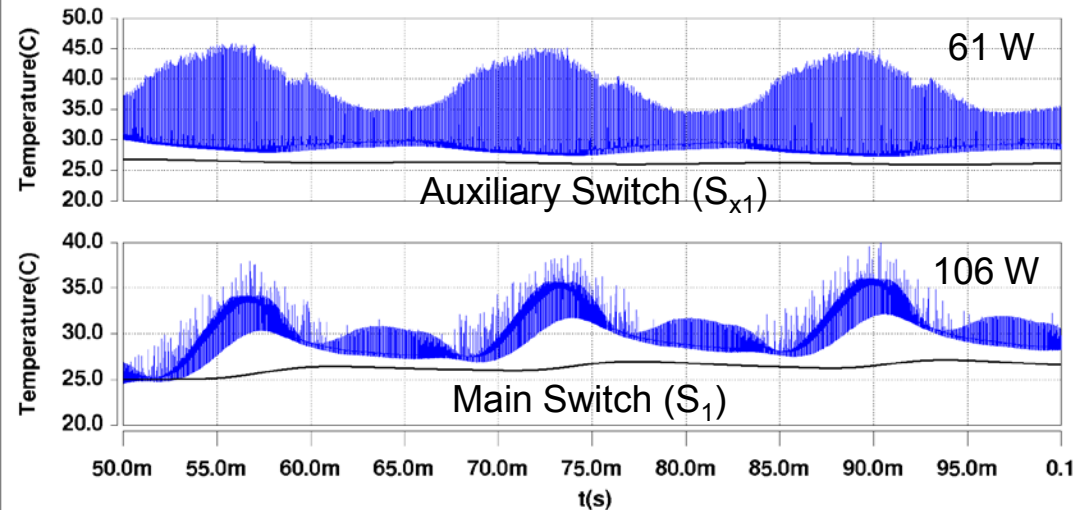


Comparison of forward characteristics for 650 V, 60 A Si CoolMOS anti-parallel diode; 600 V, 200 A SiC JBS diode; and 600 V, 200 A Si PiN diode at 75 °C.

Electro-thermal Simulation: Soft-Switching Vehicle Inverter



Freedom Car Soft
Switching Inverter
Electrical Circuit Model



Electro-thermal simulation of junction temperature
for switches undergoing half-sine wave power cycle.

Electro-thermal modeling permits the determination of both the junction temperature (blue lines) and the low frequency thermal cycling parameters for the bottom of the chip (black lines) when the surface of the chip undergoes high frequency power cycling.



Accelerated Testing for Electrothermal-mechanical Model Validation: Protocol Developed

- Fully characterize module architecture (materials and geometry).
- Procure between 3 and 10 samples for each test.
- Conduct initial analysis and validate layout and stack-up.
 - C-SAM for cracking; X-ray for void growth; Cross-sectioning for damage
- Determine temperature cycling conditions.
- Determine stress/strain on the sample for each temperature cycle.
- Conduct initial time-to-failure calculation.
- Conduct temperature cycling using NIST variable speed thermal stress cycler.
- Monitor for TSP using 450 W pulse for 10 ms at 30 cycles, and then in 100 cycle intervals.
- Convert TSP to temperature and plot ΔT vs. number of cycles.
- Take sample out periodically for analysis. (C-SAM, X-ray, Cross-sectioning)
- Identify degradation points at various percentage increase in temperature.
- Incorporate thermal degradation model into electro-thermal model.
- Validate degradation mechanism using results of the physical damage analysis.
- Model electrical performance parameters as a function of cycling time.



Development of Electrothermal-mechanical Model: Initial Time to Failure Calculations Using PoF Models



Testing Condition:

- SiC MOSFET, SiC antiparallel diode, Si series diode
- 100 μm thick Sn37Pb eutectic die attach
- Temperature from 25°C to 200°C, 20 minute cycle
- 10 min hold at 200°C, 5 minute ramp up, 5 minute ramp down
- Predicts failure should be observed around 900-1300 cycles

Using Strain-Range Approach for Sn37Pb Eutectic Solder

$$N_f = 0.5(\Delta\gamma/2\varepsilon_f)^{1/c}$$

$$c = -0.442 - 6 \times 10^{-4} T_{sj} + 1.74 \times 10^{-2} \ln(1 + (360/t_d))$$

- SiC MOSFET is 8 mm x 8 mm
 $\Delta\gamma = 0.0198 \rightarrow 1240$ cycles
- SiC antiparallel diode is 4mm x 5mm
 $\Delta\gamma = 0.0112 \rightarrow 4440$ cycles
- Si series diode is 10mm x 8 mm
 $\Delta\gamma = 0.0224 \rightarrow 940$ cycles

Using Norris – Landzberg for High Lead Solder Die Attach

$$N = \frac{30}{(\Delta\gamma)^2} \text{CPH}^{0.33} e^{(1.87 - 0.0134 T_{\max})}$$

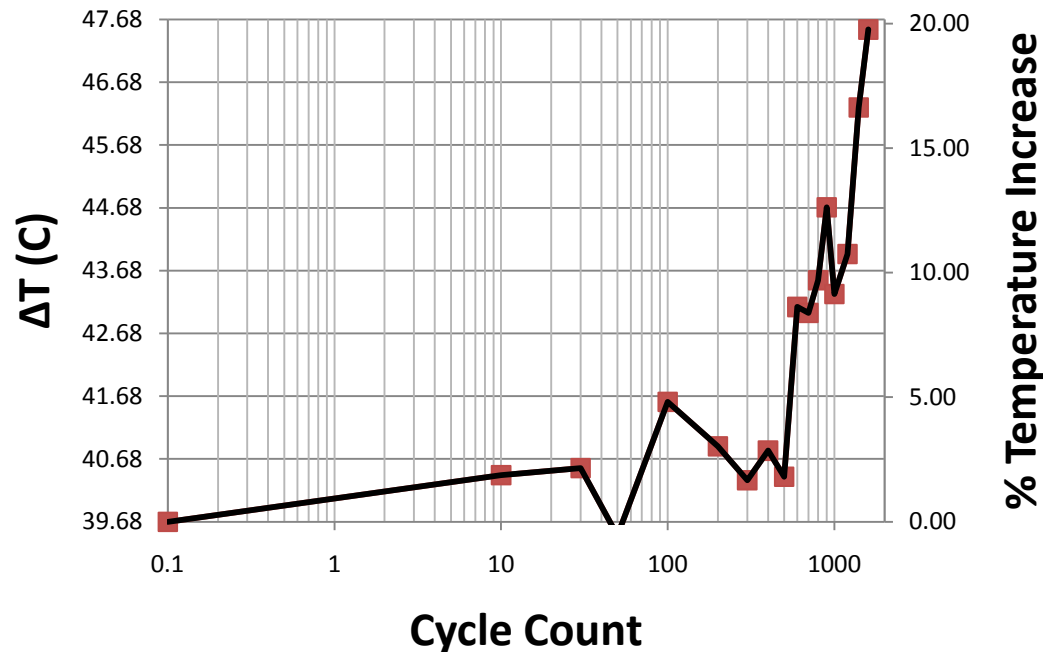
$$\text{where } \Delta\gamma = \frac{L\Delta\alpha\Delta T}{2t}$$

- SiC MOSFET is 8 mm x 8 mm
 $\Delta\gamma = 0.0198 \rightarrow 1266$ cycles
- SiC antiparallel diode is 4mm x 5mm
 $\Delta\gamma = 0.0112 \rightarrow 3956$ cycles
- Si series diode is 10mm x 8 mm
 $\Delta\gamma = 0.0224 \rightarrow 989$ cycles



Measured Increase in T_j Resulting From Temperature Cycling of a SiC MOSFET Module

C-M-37-3, 450W, 10ms
Max Temp vs. Thermal Cycles

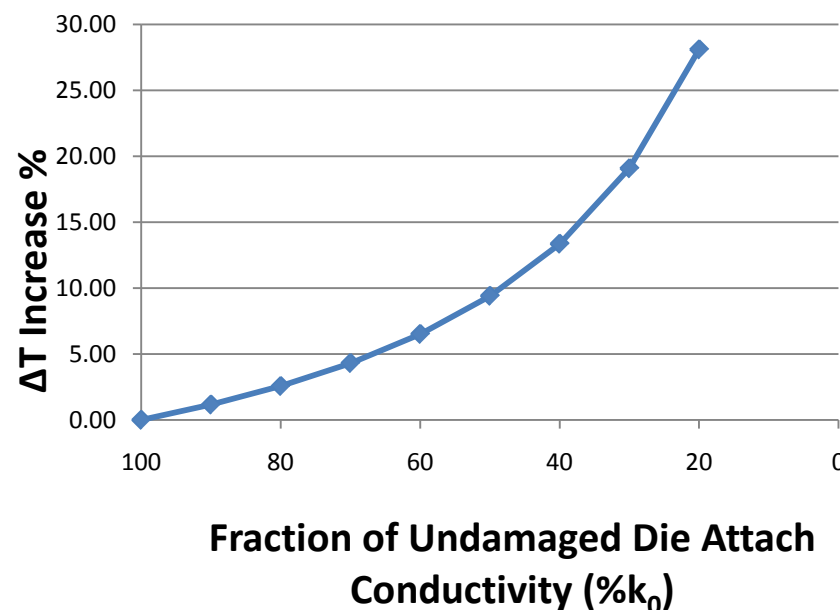
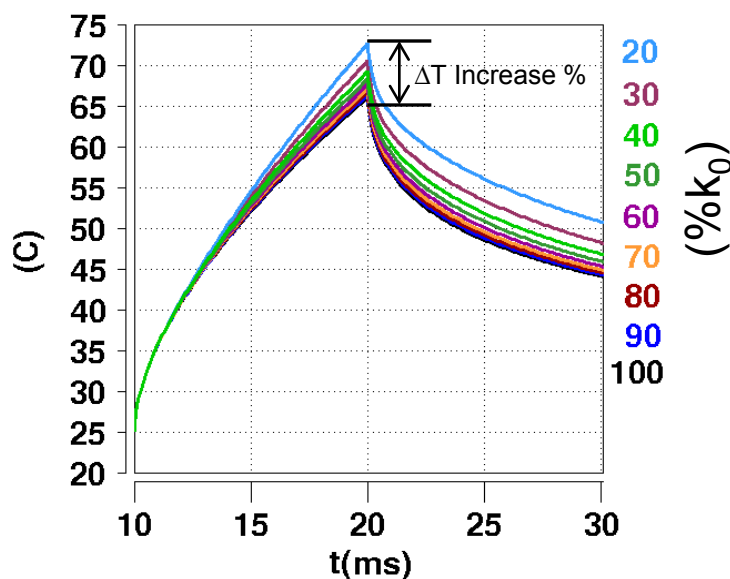
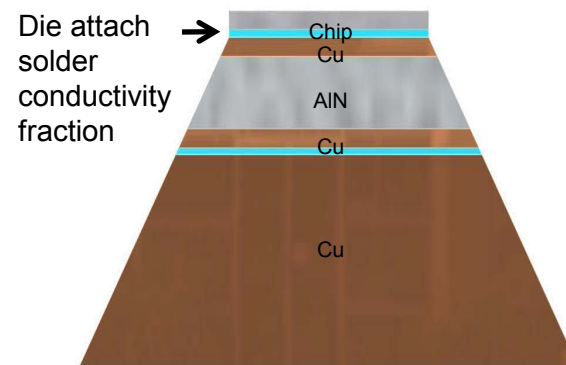


- Device surface temperature (T_j) is measured periodically during thermal cycling using High Speed Temperature Sensitive Parameter Method
- Increase in temperature after 500 cycles indicates substantial packaging damage (potentially die attach fatigue).



Thermal Simulation is Used to Correlate ΔT with Decrease in Interface Conduction

- As the package undergoes thermal cycling, the die attach degrades, decreasing its thermal conductivity.
- The decrease in die attach thermal conductivity leads to an increase in the junction temperature of the device similar to that seen experimentally.





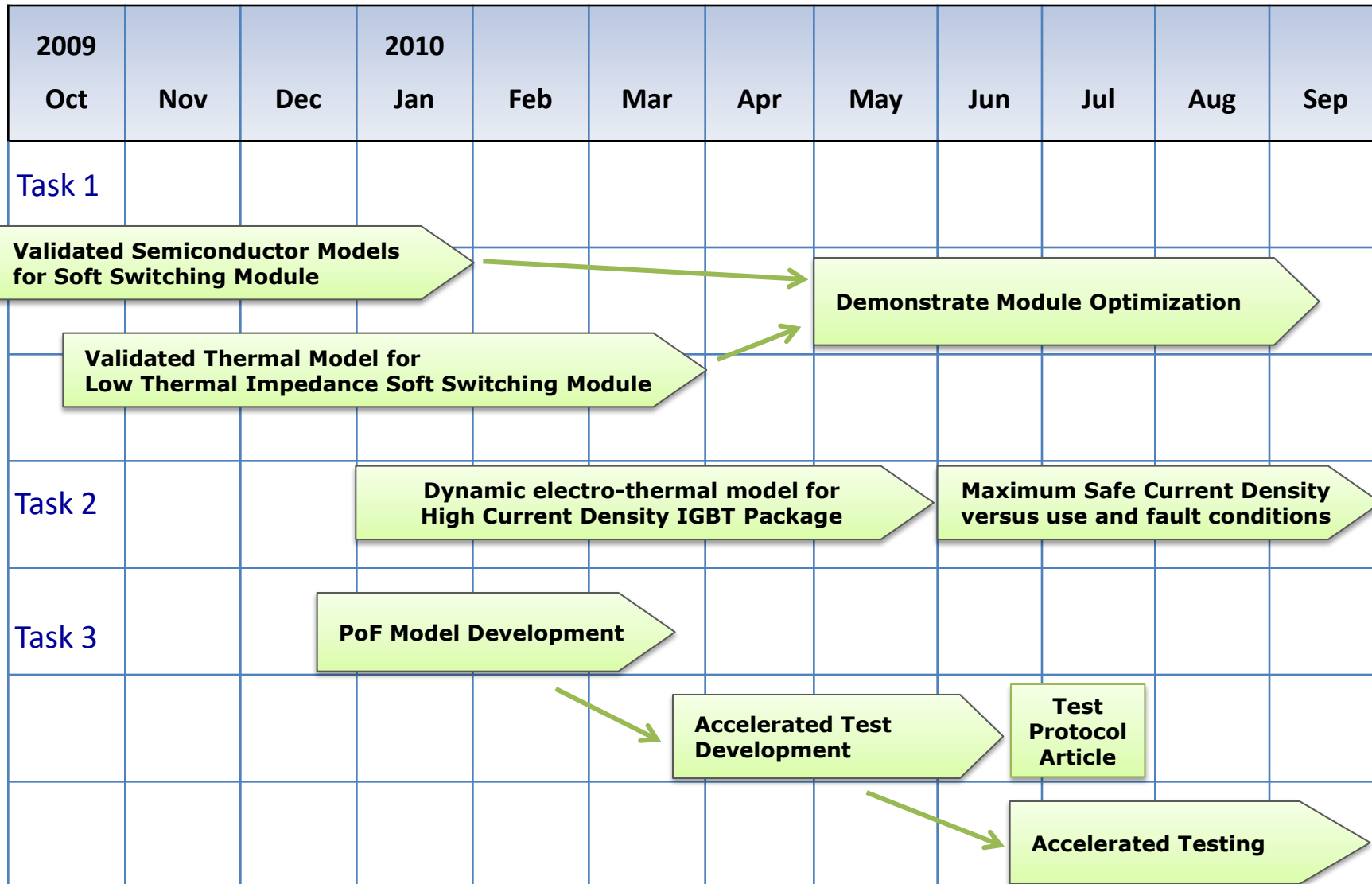
Collaborations



- NIST – (Government) – Electro-thermal models for semiconductor devices, packages and cooling; simulation for vehicle application conditions.
- University of Maryland (CALCE) – (Academic) – Providing reliability models to assess the degradation of packaging materials with time.
- Virginia Tech – (Academic) – Leads team providing low thermal impedance, high voltage SiC hybrid soft switching module for performance and reliability analysis at 105 °C.
- Delphi – (Industrial) – Providing a double-sided-cooling high current density IGBT package for performance and reliability assessment at high current density.
- NREL – (Federal Lab) – Developing and assessing cooling technologies for improved performance and reliability for 105°C coolant conditions.



FY10 Approach and Challenges





Future Work



- FY10
 - Incorporate thermal stress modeling into dynamic electro-thermal models
 - Demonstrate Dynamic Electro-thermal Model for High Current Density IGBT Package
 - Identify maximum safe current density vs. use and fault conditions in High Current Density IGBT Package
 - Document a series of metrics for in-situ monitoring in test and in the field that can be used to quantify the effects of the package degradation on the thermal and electrical performance of a generic module.
- FY11
 - Perform detailed optimization analysis for low thermal resistance, soft switching module.
 - Develop thermal network component model for air cooling system.
 - Develop electro-thermal models for advanced semiconductor devices including SiC MOSFETs and SiC JFETs.
 - Develop electro-magnetic package/system interconnect models.
- FY12
 - Include impact of air cooling and advanced semiconductors in optimization of low thermal resistance, soft-switching module.
 - Perform EMI simulations using electro-magnetic package/system interconnect models.



Summary



- The need for increased power density in advanced vehicle power electronic modules is leading to the development of new materials, devices, circuit topologies (VA Tech), packaging structures (Delphi), and cooling strategies (NREL).
- The effects of these new technologies on the performance and reliability of power electronic modules must be examined and designs optimized.
- Dynamic electro-thermal models and physics-of-failure models (UMD) based on thermo-mechanical degradation, have been developed for next generation power modules relevant to VT programs.
- Accelerated test protocols have been developed and are being used for validation of the models.
- Initial testing has confirmed increases in the temperature sensitive parameter with cycling consistent with accumulated damage in the package.
- The models will be used to set and monitor device performance metrics and to develop standards to guide the reliable insertion of technologies into next generation products.