Development, Test and Demonstration of a Cost-Effective, Compact, Light-Weight, and Scalable High Temperature Inverter for HEVs, PHEVs, and FCVs

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Project Overview

Timeline

- Start: Jan. 2008
- Finish: July 2011
- Approx. 85% complete

Budget

- Total project funding
  - DOE: $4,952k
  - Contractor: $3,258k
- DOE funding to date
  - FY08: $1,731k
  - FY09: $1,271k
  - FY10: $1,122k
  - FY11: $ 688k
  - Total $4,812k

Barriers

- Reduce system cost by 50% ($275)
  - Compatible with engine coolant (105°C), volume manufacturing, and scalable
- Reduce system volume by 50% (4.6 L)
- Reduce system weight by 50% (4.6 kg)

Partners

- Delphi: Project lead
- Dow Corning/GeneSiC: SiC-on-Si power semiconductor devices
- GE: Film capacitors
- Argonne NL: Film-on-foil capacitors
- ORNL: System modeling/simulation, power device characterization, system testing
- NREL: Thermal modeling

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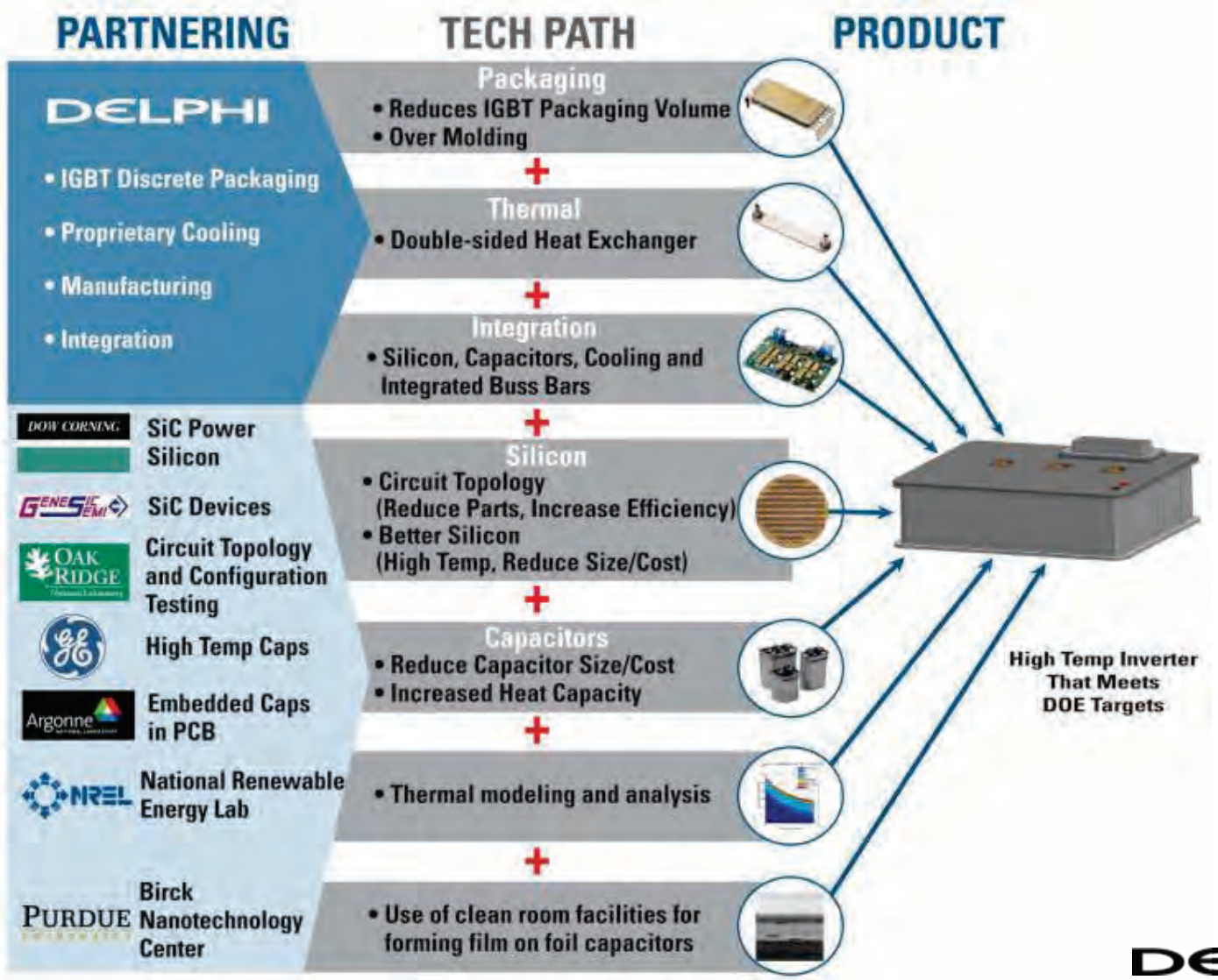
Collaboration



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Relevance: Objectives, Targets, Uniqueness, Impacts

- Objective
  - Develop, test and demonstrate a 30 kW continuous 55 kW peak inverter that can operate from the vehicle's existing coolant system (105°C), be 4.6 liters or less in volume, 4.6 kg or less in weight, manufacturable in high volumes and cost less than $275 in quantities of 100,000/year
- Targets Addressed
  - Power device packaging provides greater than 30% improvement in thermal resistance junction to coolant vs. the best commercially available product today
  - Advanced Si devices with conduction losses ~17% lower than target
  - Identifies technical path to lower cost, smaller, high-temperature bulk capacitors
- Uniqueness
  - Lower thermal resistance packaging and lower device losses enables less silicon
    - » Less silicon enables less silicon packaging, which enables smaller bulk capacitor, which enables smaller package, lower weight, easier to manufacture and lower cost
- Impacts
  - Meeting cost, size, weight and other application requirements for inverters will help the U.S. automotive industry expand the market for energy efficient and alternative energy compatible HEVs, PHEVs and EVs
    - » ***This will help reduce U.S. dependence on foreign oil and also reduce greenhouse gas emissions***

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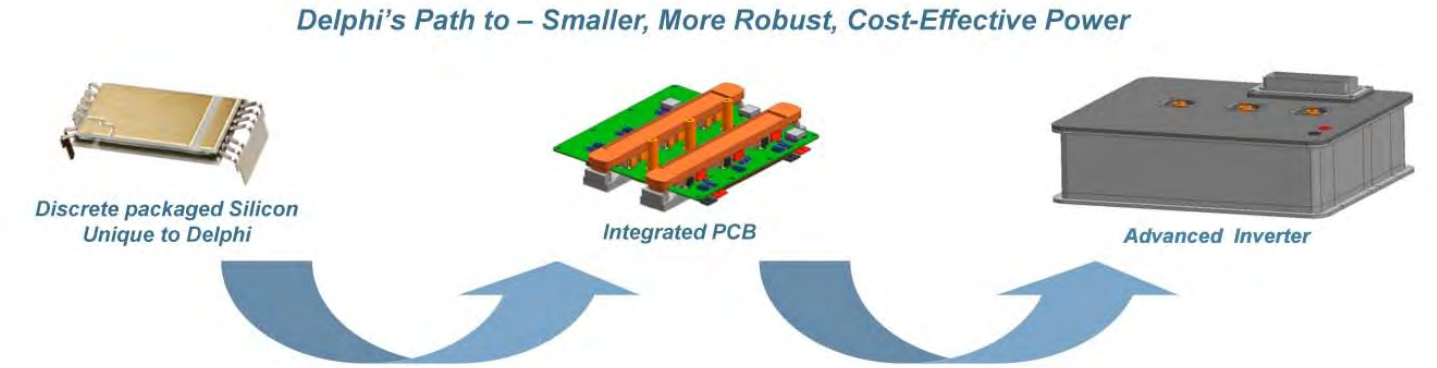
Approach / Strategy for Deployment: Description of Technology

- Unique silicon packaging
  - Higher silicon utilization
  - No wire-bonds
- High performance thermal stack
  - Cool top and bottom surfaces of the discrete power switch for Double Sided Cooling (DSC)
  - 30%+ improvement in thermal resistance junction to coolant over “best” commercially available product today
- Extruded PEI capacitor
  - Higher temperature
  - Smaller volume capable
  - Lighter weight
  - Lower cost



Delphi's Small (4.6 liters), Lightweight (< 4.6 kgs), High Temperature Inverter (105°C capable)
Showing Building Blocks: Packaged Silicon, Integrated PCB and Thermal System

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Accomplishments: 3C-SiC/Si (Dow Corning)

- Objective
  - Demonstrate functional 3C-SiC/Si diodes and MOSFETs
  - Show materials process and device process cost reduction routes to achieve DOE cost targets for inverter chip set
- Cost model updated
- Epitaxy thickness uniformity good and bow/warp in line with targets
- Demonstrated good crystal quality in CVD processes
- Delivered mechanical samples that performed well in package integrity tests using Delphi packaging technology
- Delivered SiC-on-Si wafers to GeneSiC for development of unit process steps
  - Etching development and oxide growth unit processes completed at GeneSiC
- Dow Corning is experiencing difficulty in making wafers with correct doping, due to undetermined source of N2 in CVD system
  - Current film doping is too high and does not currently meet Delphi's final deliverables needs
- First fully fabricated diode lots are projected to be completed by the end of calendar Q2, 2011

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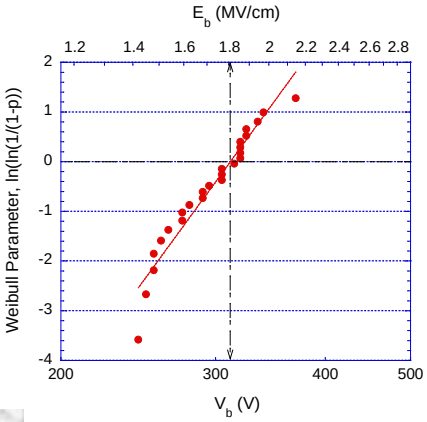
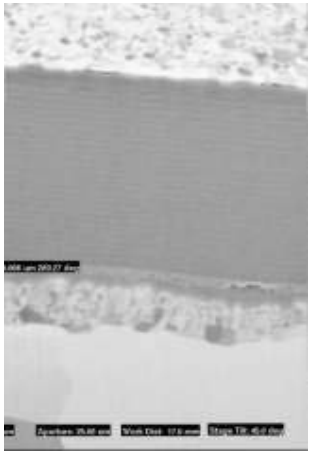
Accomplishments: Film-on-Foil Capacitors (Argonne National Lab)

- Transferred process as it exists today to a clean room facility at BNC/Purdue University
- Less variation in dielectric properties observed on samples made in clean room
- Added process controls (inspection of substrate before and after each process step)
- Moved away from polished nickel substrate to metalized silicon wafers and demonstrated good breakdown fields
- Make physically larger size capacitors
- Capacitors that are being made today are larger and better quality than earlier versions
- Still have a long way to go
- The goal is to have a better understanding of the viability of this technology, particularly to reduce capacitor cost and volume

Sample 754373: 15L PLZT/LNO/Ni with aluminum electrodes (1”x1”)





Sample 705-05-3: Thickness of the PLZT was measured at 3.066μm 600V breakdown voltage capable.

Cap Size	Room 0V Bias	+140°C 0V Bias	- 40°C 0V Bias	DK Room 0V Bias	DK +140°C 0V Bias	DK -40°C 0V Bias	Room 18V Bias	+140°C 18V Bias	- 40°C 18V Bias	DK Room 18V Bias	DK +140°C 18V Bias	DK -40°C 18V Bias
	nF	nF	nF				nF	nF	nF			
5mm	572	698	526	1975	2410	1816	220	218	208	759	753	718

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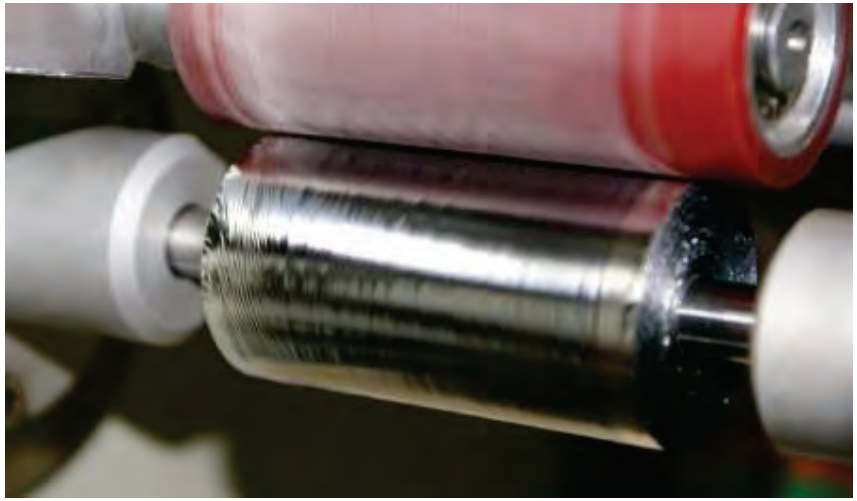
Accomplishments: Film Capacitors (GE®)

- Various resins (PEI, PPS, PC) were identified as high temperature dielectrics for capacitors
- Extrudable PEI and High Dielectric Constant (Dk) PC showed the most promise:
  - PEI film: Tg=217°C, Dk=3.2, Df=0.1%, BDS = 550-600 V/μm
  - Experimental high-heat PC: Tg=172°C; Dk= 4.0 (RT), Df<0.3% (1kHz); DS=663V/μm
- A cost vs. volume model was derived to compare the different film technologies
- Team proposes to use 5μm thick extruded PEI film to build 800μF prototype capacitors for inverters
  - High-Dk PC, while promising, requires more time to develop and will not be available in time for this program
  - Sample 0.4μF POC high-heat PC caps were made by a solvent cast process
- A 5μm PEI extruded film was qualified, metallized and turned into 1μF and 28μF POC capacitors
  - 28μF caps are being considered as modules for building the 800μF prototype caps
- Due to film thickness, the PEI capacitor will cause the inverter to exceed the volume target
  - It can be shown that, with additional development, a 4μm film capacitor could enable the inverter to meet the target 4.6L, as well as lowering cost and weight.

POC capacitor made from 5μm thick PEI extruded film



Properties of 28μF POC capacitors

Caps after leads installed (0.5" wide braid)	Flash @300 VDC	Insulation Resistance @ 200VDC (M-Ohm)	Capacitance @1kHz	Df % @1kHz	MRK (Resonance Frequency) kHz	Impedance (mΩ)
BLOCK SECTIONS	√	4,444	27.55	0.24	228	24
	√	4,545	27.66	0.24	162	4
	√	4,651	27.76	0.25	228	22
	√	4,762	27.61	0.24	115	2
Individual	√	6,061	27.86	0.25	192	12
Individual	√	6,451	27.75	0.25	192	4

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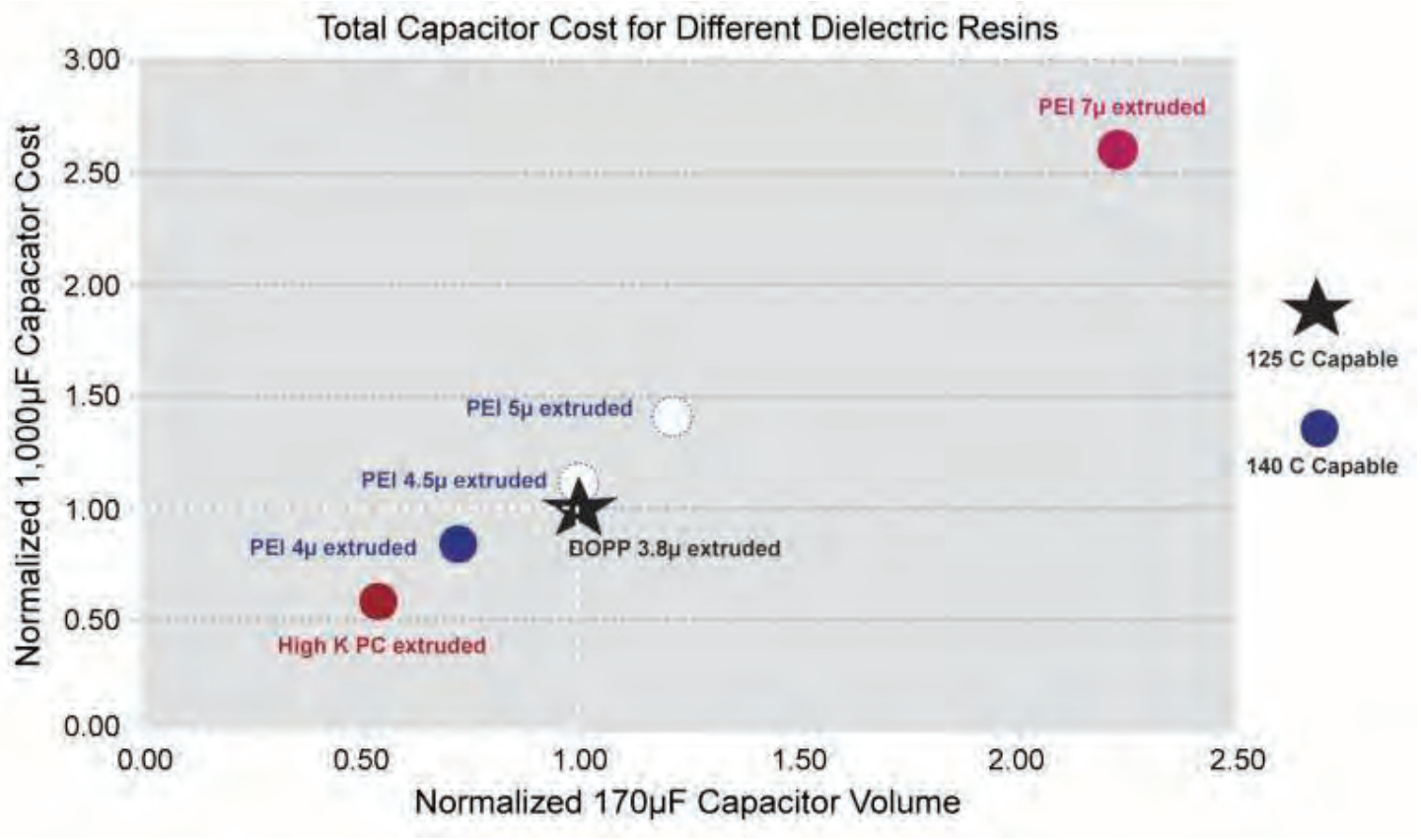
Accomplishments:
Film Capacitors (GE®)



The processing cost per unit volume of capacitor module was kept constant, the same as that for the BOPP, although it may be different for resins other than BOPP, especially in those cases in which the raw material cost or the processing cost to make the film by extrusion, or both, are substantially higher than the values assumed for BOPP;

The cost to make the High Dk polycarbonate polymer commercially was estimated based on the information presently available, and it will strongly depend on the cost to make the monomer required to build the polycarbonate molecule and the final volume of resin produced, which are both unknown at this point in time.

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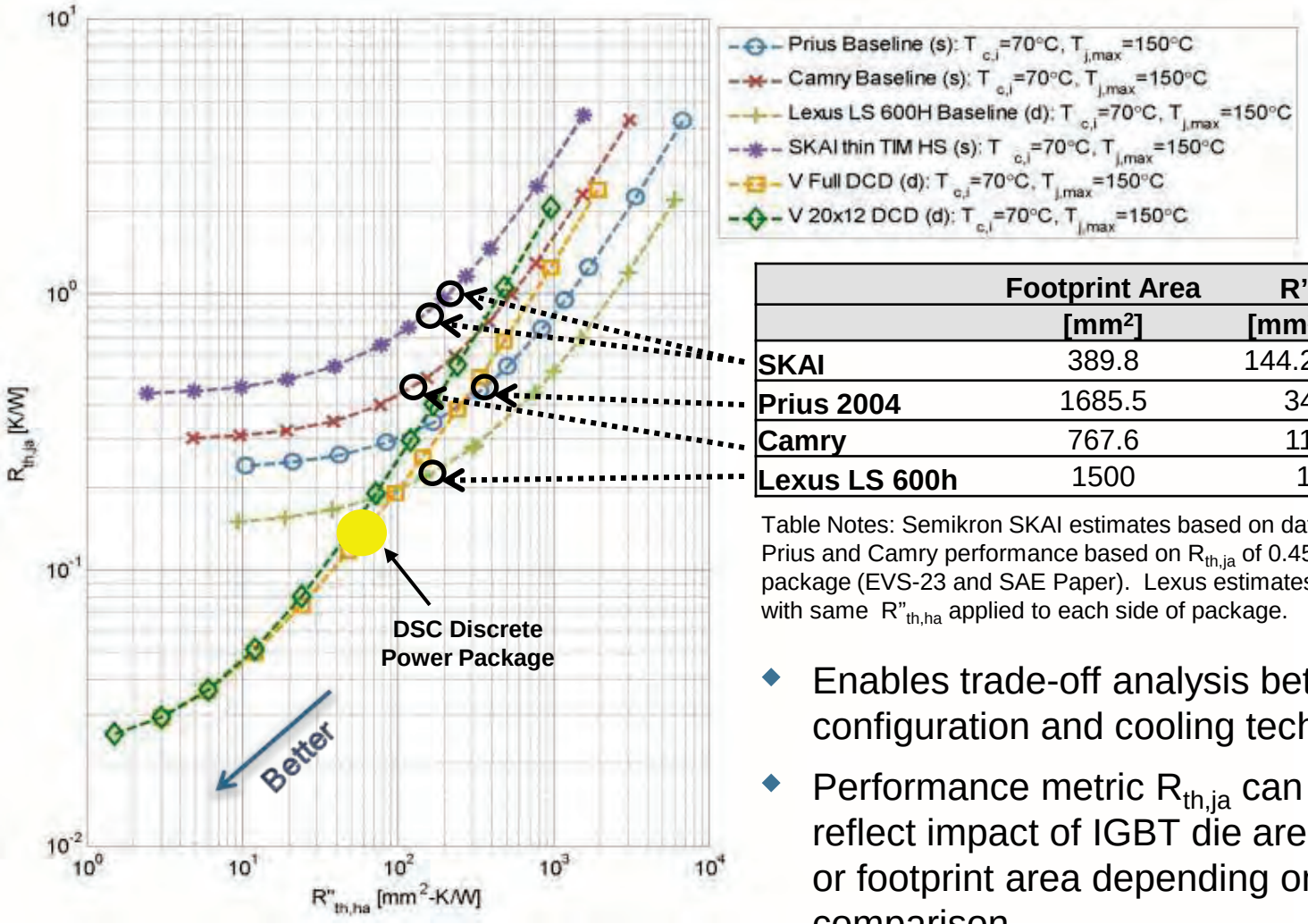
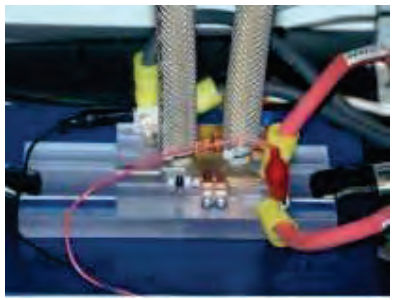
Accomplishments: Package Thermal Comparison: $R''_{th,ha}$ vs. $R_{th,ja}$ (NREL)





	Footprint Area [mm²]	$R''_{th,ha}$ [mm²-K/W]	$R_{th,ja}$ [K/W]
SKAI	389.8	144.2-206.6	0.84-1
Prius 2004	1685.5	342.2	0.452
Camry	767.6	117.4	0.452
Lexus LS 600h	1500	165	0.22

Table Notes: Semikron SKAI estimates based on data from specification sheet. Prius and Camry performance based on $R_{th,ja}$ of 0.452 K/W for a single sided package (EVS-23 and SAE Paper). Lexus estimates based on 2009 VPPC paper with same $R''_{th,ha}$ applied to each side of package.

- Enables trade-off analysis between package configuration and cooling technology
- Performance metric $R_{th,ja}$ can be adjusted to reflect impact of IGBT die area, total silicon area, or footprint area depending on the desired comparison

Note: Comparison packages contain IGBTs and diodes of different die areas.

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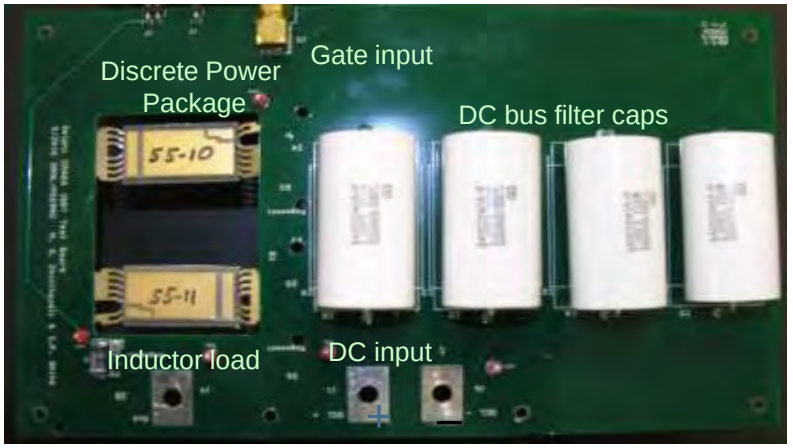
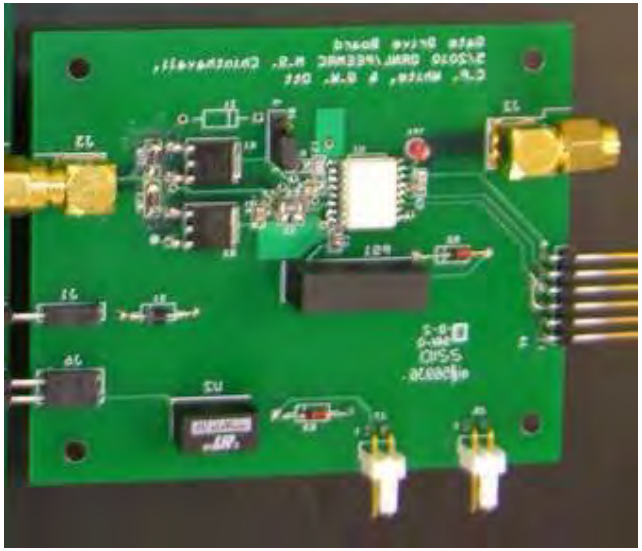
Accomplishments:
Modeling & Test (Oak Ridge National Lab)

- Dynamic tests of the Si IGBT and Si pn diode in a discrete power package were completed at temperatures from 25°C to 150°C
  - Data was obtained at 240V, 360V and 420V with current readings at 10A, 25A, 50A, 100A, 200A, 300A and 400A
- Device losses were acquired at 400A, 420V across a temperature range from 25°C to 150°C
  - The Si IGBT losses increased from 69.55 mJ at 25°C to 76.41 mJ at 150°C
  - The Si diode losses increased from 0.88 mJ at 25°C to 2.87 mJ at 150°C
- The switching loss data has been forwarded to Delphi
- The inverter test plan was completed and reviewed by Delphi, in preparation for verification testing

Power Board





Gate Drive Board

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Accomplishments: Packaging Thermal and Integration (Delphi)

- Down selection of technologies and inverter designs was completed
- Delphi has taken a medium risk / high risk dual path approach to both its power semiconductor and its capacitor technology
  - Investigated with partner Dow Corning high-risk 3C-SiC/Si vs. medium-risk silicon solutions
    - Delphi is proceeding with packaging and integration of the medium-risk advanced silicon devices
    - Current plans suggest that the high-risk 3C-SiC/Si diodes may be available for test by the end of this program, and possibly for integration into the Inverter
  - Investigated with our partners Argonne and GE advanced capacitor technology
    - The medium-risk GE extruded PEI film capacitor is showing encouraging results, but more work is needed to demonstrate the processes required for volume production of the film
      - Delphi will demonstrate this film capacitor technology in our inverter design, specifically its high temperature capability, as well as its potential for smaller size and lower cost
    - The high-risk Argonne film-on-foil approach has shown much promise for very high energy density, very small size and lower cost capacitors, but is not ready to demonstrate in commercial applications
- Modeling results from NREL have shown our double side cooling (DSC) technologies to be better than today's commercially available systems
  - Delphi will demonstrate DSC as part of our inverter design
- Topology studies conducted with ORNL have shown a non-boosted voltage source inverter topology gives us the lowest cost, smallest volume
  - Delphi's inverter will use a voltage source topology

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Accomplishments: Packaging Thermal and Integration (Delphi – cont'd)

- Non-optimized, scalable solution for multiple applications
  - Meet DOE performance requirements
  - Scalable, capable of operating over a wide range of applications
    - Capable of 80A to > 300A / phase output
    - Parts delete and part substitution
  - Utilize Advanced Si with improved heat sink
    - Characterized static and dynamic performance of advanced silicon devices over temperature (25°C and 150°C)
      - Conduction losses show substantial reduction vs. baseline and target
      - Switching losses can be optimized to minimize total losses for a given drive cycle
  - Utilize 105°C engine coolant
    - Double sided cooled discrete power switch
    - Using light weight high performance heat rails
    - Thermal performance characterized with 105°C coolant
  - Utilize high performance phase change material
  - Utilize scalable high current connection system
  - Utilize PP or extrudable PEI capacitor
    - PP will not meet the temperature requirements but does meet the volume target
    - PEI will meet 140°C temperature requirement but does not meet the volume targets

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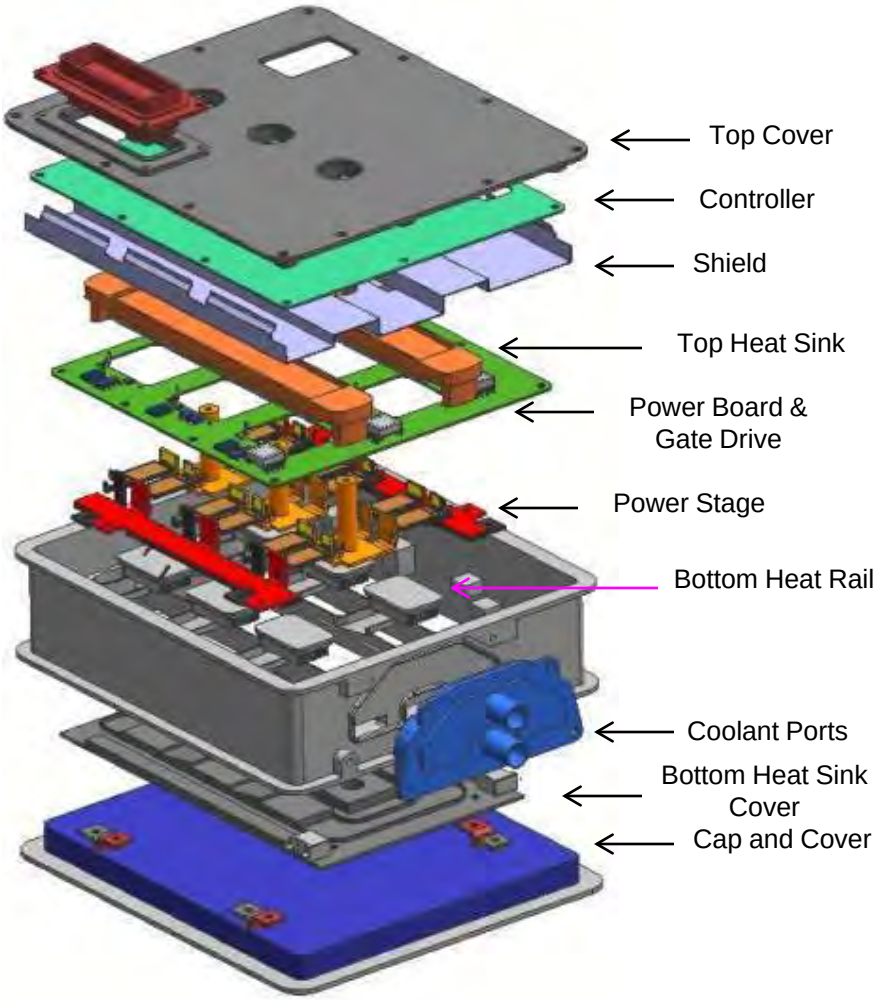
Accomplishments:
Packaging Thermal and Integration (Delphi – cont'd)

- Completed system design
- Schematics complete and reviewed
- Circuit boards currently in layout
- Parts on order
- Lab setup for bench testing in process
- Dyne time has been scheduled



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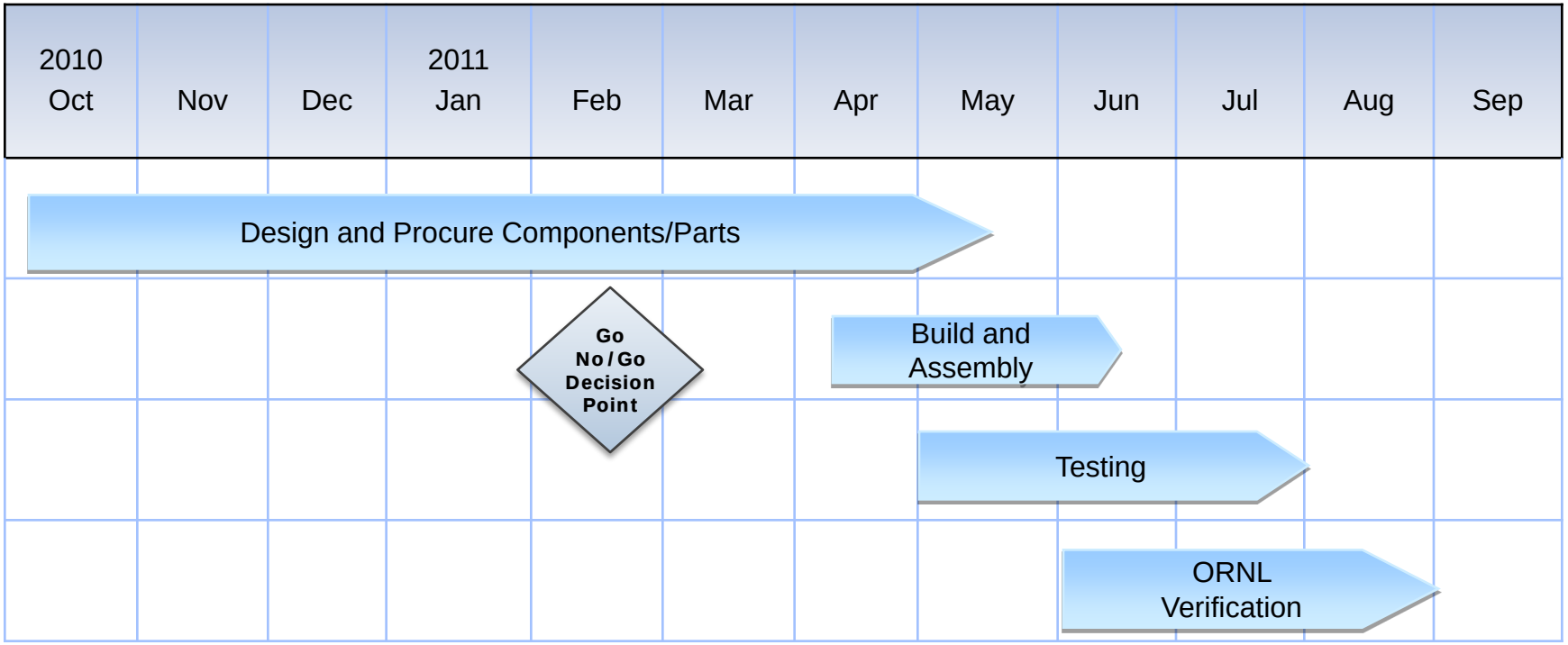
Future Work/Activities (FY11)



Go No/Go Decision Point: Go No/Go decision point on the inverter build

Challenges/Barriers: Microprocessor and electronic component availability, connector system, PEI capacitor, 3C-SiC/Si

Proposed Future Work/Activities:

Build and test inverter
Package and test 3C-SiC/Si diodes
Invite ORNL to do verification testing of the inverter
Deliver the inverter to the DOE

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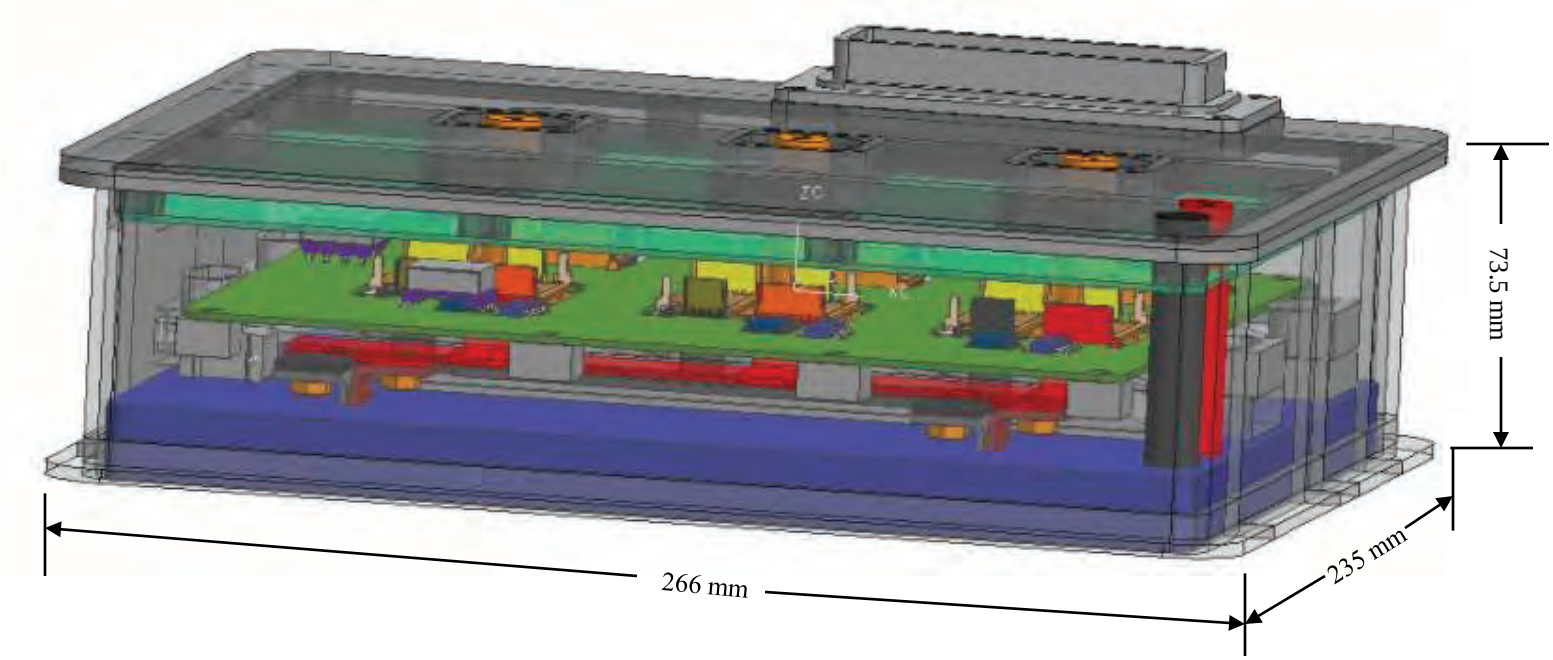
Summary

Inverter design is scalable and flexible
to accommodate different vehicle configurations



Smaller Package Volume – Lower Weight – Easier to Manufacture – Lower Cost

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