NREL
NATIONAL RENEWABLE ENERGY LABORATORY

Integrated Module Heat Exchanger

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Overview

Timeline

Project Start Date: FY 2012

Project End Date: FY 2013

Percent Complete: 30%

Barriers and Targets

- **Cost**
- **Performance (Power Density)**

Budget

Total Project Funding:

DOE Share:$200K (FY12)

Funding Received in FY11: $0K

Funding for FY12: $200K

Partners

- Interactions / collaborations
  - Sapa
- Project lead
  - National Renewable Energy Laboratory

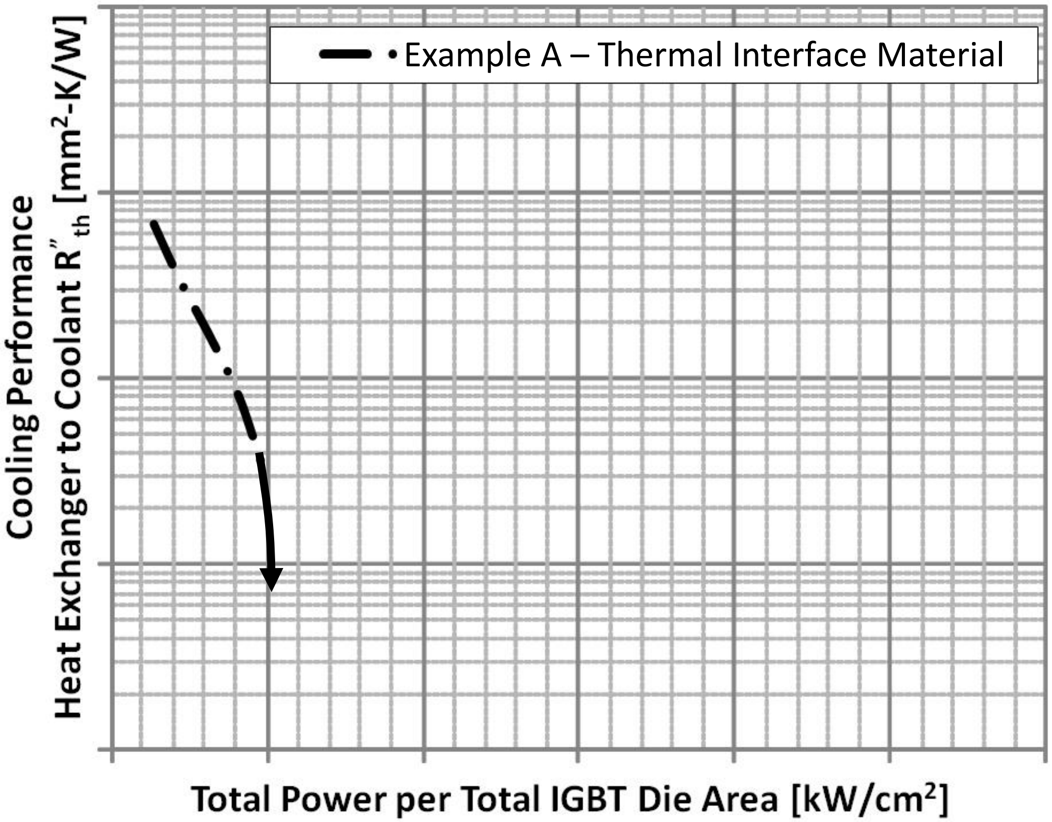
Relevance/Objectives

Problem: Cost, Volume, and Weight

"Easy ways to increase output power are paralleling more silicon chips and/or step-up the die size to increase current capacity. But this strategy is unaffordable in terms of both increased chip cost and packaging space." (2007) [1]

Primary Concern: Heat

"The most significant concern for increasing current is intensified heat dissipation in the silicon chips" (2007) [1]



[1] Source: Yasui, H., et al., "Power Control Unit of High Power Hybrid System" – Denso and Toyota, SAE 2007-01-0271

Relevance/Objectives

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Primary Concern: Heat

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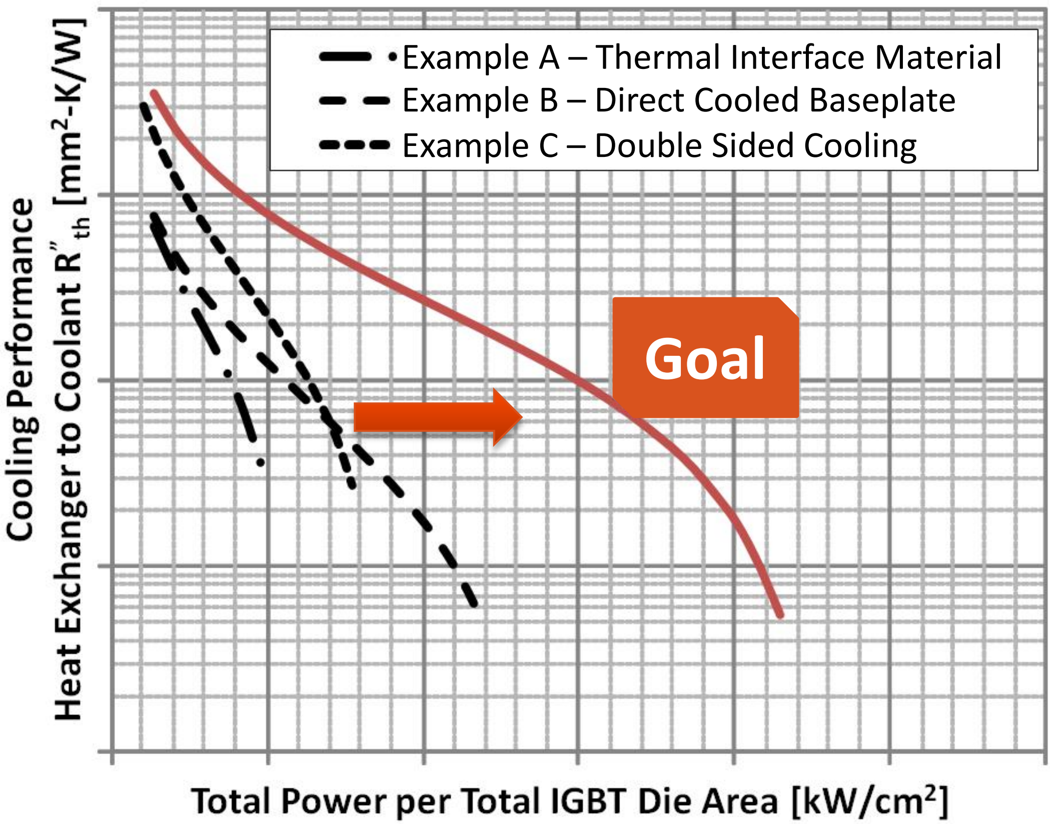
Current Technology:

Packaging and cooling developments have improved heat removal to increase power capability (power per die area)

Goal:

Improve heat dissipation to improve power per die area (cost)



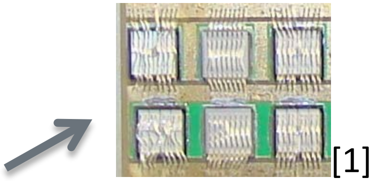
[1] Source: Yasui, H., et al., "Power Control Unit of High Power Hybrid System" – Denso and Toyota, SAE 2007-01-0271

Relevance/Objectives

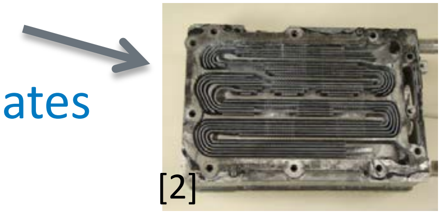
Objective

- Design and build a prototype heat exchanger module that improves power per die area capability while enabling low cost and scalable heat exchanger technologies

Addresses Targets


[1]

- Reduces cost by:
  - Improving the power per die area by 100%
  - Introducing a modular and scalable thermal approach to reduce the need for custom heat exchanger redesigns as applications scale in power
- Reduces weight by eliminating large heat exchanger cold plates
- Maintains best-in-class power density capabilities


[2]

Uniqueness and Impacts

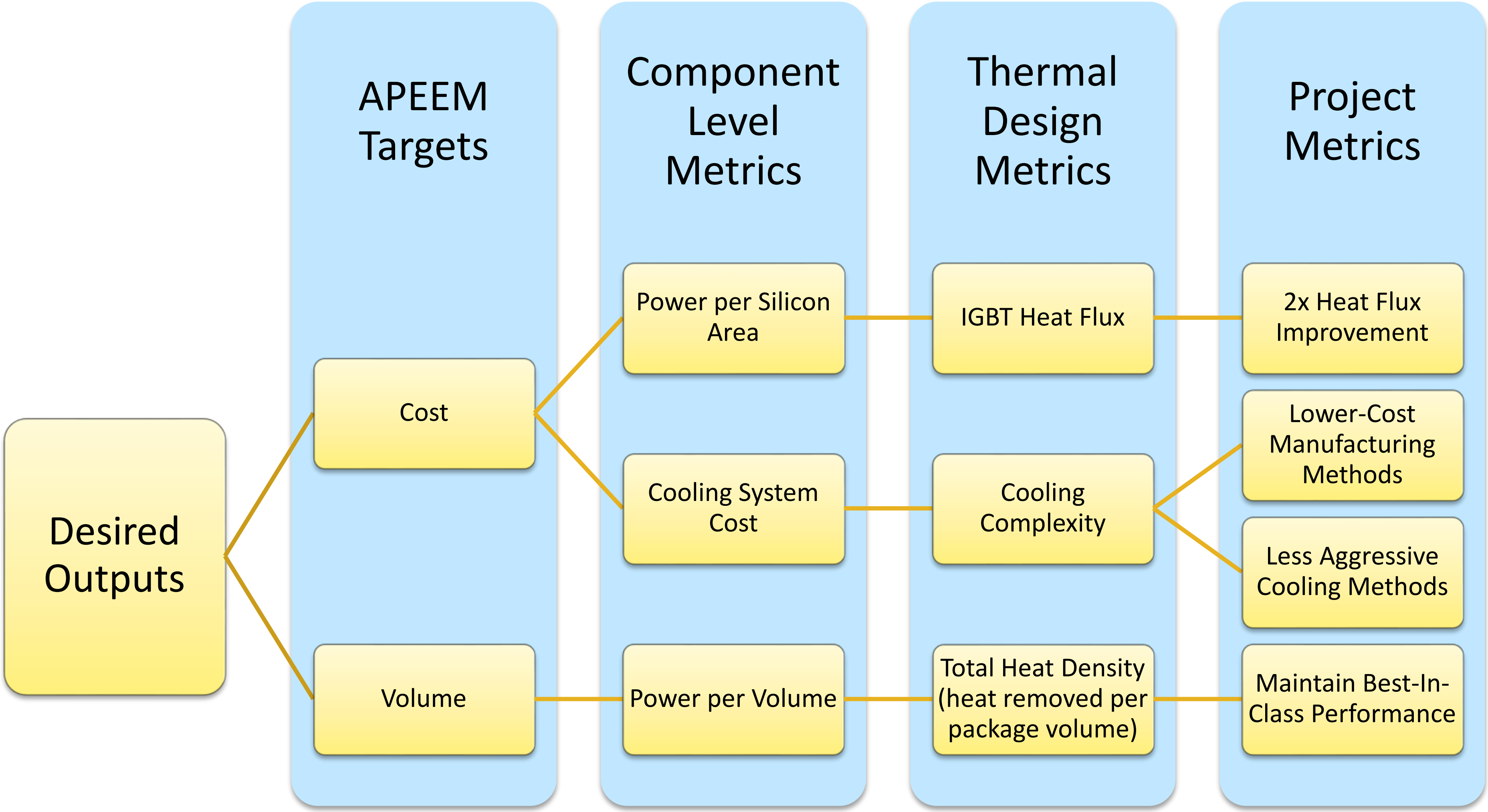
- Technology is scalable to liquid-cooled systems and air-cooled systems
- Research will improve liquid and air cooling of power electronics

[1] Credit: Mark Mihalic, NREL
[2] Credit: Kevin Bennion, NREL

Milestones

Date	Milestone or Go/No-Go Decision
September 2011	Internal Milestone: • Patent application submitted
February 2012	Go/No-Go: • Computer simulations of design match preliminary analysis expectations and justify hardware prototype development
April 2012	Internal Milestone: • Finalize initial prototype design
September 2012	DOE Milestone: • Complete hardware tests on prototype • Submit report on design and test results Go/No-Go: • Prototype heat exchanger hardware matches design expectation • Proceed to second project phase to integrate with power electronics package

Approach/Strategy



Desired Outputs

APEEM Targets

Cost

Volume

Component Level Metrics

Power per Silicon Area

Cooling System Cost

Power per Volume

Thermal Design Metrics

IGBT Heat Flux

Cooling Complexity

Total Heat Density (heat removed per package volume)

Project Metrics

2x Heat Flux Improvement

Lower-Cost Manufacturing Methods

Less Aggressive Cooling Methods

Maintain Best-In-Class Performance

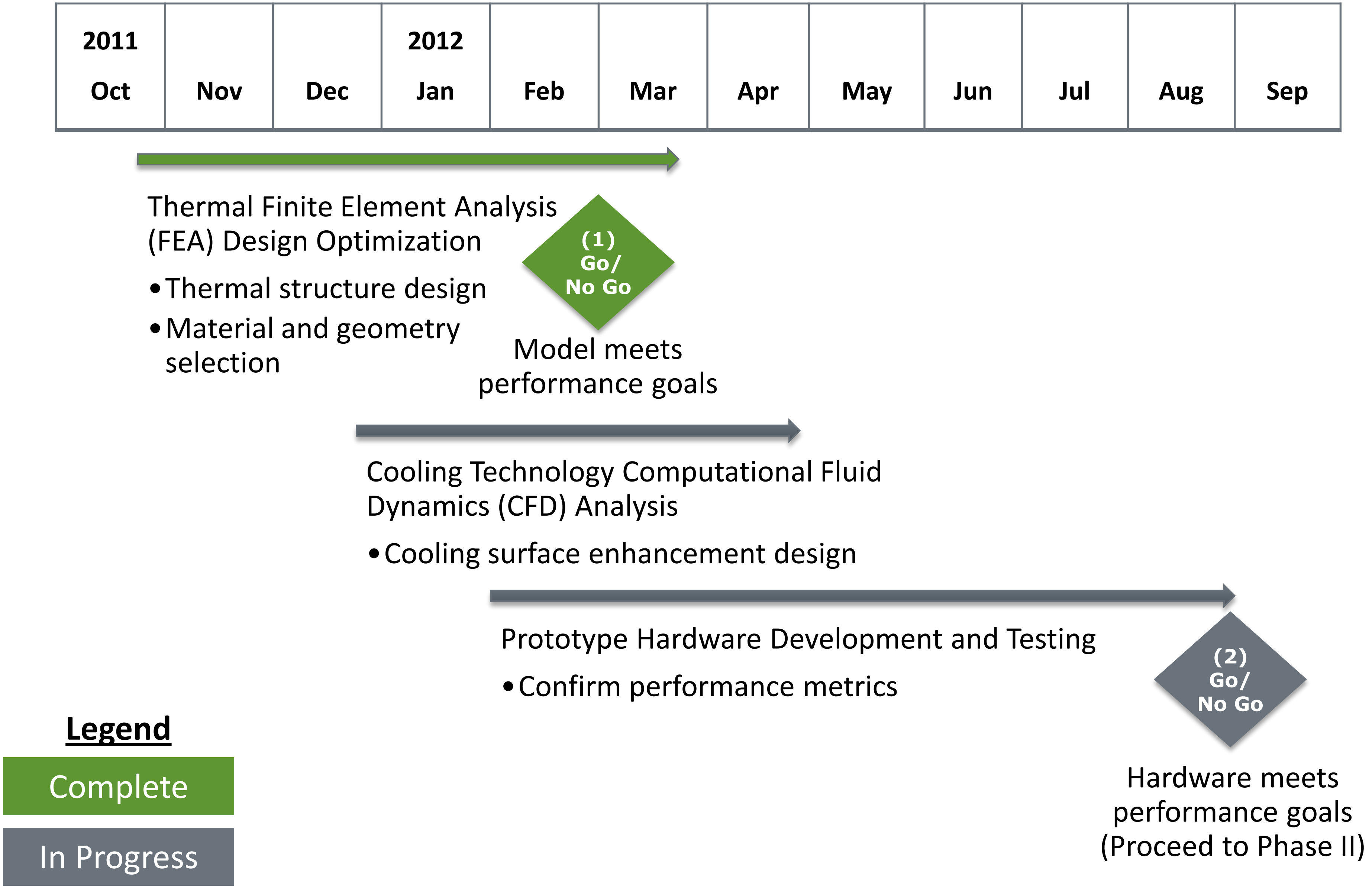
APEEM – Advanced Power Electronics and Electric Motors
IGBT – Insulated Gate Bipolar Transistor

Approach/Strategy

All Images - Credit: Kevin Bennion, NREL

Challenges	Strategy
Eliminate fixed custom-designed, cold plate heat exchangers	Integrate existing low-cost and scalable fabrication methods
Scale research and development prototype to address fabrication	Collaborate with industry partners
Integrating electronics package with cooling requires robust and low thermal resistance interfaces	Collaborate with current APEEM efforts in bonded interface material characterization
Support multiple power semiconductor packaging methods	Consider single/double-sided cooling and alternative interconnect methods

Approach/Strategy



2011 Oct	Nov	Dec	2012 Jan	Feb	Mar	Apr	May	Jun	Jul	Aug	Sep

Thermal Finite Element Analysis (FEA) Design Optimization

- Thermal structure design
- Material and geometry selection

Model meets performance goals

Cooling Technology Computational Fluid Dynamics (CFD) Analysis

- Cooling surface enhancement design

Prototype Hardware Development and Testing

- Confirm performance metrics

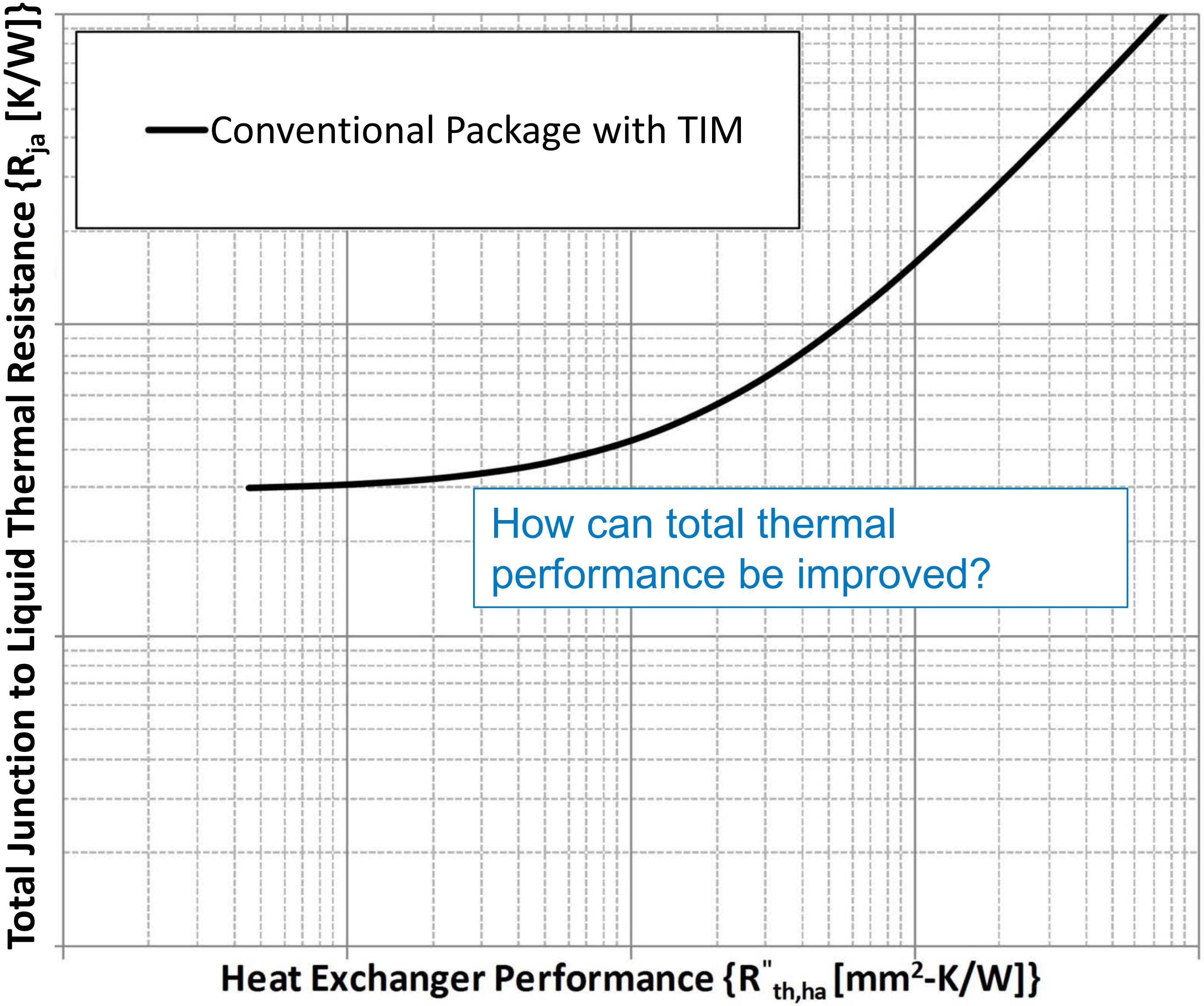
Hardware meets performance goals (Proceed to Phase II)

Legend

🟩 Complete

▨ In Progress

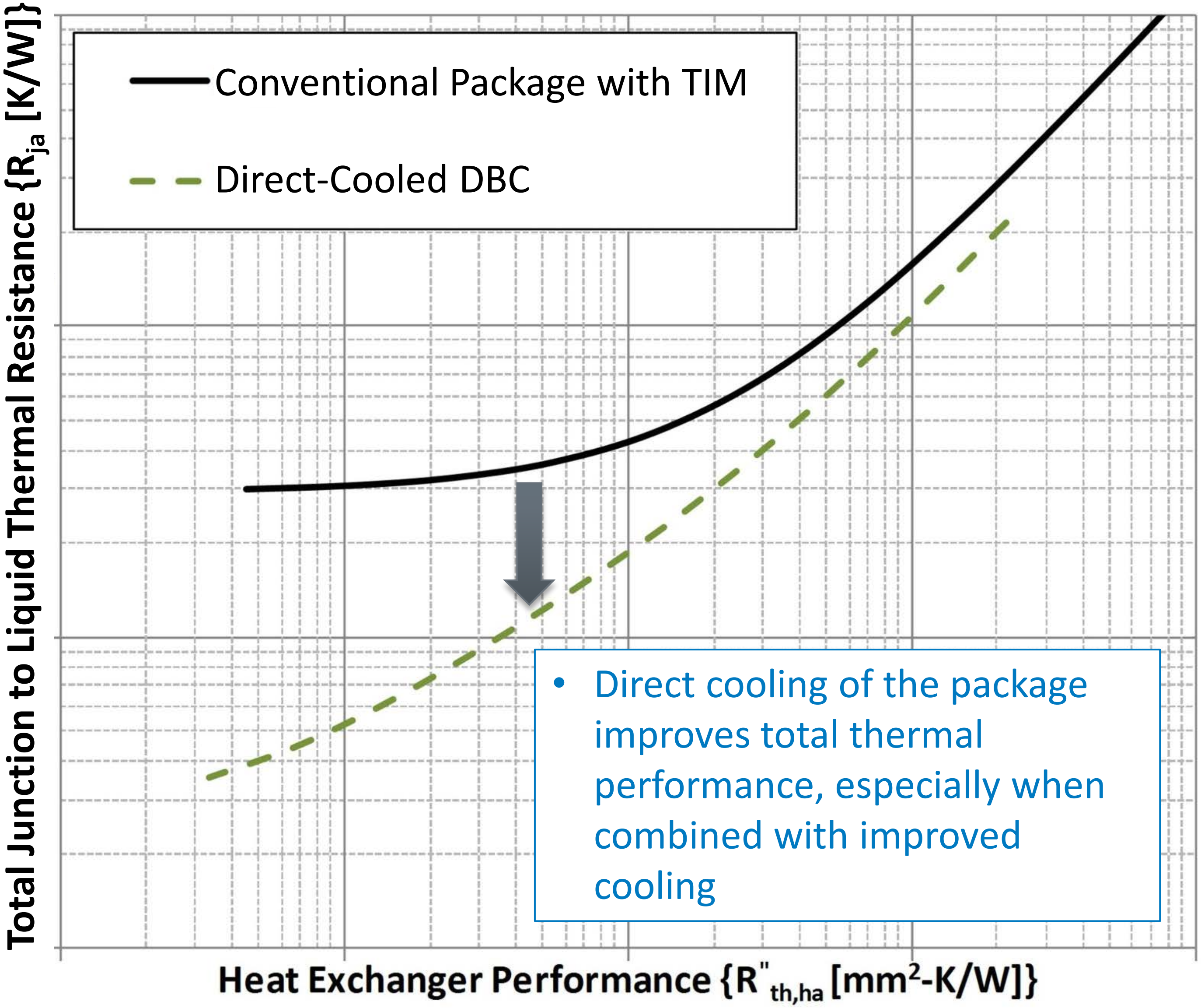
Approach/Strategy



How can total thermal performance be improved?

TIM: Thermal Interface Material

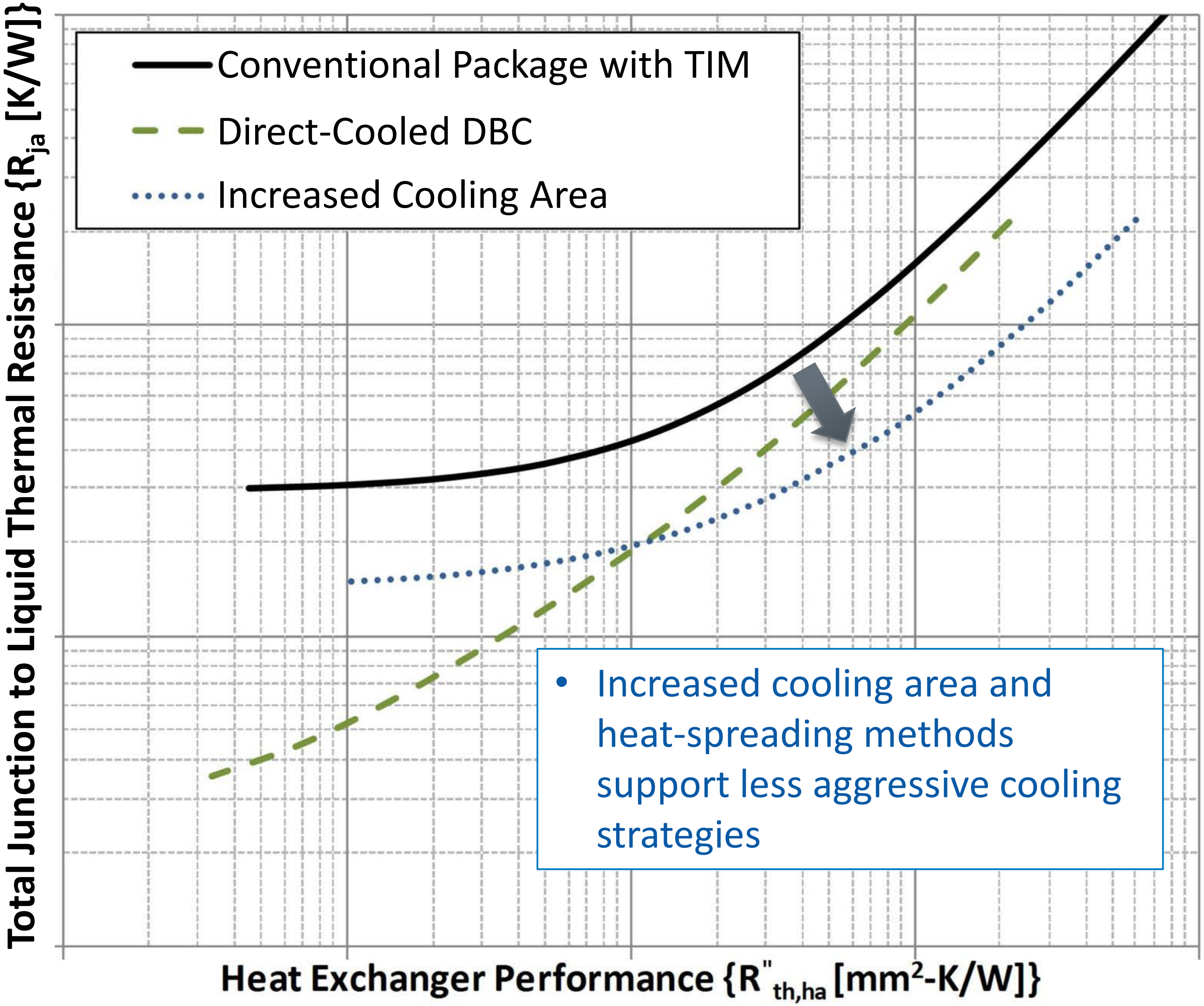
Approach/Strategy



- Direct cooling of the package improves total thermal performance, especially when combined with improved cooling

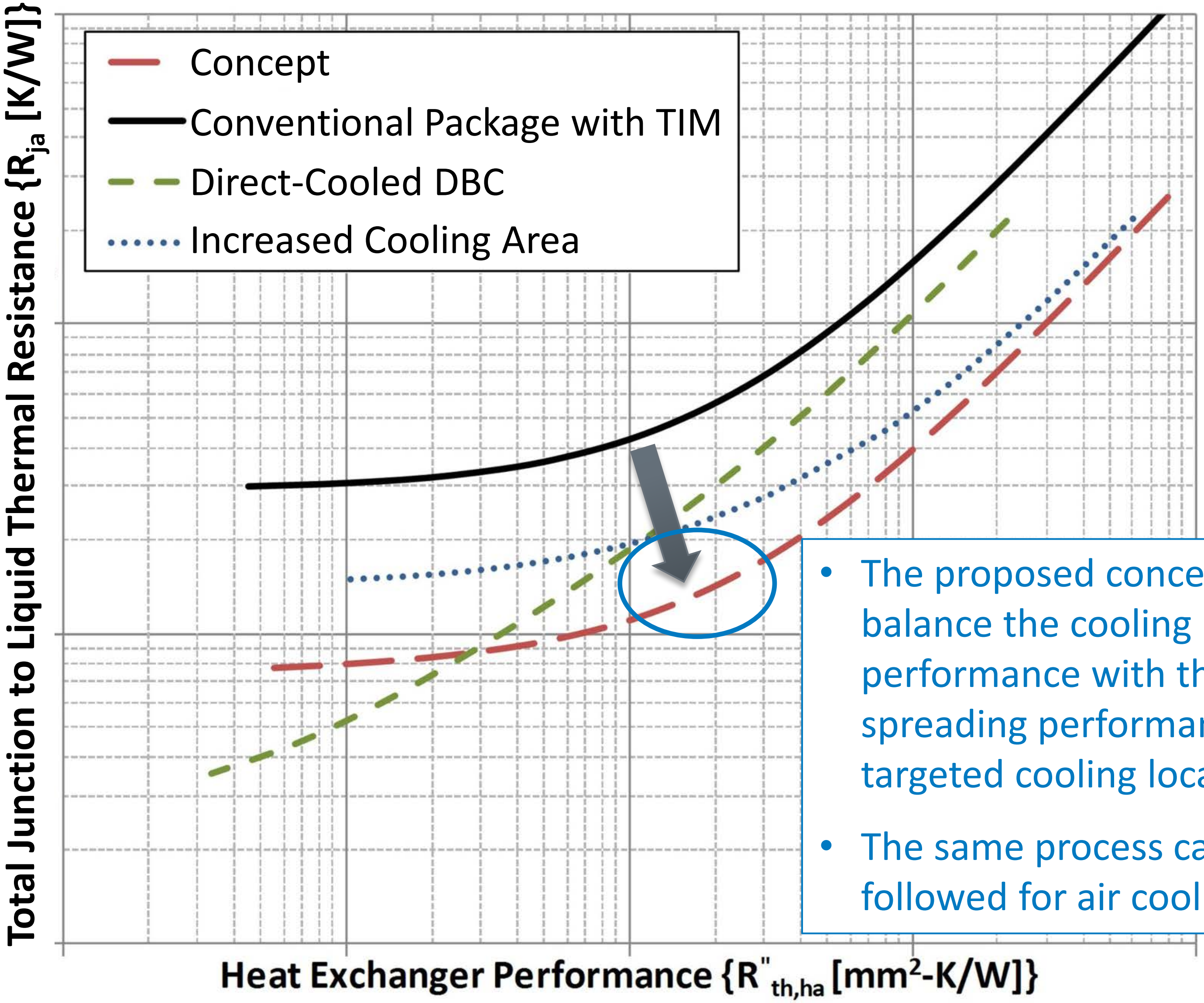
DBC: Direct Bond Copper

Approach/Strategy



- Increased cooling area and heat-spreading methods support less aggressive cooling strategies

Approach/Strategy



- The proposed concept seeks to balance the cooling performance with the heat spreading performance in the targeted cooling location
- The same process can be followed for air cooling

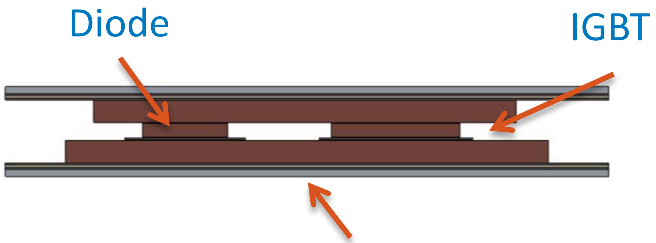
Technical Accomplishments and Progress

Selected baseline thermal stack configurations

Thermal Stack Comparisons

Baseline A

- 2008 Lexus LS 600H [1,2]

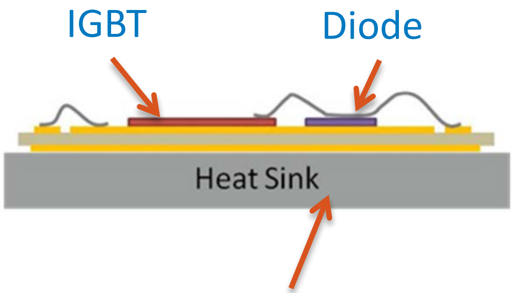


Baseline "A" Comparison Heat Exchanger Location
(cooled on each side)

Provides direct comparison to high performance commercial integrated package cooling design

Baseline B

- Direct-Cooled Baseplate



Baseline "B" Comparison Heat Exchanger Location
(single side shown)

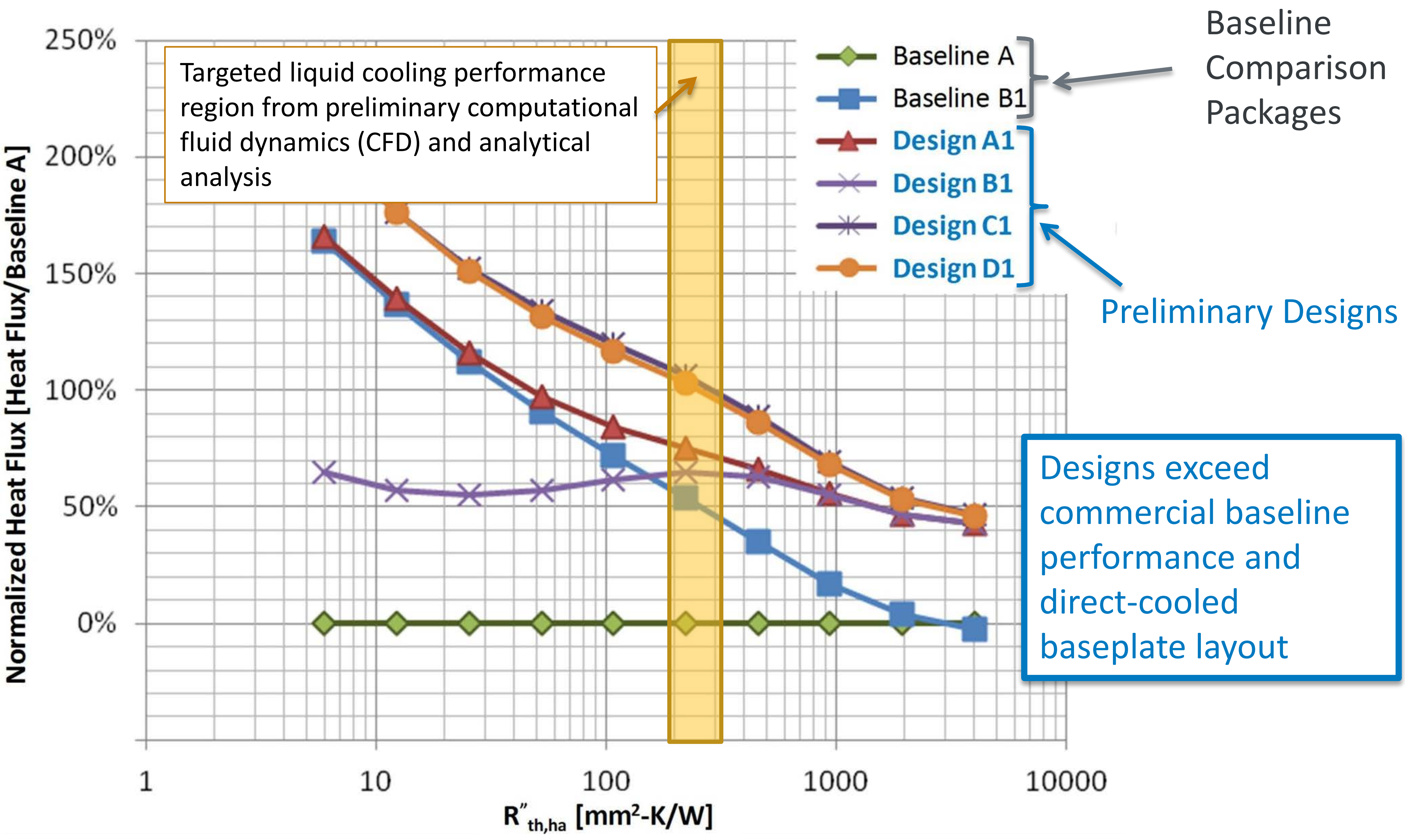
Provides direct comparison to low thermal resistance package stack.

[1] K. Bennion and K. Kelly, *Rapid Modeling of Power Electronics Thermal Management Technologies,* NREL Milestone Report, Jul. 2009.

[2] T. Burress, C. Coomer, S. Campbell, A. Wereszczak, J. Cunningham, L. Marlino, L. Seiber, and H.-T. Lin, *Evaluation of the 2008 Lexus LS 600H Hybrid Synergy Drive System.* Oak Ridge National Laboratory. ORNL/TM-2008/185, Jan. 2009.

Technical Accomplishments and Progress

Compared performance of alternative designs at targeted cooling performance region



Targeted liquid cooling performance region from preliminary computational fluid dynamics (CFD) and analytical analysis

Baseline Comparison Packages

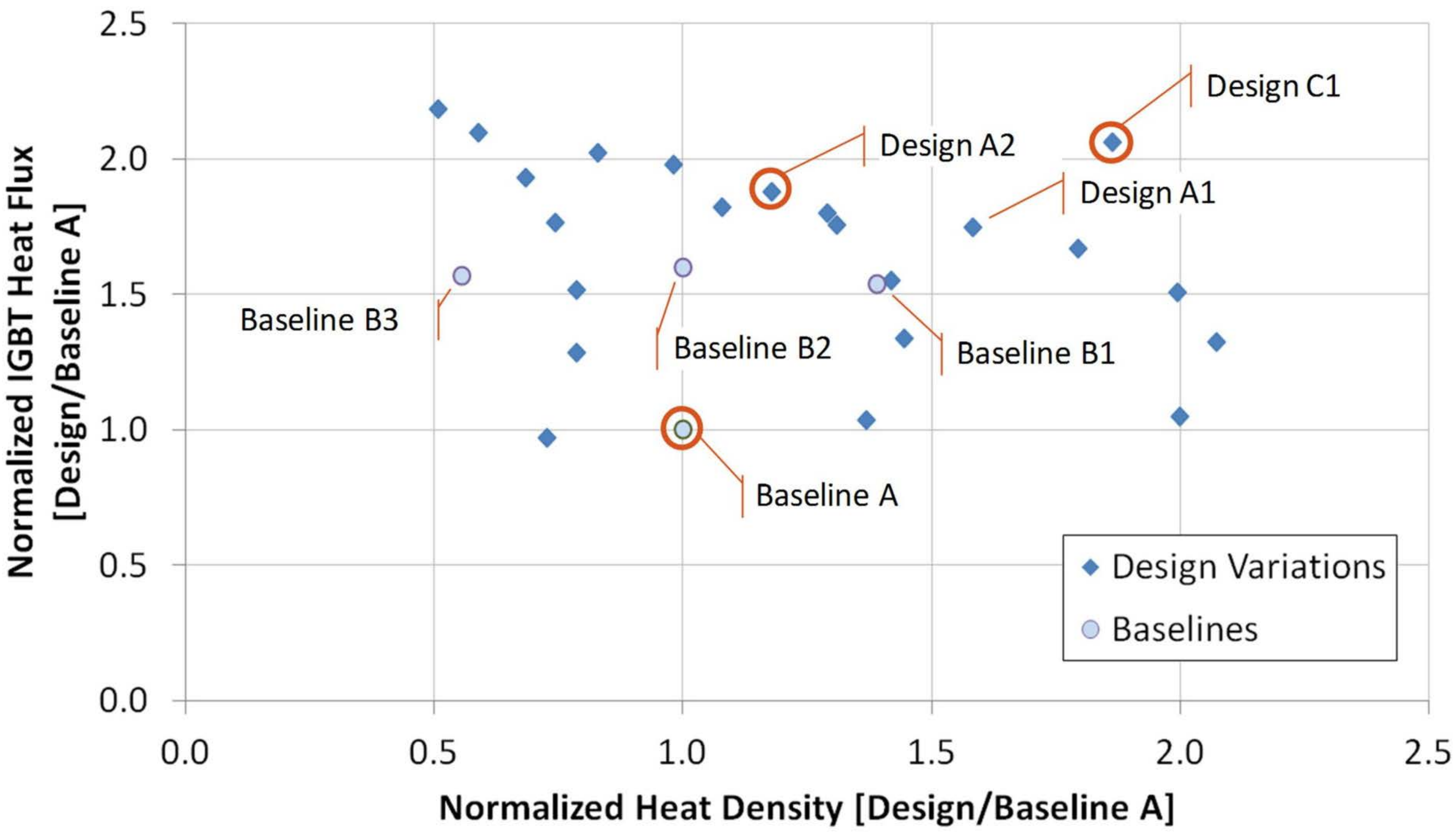
Preliminary Designs

Designs exceed commercial baseline performance and direct-cooled baseplate layout

Technical Accomplishments and Progress

Compared designs relative to baseline packages (heat density versus IGBT heat flux)

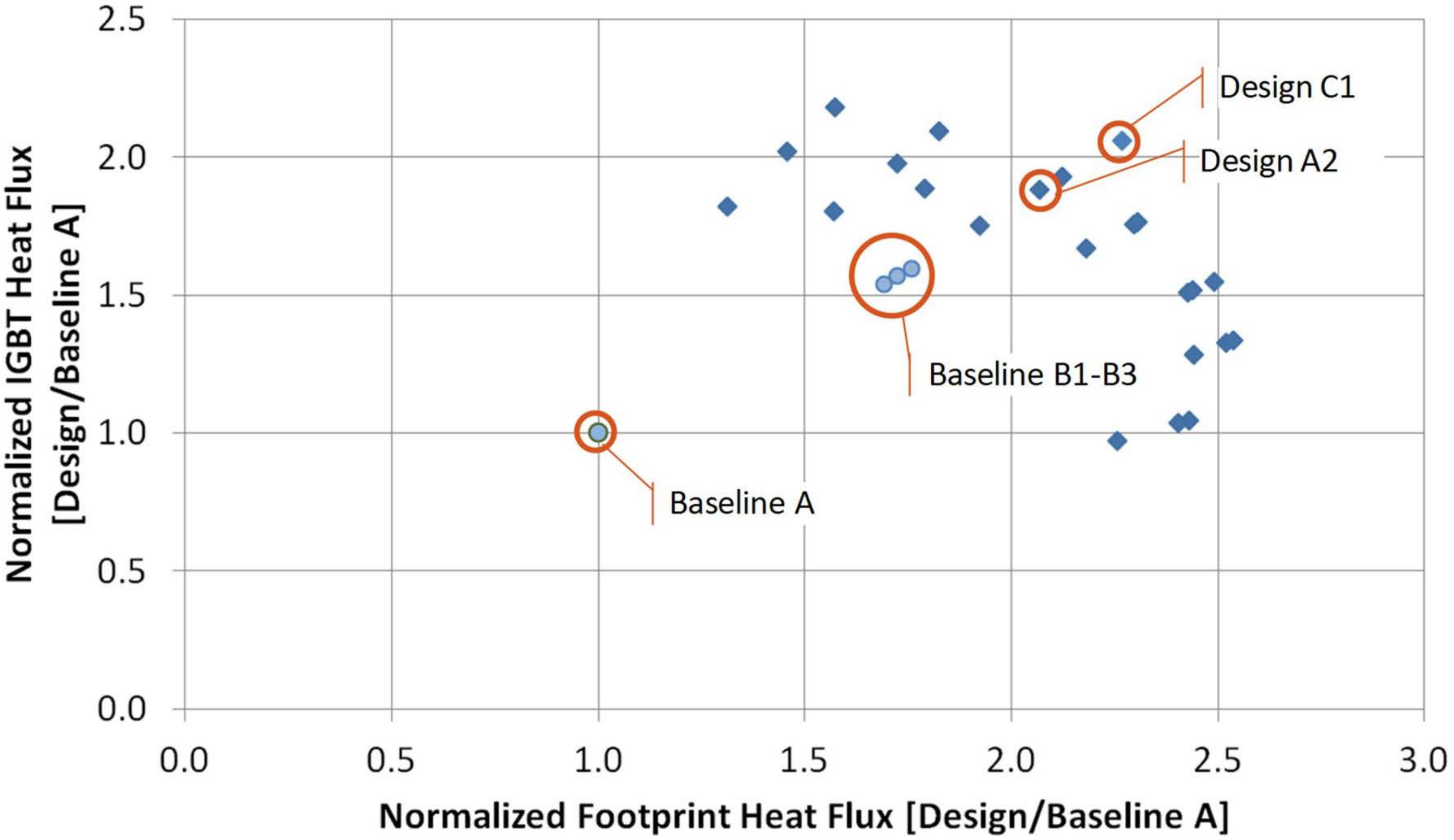
- Design C1 shows best performance but has cost concerns
- Design A2 shows good performance across design goals



Heat Density = Heat Rejection/Package Volume

Technical Accomplishments and Progress

Compared designs relative to baseline packages (footprint heat flux versus IGBT heat flux)

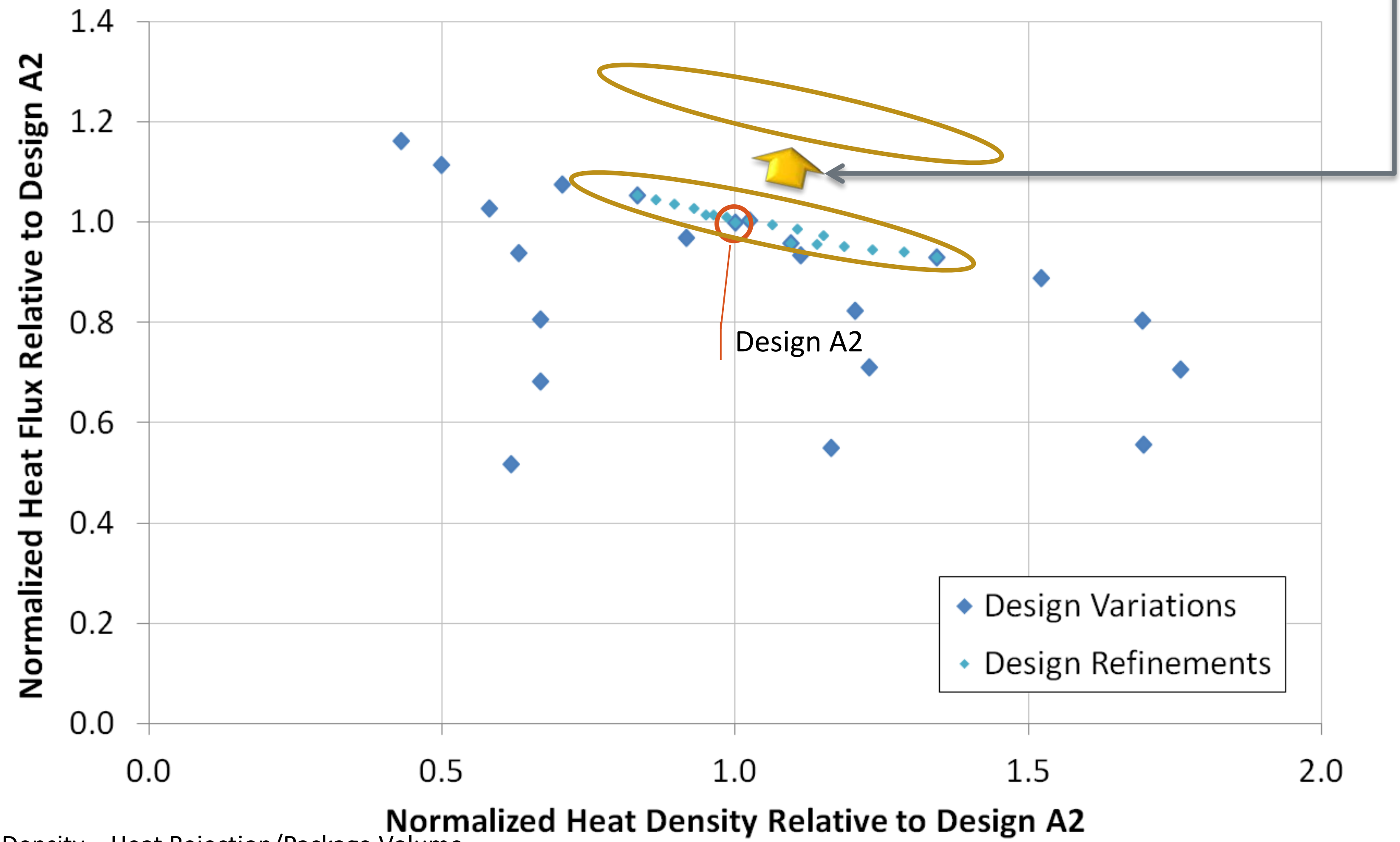


Footprint Heat Flux = Heat Rejection/Base Footprint Area

Technical Accomplishments and Progress

Performed parametric design study around the selected design point (Design A2)

- A significant jump to a better operating region was not found within the design constraints
- Proceeding with Design A2

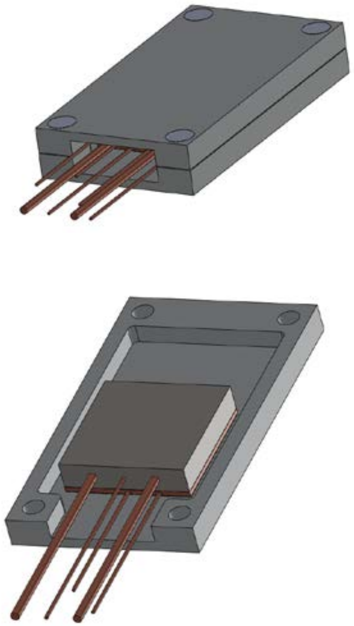


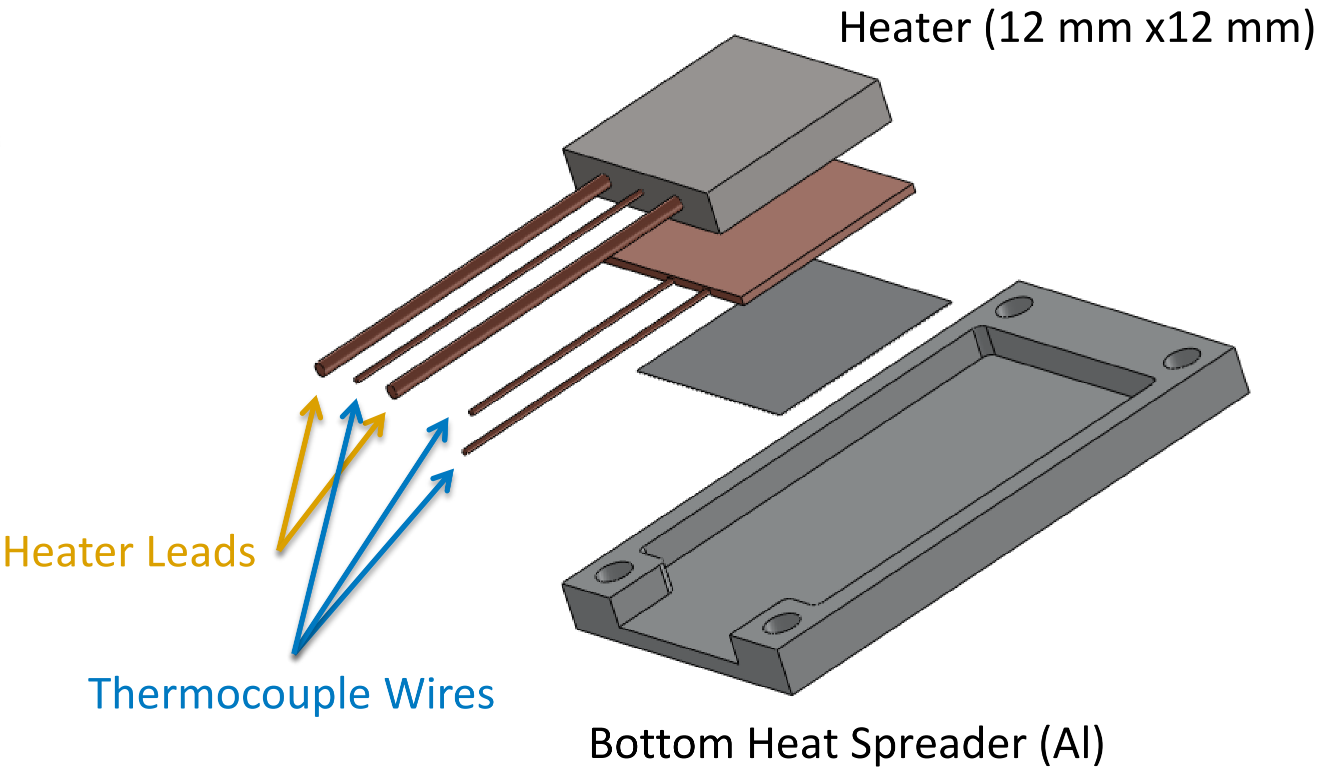
Heat Density = Heat Rejection/Package Volume

Technical Accomplishments and Progress

Developing heater package to represent power semiconductor package for prototype testing

- Capable of single- or double-sided cooling
- Enables validation of thermal model
- Represents generic power semiconductor package





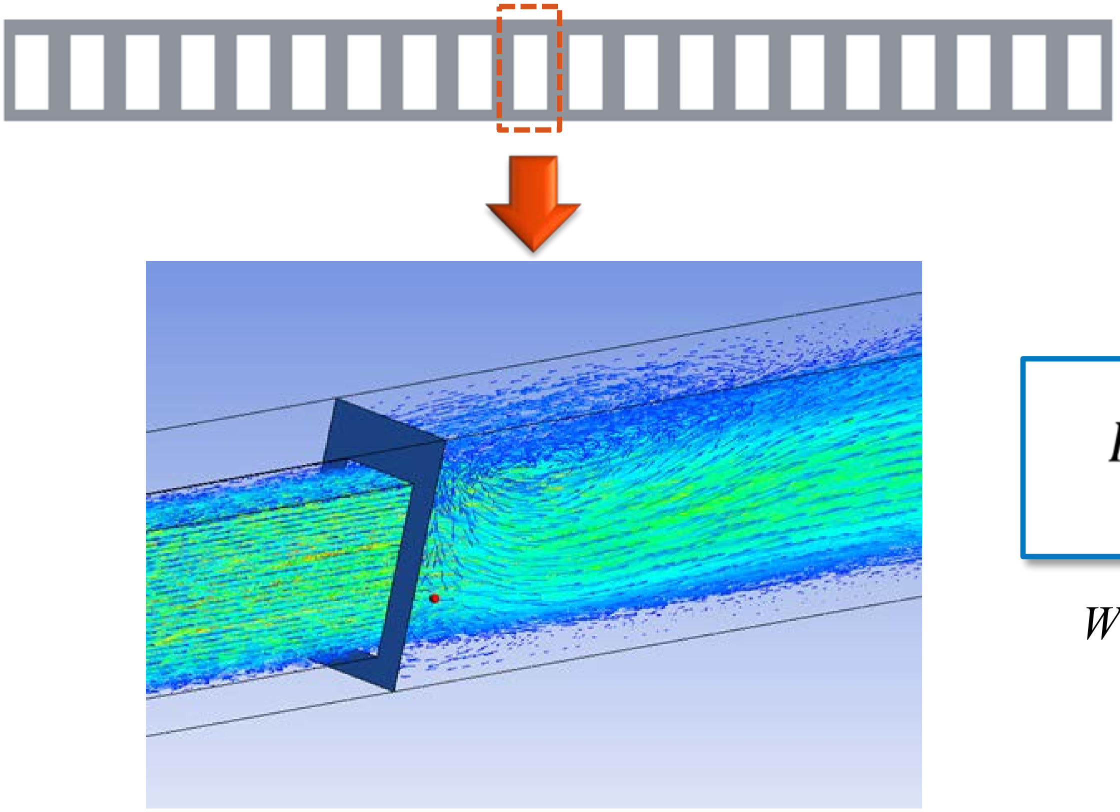
Note:

- Preliminary design
- Additional thermocouples will be placed on the heat spreader plate, which is not shown.

Technical Accomplishments and Progress

Developing CFD model for heat transfer design

- Provided preliminary estimate for heat exchanger cooling performance
- Compared against analytical methods
- Focusing initially on channel flow
- Moving towards more complex, full-system CFD for additional design studies and fin design



h

UA

$$\boxed{R_{NTU} = \frac{1}{\varepsilon \dot{m} c_p} \quad or\ \boldsymbol{R_{th,ha}}}$$

Where: $\varepsilon = f(NTU)$

or

$\varepsilon = f(UA, \dot{m}, c_p)$

Collaboration and Coordination

Other Government Laboratories

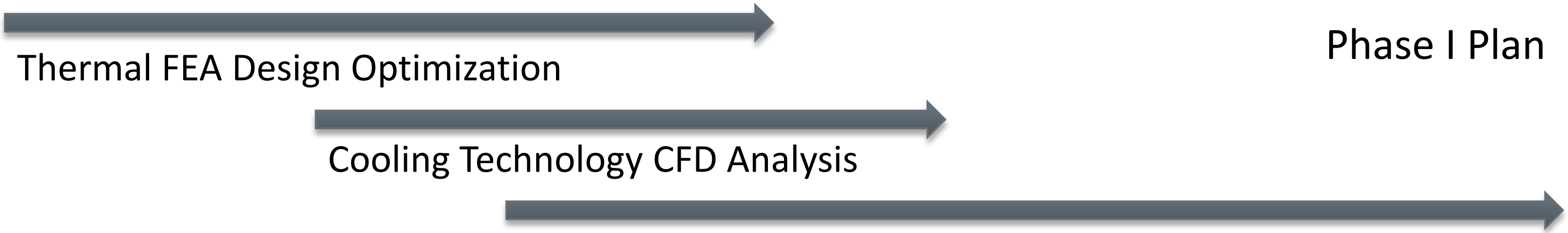
Oak Ridge National Laboratory/APEEM Program

- Support from benchmarking activities
- Ensure thermal design space is appropriate and modeling assumptions are consistent with other aspects of APEEM research

Industry

Heat Exchanger Collaboration Partner (Sapa)

Power Semiconductor Packaging Partner for Phase II



Phase I Plan

Thermal FEA Design Optimization

Cooling Technology CFD Analysis

Prototype Hardware Development and Testing

Proposed Future Work

FY12 (Phase I)

- **Software Prototype Design**
  - Refine prototype heat exchanger design through full-system CFD thermal and fluid analysis

- **Hardware Prototype Testing**
  - Build prototype of heat exchanger module with heat sources representing power electronics package
  - Compare experimental results against model results
    - **Go/No-Go**: If prototype heat exchanger hardware matches design expectation, proceed to second project phase to refine design and integrate with a power electronics package.

Proposed Future Work

If FY12 simulation and test results achieve design targets, the plan is to proceed to the second project phase in FY13

- **FY13 (Phase II)**
  - Incorporate lessons learned from Phase I prototype build to refine design to improve performance and fabrication
  - Identify partner for power electronics package
  - Design and build second prototype heat exchanger module integrated with power electronics package
  - Complete testing of integrated heat exchanger module
  - Explore opportunity for application to air cooling

Summary

Relevance

- Increased heat dissipation is necessary to reduce power semiconductor cost, weight, and volume
- Integration of the power electronics package thermal design and the cooling design can improve power semiconductor performance
- A modular and scalable thermal approach can reduce the need for custom heat exchanger redesigns as applications scale in power

Approach/Strategy

- Optimize integrated thermal package design and cooling technology for the targeted cooling performance
- Reduce cost by increasing semiconductor heat flux
- Reduce cost by enabling less aggressive and lower cost cooling methods
- Maintain best-in-class power density while doubling semiconductor heat flux
- Enable compatibility to alternative power semiconductor packaging technologies

Summary

Technical Accomplishments

- Selected and analyzed baseline thermal stack configurations for performance benchmarking
- Compared performance of alternative designs at targeted cooling performance region against selected baseline configurations
- Performed parametric design study around the selected design point and selected preliminary design for hardware prototype testing
- Developing heater package to represent power semiconductor package for prototype testing
- Developing CFD model for heat transfer design

Collaborations

- Established collaboration with heat exchanger development partner (Sapa)
- Future work will look to incorporate power semiconductor partner as project transitions to Phase II

Acknowledgments:

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