annual progress report

2009

ANNUAL PROGRESS REPORT FOR ADVANCED POWER ELECTRONICS

EPARTMENT OF ENERGY | Energy Ef i iency & Renewable Energy

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Annual Progress Report for Advanced Power Electronics

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Acronyms and Abbreviations

3D	three-dimensional
3G	third generation
Al_2O_3	aluminum oxide or alumina
ac	alternating current
Alnico	aluminum-nickel-cobalt (alloy used to make permanent magnets)
APEEM	Advanced Power Electronics and Electric Machines
APF	active power filter
BGR	bandgap voltage reference
CMOS	complementary metal-oxide semiconductor
CSI	current source inverter
DBC	direct bonded copper
dc	direct current
DMOS	double diffused metal-oxide semiconductor
DOE	U.S. Department of Energy
DSP	digital signal processing
ECVT	electronically controlled continuously variable transmission
EDS	energy dispersive x-ray spectroscopy
EETT	Electrical and Electronics Technical Team
EMF	electromotive force
EMI	electromagnetic interference
EOL	end-of-life
ETA	Electric Transportation Applications
EV	electric vehicle
FEA	finite element analysis
f_m	modulation frequency (inverter)
f_{sw}	switching frequency (inverter)
HEV	hybrid electric vehicle
HSF	hard switch fault
HVNMOS	high voltage NMOS
ID	inner diameter
IGBT	insulated gate bipolar transistor
IM	induction motor
IMFP	isolated multiple flux path
INL	Idaho National Laboratory
INV/CONV	inverter/converter
IPM	internal permanent magnet
JBS	junction barrier Schottky (device/diode)

JFET	junction field-effect transistor
Ld	direct axis inductance (IPM motor)
Lq	quadrature axis inductance (IPM motor)
LCR	inductance, capacitance, resistance (as in an LCR meter, used to measure impedance)
MG	motor/generator
MOSFET	metal-oxide semiconductor field-effect transistor
NMOS	n-channel metal-oxide semiconductor
OD	outer diameter
ORNL	Oak Ridge National Laboratory
OTA	operational transconductance amplifier
PCU	power control unit
PE	power electronic
pF	power factor
PHEV	plug-in hybrid electric vehicle
PI	proportional-integral
PM	permanent magnet
PMOS	p-channel metal-oxide semiconductor
p-p	peak-to-peak
PSIM	Powersim (circuit simulation software)
PWM	pulse-width modulation
R24	conceptual design revision 24 (for the Novel Flux Coupling Machine without PMs)
RMS	root mean square
SiC	silicon carbide
SPICE	Simulation Program with Integrated Circuit Emphasis
SOI	silicon-on-insulator
SR	switched reluctance
SRM	switched reluctance motor
UVLO	undervoltage lockout
Vdc	dc voltage
Vgs	gate-source voltage
VSATT	Vehicle Systems Analysis Technical Team
VSI	voltage source inverter
WBG	wide bandgap
WEG	water-ethylene glycol
ZTC	zero-temperature coefficient

1. Introduction

The U.S. Department of Energy (DOE) and the U.S. Council for Automotive Research (composed of automakers Ford, General Motors, and Chrysler) announced in January 2002 a new cooperative research effort. Known as FreedomCAR (derived from "Freedom" and "Cooperative Automotive Research"), it represents DOE's commitment to developing public/private partnerships to fund high-risk, high-payoff research into advanced automotive technologies. Efficient fuel cell technology, which uses hydrogen to power automobiles without air pollution, is a very promising pathway to achieve the ultimate vision. The new partnership replaces and builds upon the Partnership for a New Generation of Vehicles initiative that ran from 1993 through 2001.

The Advanced Power Electronics and Electric Machines (APEEM) subprogram within the Vehicle Technologies Program provides support and guidance for many cutting-edge automotive technologies now under development. Research is focused on understanding and improving the way the various new components of tomorrow's automobiles will function as a unified system to improve fuel efficiency.

In supporting the development of advanced vehicle propulsion systems, the APEEM effort has enabled the development of technologies that will significantly improve efficiency, costs, and fuel economy.

The APEEM subprogram supports the efforts of the FreedomCAR and Fuel Partnership through a three-phase approach intended to

- identify overall propulsion and vehicle-related needs by analyzing programmatic goals and reviewing industry's recommendations and requirements and then develop the appropriate technical targets for systems, subsystems, and component research and development activities;
- develop and validate individual subsystems and components, including electric motors and power electronics; and
- determine how well the components and subsystems work together in a vehicle environment or as a complete propulsion system and whether the efficiency and performance targets at the vehicle level have been achieved.

The research performed under this subprogram will help remove technical and cost barriers to enable the development of technology for use in such advanced vehicles as hybrid electric vehicles (HEVs), plug-in HEVs (PHEVs), all electric vehicles, and fuel-cell–powered automobiles that meet the goals of the Vehicle Technologies Program.

A key element in making these advanced vehicles practical is providing an affordable electric traction drive system. This will require attaining weight, volume, and cost targets for the power electronics and electrical machines subsystems of the traction drive system. Areas of development include these:

- novel traction motor designs that result in increased power density and lower cost;
- inverter technologies involving new topologies to achieve higher efficiency, with the ability to accommodate higher-temperature environments while achieving high reliability;
- converter concepts that employ means of reducing the component count and integrating functionality to decrease size, weight, and cost;
- new onboard battery charging concepts that result in decreased cost and size;
- more effective thermal control and packaging technologies; and
- integrated motor/inverter concepts.

ORNL's Power Electronics and Electric Machinery Research Center conducts fundamental research, evaluates hardware, and assists in the technical direction of the DOE Vehicle Technologies Program, APEEM subprogram.

The thermal management of electronics and electronic systems represents a major technical barrier to achieving specific Advanced Power Electronics and Electric Machine (APEEM) technical targets. Excessive heat can degrade the performance, life, and reliability of power electronic components. Advanced thermal management technologies can enable higher power densities and lower system cost. Additionally, increased heat dissipation may enable lower cost package configurations and lower cost materials.

The Advanced Thermal Management for Vehicle Power Electronics and Electric Machines research activity is focused on developing thermal management technologies that enable advanced power electronics and electric machine technologies that are efficient, small, light, low cost, and reliable. Specifically, we are concerned with addressing and overcoming any and all thermal barriers to these systems within the systems context of the entire vehicle—ultimately working towards a total vehicle thermal system that is low-cost, small, light, reliable, effective, and efficient.

We work closely with industry and research partners in developing candidate thermal management technologies to meet the program goals. The thermal management research is organized into three distinct focus areas including:

- Thermal System Integration
- Heat Transfer Technologies
- Thermal Stress and Reliability

Additionally, there are close ties to the Power Electronics packaging focus area. The power electronics package including the device layout, material selection, and topology define the package thermal resistance and required heat flux levels and the induced thermal stresses. Conversely, aggressive heat transfer performance may enable higher power densities and novel package designs.

2. Thermal Management Systems

2.1 Direct Cooled Power Electronics Substrate

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Objectives

The FY 2009 project objective was to finalize the design requirements for the selected architecture for a direct cooled power electronics substrate which will result in reductions in size and volume of the inverter power electronics, achieving the 2015 DOE FreedomCAR target of at least 12.0 kW/L while operating with an elevated coolant temperature of 105°C.

Proposed Solution

To use 105°C coolant for heat dissipation from the electronics, the coolant paths must be placed as close to the chip junction as possible. This project explores a direct cooled power electronics substrate which incorporates cooling channels directly in the ceramic of a direct bonded copper (DBC) substrate. The overall structure of the direct cooled substrate is a hexagonal and/or an octagonal prism. This shape simplifies the fluid seals and provides a unique structure for die attachment. The approach presented also highlights the benefits of designing the power electronics package and inverter package in parallel.

Approach

- Finalize the design requirements for a single leg prototype power electronics mounting structure DBC substrate.
- Perform a final thermal simulation as well as a mechanical stress simulation on the selected design structures and use the finite element analysis (FEA) results as a basis for comparison of FY 2009 test results.
- Complete the assembly of the single leg prototype direct cooled DBC designs as follows.
  - — Manufacture the selected ceramic substrate designs.
  - — Design, purchase components, and fabricate the testing apparatus.
  - — Finalize the substrate fabrication (copper cladding and plating).
  - — Assemble components onto the substrate (diode attachment and wire/ribbon bonds).
- Test the assembled prototypes.
  - — Instrument and install assembled prototypes in the testing apparatus.
  - — Test assembled prototypes using 105°C water-ethylene glycol (WEG) coolant.

Major Accomplishments

- Designs were selected.
- Thermal and mechanical FEA results were obtained.
- DBC substrates were fabricated (copper clad, plated, and dies attached with ribbon bonds applied).
- Flow tests were completed.
- FEA models were updated and comparisons made based on experimental flow results.
- Prototypes were assembled, instrumented, and tested using various WEG temperatures, including 105°C.
- Model validations were performed based on comparisons between experimental results and modeling results.

Future Direction

- Iterate mechanical design based on FY 2009 laboratory test results.
- Fabricate and assemble the next generation inverter prototype.
- Finalize inverter prototype design and testing.

Technical Discussion

The goal of the Direct Cooled Power Electronics Substrate project is to enable the use of 105°C coolant with the power electronic components used in hybrid electric and plug-in hybrid electric vehicles (HEVs and PHEVs). The proposed concept in this project was to develop an innovative power electronics mounting structure, generate three-dimensional models, and perform both thermal and mechanical FEA. This concept involved integrating cooling channels within the DBC substrate and strategically locating these channels underneath the power electronic devices. Reducing the size and weight of the heat sink for power electronics are among the other benefits sought.

Of the design concepts modeled, two of the most promising designs were fabricated, assembled, and tested. These designs took into account issues such as containment of the fluid (separation from the electronics) and synergy with the whole power inverter design architecture. Testing results were compared to the final FEA modeling performed on the two designs to validate both the modeling results and the success of the design approach.

Information contained in this annual report serves as a general discussion of this research effort. For more detailed information, please refer to *Preliminary Testing Results of Direct Cooled Power Electronics Substrate,* ORNL/TM-2009/204 [1].

Recap of FY 2008 Work

In FY 2008, the research effort showed that a ceramic heat exchanger concept involving 105°C WEG cooling was a viable option. Several design iterations including FEA results for each design were performed. A performance matrix and weighting system was developed to help evaluate the effectiveness of each design. These design matrix summaries are listed in *Direct Cooled Power Electronics Substrate,* ORNL/TM-2008/112, Tables 7–13 [2]. They contain the loads, thermal data resulting from the use of three or four insulated gate bipolar transistors (IGBTs), manufacturing variables and trade-offs, and cost to manufacture in quantities of 100,000 pieces.

Based on cost evaluations, research was geared primarily toward alumina (Al_2O_3) as the substrate material. The overall size of the structure grew to accommodate more heat spreading, which is required because of Al_2O_3's lower thermal conductivity compared with other candidate ceramic materials. Knowing that Al_2O_3 was inert to WEG, compatibility tests were completed to demonstrate the effect of

50/50 WEG on other candidate ceramics. The annular substrate and the four-hole substrate were two of the most promising design iterations. These were selected for the second phase of the research effort.

Selection of Final Single Leg Prototype Designs

Detailed models of the annular substrate and the four-hole substrate were run. These models include more geometry detail such as rounded ends, wire bonds, actual chip sizes, and distributed loading. The original models from FY 2008 had a copper cladding thickness of 0.050 in. (1.27 mm). The first quote from a vendor was to clad the substrate with 0.020 in. (0.5 mm) copper. After some debate, a few models were run to compare cladding thickness differences. The thinner cladding increases the junction temperature of the chip by 5ºC. Thus the copper cladding should be as thick as possible. One vendor was able to provide a quote for 0.050 in. thick cladding; therefore this thickness was used for the thermal models.

Because the flow properties of the thermal enhancing metal matrix were unknown at this time, three separate approaches to model the porous media flows were run for each design case to establish an operational range.

The Darcy model, which assumed a plug flow or flat velocity profile, was used in FY 2008. The Darcy flow model resulted in the lowest temperature predictions because of the large velocity gradient at the wall. The parameters used for the porous media model were taken from the literature for comparable applications [3]. The permeability for aluminum foams with similar specifications is on the order of 1e-8 m^2. This permeability provides a high flow restriction that increases the difficulty of obtaining a converged solution. For a basic comparison and simpler computational scheme the permeability was 1e-4 m^2, and the porosity was 0.89. The Darcy model forms the lower bound of the operational range.

The Brinkman porous media flow model takes into account the viscous effects at the inner wall of the flow channel, which results in a more parabolic velocity profile. The decrease in velocity gradient at the channel wall results in less heat transfer to the fluid. This model is only valid for laminar flows. The flow parameters were consistent with the Darcy model. In general, the Brinkman model produces the highest junction and fluid temperatures. It forms the upper bound of the operational range.

However, the Brinkman model does not account for the turbulent mixing within the metal foam inserted in the flow channels. A Brinkman model with a Forchheimer correction flattens the velocity profile. The flatter profile increases the velocity gradient near the wall, which causes more local heat transfer. This effect lowers the maximum temperatures compared with the Brinkman model but not to the point of equaling the Darcy model. The Brinkman model with the Forchheimer correction is believed to be more accurate because it accounts for the added flow resistance resulting from turbulence. The Forchheimer friction coefficient was calculated from a correlation in the literature [4].

Annular Design

The results for the three cases are shown in Table 1. The highest predicted temperature is above the desired 150°C but still below the absolute maximum of 175°C. As predicted, the Darcy model forms the lower bound, and the Brinkman model forms the upper bound. All diode temperatures are below the 150°C design point. The Brinkman model also shows the fluid wall temperature exceeding the boiling point of the 50/50 WEG, but the other two models are below the 130°C limit. These results show that the operational range of the direct cooled annular substrate is reasonable with respect to the design parameters and the material property assumptions.

Table 1. Thermal Modeling Results for Annular Design

Maximum temperatures	Darcy	Brinkman	Brinkman with Forchheimer correction
T_{IGBT} (ºC)	149.9	156.6	154.8
T_{diode} (ºC)	143.5	149.7	148.1
T_{fluid} (ºC)	123.1	131	128.8

Four-Hole Design

The results of the three flow cases for the four-hole design are shown in Table 2. The Darcy model resulted in a maximum fluid wall temperature close to the maximum allowable temperature. Modeling the Brinkman and Forchheimer correction confirmed the fluid temperature would exceed the boiling point.

The other flow models result in increases in the predicted junction temperatures. The chips can theoretically survive at these temperatures, but their reliability may be compromised. Because the nonconservative models predict temperatures above boiling, the actual junction temperatures may be lower because of phase change effects. On the other hand they may be higher because of local hot spots and bubble formation. The model does not account for the latent energy exchange at boiling and thus cannot accurately prescribe junction temperatures if the boiling point is exceeded. The operational range for the four-hole design extends beyond the design limits but may be improved with further work on hole size and placement.

Table 2. Thermal Modeling Results for Four-Hole Design

Maximum temperatures	Darcy	Brinkman	Brinkman with Forchheimer correction
T_{IGBT} (ºC)	150.8	160.0	156.0
T_{diode} (ºC)	152.9	160.4	156.9
T_{fluid} (ºC)	127.7	139.7	134.3

From the modeling with all properties determined by engineering estimates, the annular structure should perform better than the four-hole design. Flow properties and thermal validation experimentation were used to evaluate the accuracy of the model parameters.

Mechanical FEA Results

The two designs were also evaluated through a statistical mechanics program intended to determine the probability of failure for ceramic components. The four-hole design had a probability of failure of 4 ppm. The annular design had a probability of failure of 8 ppm. These evaluations were based on the thermal fatigue from the temperature distribution found at the end of FY 2008. The survivability of both parts is well within an acceptable range.

Experimental Flow Test Results

In previous modeling, the aluminum foam was modeled using several governing equations for porous media. This modeling was used to provide a range of temperatures for the ceramic substrate and electronics because the exact properties of the foam were unknown at the time.

Upon receipt of the aluminum foam, the porosity was measured. The annular pieces had an average porosity of 0.90, and the cylinders for the four-hole design had an average porosity of 0.91. These values reflect a maximum of a 2% increase over the assumed value of 0.89 in previous modeling.

Flow tests were conducted to measure pressure drop across the metal foam as a function of average inlet velocity. A schematic of the component test experiment is shown in Fig. 1. A schematic of the test fixture for pressure drop measurements is presented in Fig. 2. A Bay Voltex unit (a custom commercial heater/chiller), circulates the 50/50 WEG. This unit is capable of regulating the temperature of the working fluid (in this case WEG) from 0ºC to 110ºC and providing flow from 0.25 to 2.5 gpm at various discharge pressures. An auxiliary heater was installed on the Bay Voltex unit to assist the internal heating element when running at elevated temperatures.

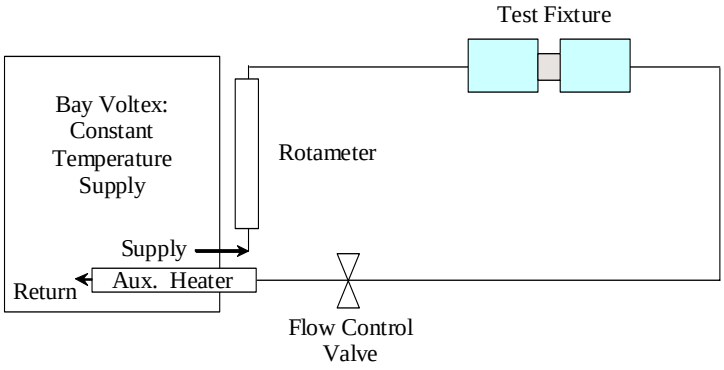

Fig. 1. Schematic of component test experiment.

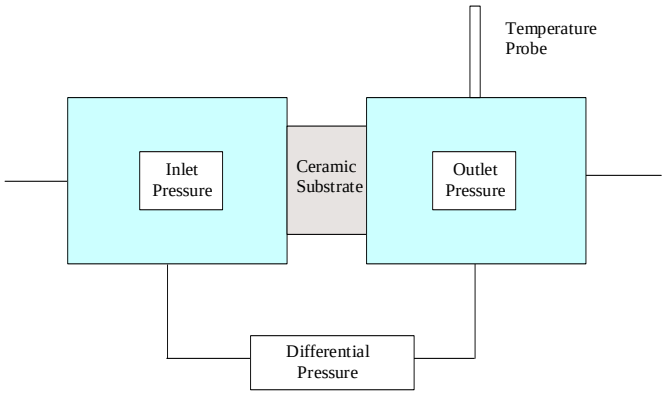

Fig. 2. Schematic of test fixture for pressure drop measurements.

The pressure drop was recorded for both designs at 25°C and 100°C. After reducing the data, the results generally formed a quadratic relation. The Darcy-Forchheimer model was used to derive permeability and a Forchheimer friction coefficient from the data. For the annular foam structure the permeability was 9.46e-8 m^2, and the Forchheimer friction coefficient was 0.072. For the four-hole foam structure the permeability was 6.54e-8 m^2, and the Forchheimer friction coefficient was 0.056. These flow variables differ greatly from those used in the thermal modeling. The permeability was more in-line with that reported in the literature. The Forchheimer coefficients are smaller than that predicted by the correlation but are within values reported in the literature. A different solution scheme was found to obtain converged models with smaller permeabilities, and the thermal models were updated to reflect the change in flow parameters. In general, the chip temperatures decreased because the lower permeability restricts flow. The flow restriction flattens the flow profile and pushes it closer to a plug type/Darcy flow.

Further discussion of these results and the experimental setup is in the *Preliminary Testing Results of Direct Cooled Power Electronics Substrate,* ORNL/TM-2009/204 [1].

Prototype Manufacturing and Assembly

The ceramic substrate geometries fabricated by CoorsTek were received with reasonably flat surfaces and within the design specifications. The substrates were fabricated using an injection molding process to produce the "green" parts and were then fired to complete the final product. Upon inspection of the flat surfaces, the total surface flatness on the parts was within 0.001 in. to 0.002 in. The flat surfaces are necessary for the die attachment, especially if the dies are to be sintered into position.

Finalize Substrate Fabrication (Copper Cladding and Plating)

Once the substrates were received from CoorsTek, the next process was to have each of the flat surfaces metalized with copper. The copper has to be intimately bonded to the ceramic to promote heat transfer. Aegis Technology, Inc., of Santa Ana, California, was contracted to complete this task. Before the parts were returned, the copper was nickel-gold plated to help with the chip soldering/sintering. The gold plating and presumably the nickel plating wrapped the edges onto the sealing boss. A test was performed using a mega-ohm testing unit to determine that the two landing areas (the 12 mm wide flat for diode attachment and the 5 mm flat for wire bond attachment) were isolated from each other. Each metalized substrate passed a mega-ohm test at 1,000 V. Some flaking in the plating layer was noticed, but it seemed to be adhering in the critical locations (i.e., under the diode footprint).

After metallization and plating, the next step in the fabrication process was die attachment. The substrates were sent to NBE Technologies, LLC, of Blacksburg, Virginia, to have the chips soldered in position on the 12 mm flats. Soldering was chosen as the attachment method because of time restraints and because sintering requires silver plating.

NBE Technologies advised ORNL after receiving the parts that some of the gold plating was coming off with scotch tape. They were concerned about the diodes not adhering well. Once the parts were in process, NBE Technologies contacted ORNL with the information that the flats of the hexagon were extremely uneven (on the order of 0.010 in. from the center to the edge). The ceramic had a reasonably flat surface; thus the copper cladding flatness was insufficient. They also reported that they had soldered three substrates, but air gaps under portions of the diodes were visible to the naked eye. NBE Technologies advised ORNL that a surface should be flat within ~5 μm for a sintering process to be attempted. This requirement translates into a 128-microinch finish or better.

Upon receiving the parts back from NBE Technologies, ORNL had a machine shop attempt to flatten the surfaces. They were also asked to remove the plating that overlapped the edges. As they began to prepare the surfaces, they noticed that the copper cladding was moving and could not be flattened well because it was expanding from the heat and stress of the machining operation. Also they were finding air gaps under the copper cladding when the overlap was removed.

Later discussions with Aegis Technology would confirm that they attempted to braze this 0.050 in. thick piece onto the initial 0.020 in. metalized area and had to go through several reheats because the brazing material was not filling the large gap. ORNL removed the outer thick layer of copper and noticed a large amount of oxidation between the direct bonded copper and the outer copper cladding. The bonding method used to attach the 0.050 in. hexagonal copper components was unsuccessful. However, after close inspection of the surface, it was noted that the initial 0.010–0.020 in. metallization layer adhered well.

To evaluate this problem, the DBC layer was cleaned off. The parts were returned to Aegis Technology to have another layer of DBC (0.020 in.) applied. This 0.020 in. layer is deemed sufficient to carry current around the edges of the hexagonal substrate. The flats then had thicker pads (0.050 in.) brazed directly onto them. Using discrete landings will allow for a smaller gap which the braze material should fill with

ease. The parts were returned and cleaned up at a local machine shop to prepare the copper surface. The problem with brazing the thicker pads directly to the initial metallization layer was still present.

The initial substrates prepared with soldered dies from NBE Technologies were sent to Orthodyne Electronics of Mineola, New York, to wire bond. Orthodyne noted that aluminum wire bonds were not adhering to the electroless gold plate very well. It is unknown whether this was due to the quality of the plating, unevenness/roughness of the plating, or a material incompatibility. Ideally, wire bonding directly onto an aluminized copper surface is best; however, wire bonds should be able to be attached to nickel-silver plating on copper or silver plating on copper. Further investigation and discussions took place to determine the best surface preparation.

To avoid compromising the ceramic parts, different plating materials and techniques were explored using sample pieces of copper. Other plating options were discussed with the die-attachment vendor (NBE Technologies) and the wire bonder (Orthodyne). For die attachment, nickel or electroless nickel should be fine for soldering. Silver plating is needed for the sintering process. Orthodyne has done previous research on aluminum wire bonding compatibility with various plating materials. They suggested using nickel or aluminum plating. They also provided the technical specifications for the nickel plating process to produce the best results (2.5–4 μm in an 8–12% phosphorous bath).

The performance of various electroless nickel samples from several vendors produced varying results. The samples finished using the specifications from Orthodyne produced the best results. Other batch samples sent for testing were heated to 300°C for 30 minutes before wire bonding. This process would simulate the heat cycle of the die attachment. No excessive cleaning was done between heating and wire bonding. Any surface oxidation caused by the elevated processing temperatures had little to no effect on the wire bonding process.

Samples of nickel-silver, silver, and nickel plated on copper were sent to NBE Technologies for evaluation. Results showed that the nickel-silver plating worked quite well. The sintering paste stuck very well on both the nonheated and the heated parts. The sintering paste did not stick to the silver on copper plating.

Samples of AlumiPlate aluminum plating were also obtained. These samples were plated with high purity aluminum on copper. These samples were sent for wire bonding and bond strength testing. Samples that were heated as received were tested, and the bonds and bond strength were very good.

Wire bond pull test results were received from Orthodyne. The conclusions drawn from the Orthodyne wire bond pull test results are as follows.

- AlumiPlate looks very promising in regards to wire and PowerRibbon bonding.
- Further work will need to be done to optimize bond parameters to increase the amount of remnant post-shear for both first and (especially) second bonds.

All of the wire pull results were breaks and not lifts. Breaks are the preferred type as that is indicative that the bond is firmly attached to the surface. A majority of the wire breaks were mid-span, which is the best mode.

From these tests, it was determined that the path forward would be to nickel-silver plate the die attachment landing, and the wire bond landings will be covered with aluminum plating by AlumiPlate.

Component Assembly

It had been determined previously that the post-brazing process on the surfaces for die attachment included abrasion blasting (or sand blasting) to remove the oxidation on the copper. This left the surfaces too uneven for sintering the dies into position, but NBE Technologies was able to attach the dies using solder. As discussed previously, the brazing process used to attach the 0.050 in. thick copper to the initial 0.020 in. metallization layer was unsuccessful. Testing of the assembled substrates would have resulted in poor heat transfer due to the voids between the initial metallization layer and the thick copper layer.

An alternate component assembly was conceived and used to validate the FEA method. Initial FEA results showed that a 0.020 in. thick metallization layer would meet the design requirements and result in a simpler, less expensive manufacturing process. A testing procedure to validate the models was developed using a 0.020 in. thick metalized ceramic substrate. This testing procedure uses power resistors as heaters placed directly onto the 0.020 in. thick metalized surface where diodes would normally be attached. Detailed measurements of the metalized substrate and power resistors were taken and this information was used to create a more accurate FEA part geometry for model validation. Additional FEA models were built and results were obtained using the power resistor testing configuration.

Because of the compromised cladding, the thermal validation tests should demonstrate accuracy between the modeling procedure and the experimentation. The test load may be reduced because of the thinner cladding, power restrictions on the resistor, and parasitic heat paths.

Instrumentation, Installation, and Testing of Assembled Prototypes in Test Apparatus

The four-hole design and the annulus design were populated with six 1-ohm 60W power resistors. Each power resistor was placed on the hexagonal flat area where the diodes were to be soldered/sintered in position. A small piece of garlite with the same footprint as the power resistor was placed on top of the resistor. The garlite piece has a slot cut into it so it will hold a thermocouple in intimate contact with the case of the power resistor for temperature measurements. This entire subassembly (power resistor, thermocouple, and garlite) is held down by a screw to maintain the surface contact between the power resistor and the metalized surface of the ceramic substrate. Each of the ceramic substrates has a piece of aluminum foam inserted into the flow channels to enhance the thermal conductivity of the ceramic into the WEG coolant. Another thermocouple is attached to each flat on the metalized ceramic substrate at the wire bond landing area. All of the power resistors are wired in series with each other.

The annulus design was configured and populated in the same manner as the four-hole design. The annulus design also had a flow diverter placed inside the inner diameter of the aluminum foam. This served two purposes: to direct the flow through the foam to reduce pressure drop and to keep the inner diameter of the aluminum foam from becoming a coolant flow diverter.

Each assembly was inserted into the test apparatus. The test apparatus contains a thermistor on the inlet side block and two thermistors on the outlet side block, 90 degrees apart. The inlet and outlet block have a pressure transducer mounted on each side to read the WEG inlet and outlet pressure. The apparatus was placed on an incline to ensure that the sight glass was full after the test section. The sight glass had remained full during pressure drop measurements because of the higher flow rates. The thermal validation testing takes place at 0.41 gpm. At this flow rate the sight glass does not stay full and thus not all the flow channel is filled with WEG. The incline ensures the substrate has WEG flowing through all channels.

Test Results of Assembled Prototypes Using 105°C WEG

The annulus design experiment was run to a maximum chip temperature of 150°C. The measured heat addition to the fluid was 64% of the design value. The reduced power level was due to the manufacturing complications previously discussed. The predicted temperature from the COMSOL model was within 6°C

of the experimental results. These results were at a coolant temperature of 105°C. At 90°C coolant temperature the experiment was run at 82% of design load at a maximum chip temperature of 150°C. Again, this lower load was due to manufacturing complications. The manufacturing complications equated to a thinner copper layer than originally planned. At 90°C coolant temperature the COMSOL model prediction was within 12°C of the experimental results.

The four-hole design results, having the same manufacturing complications, were also run at varying coolant temperature levels. The experiment was run at 79% design load with a maximum chip temperature of 150°C. The COMSOL model prediction was within 2.5°C of the experimental results with the chip location directly over a coolant channel. The COMSOL model was within 10°C of the experimental results with the chip location farther away from a coolant channel. At 90°C coolant temperature we ran at 88% design load with a maximum chip temperature of 150°C. The COMSOL model was within 5°C of the experimental results with the chip location directly over a coolant channel. The COMSOL model was within 16°C of the experimental results with the chip location farther away from a coolant channel.

Note that the model comparisons are based on thermal models that use the measured flow parameters and have geometry and cladding that reflect the average measured copper thickness on each substrate.

General Inverter Design

The FEA results from this research produced promising substrate designs. A preliminary design for the inverter package was developed using the hexagonal substrate. The package, shown in Fig. 3, contains the single-chip-deep annulus design, flow headers, capacitor, direct current (dc) power connections, and buss structures. One flow header is removed for clarity. This design has a total volume of 4.4 L at a maximum designed power level of 55 kW, which equates to a 12.5 kW/L power density. This design meets the 2015 FreedomCAR goal of 12 kW/L.

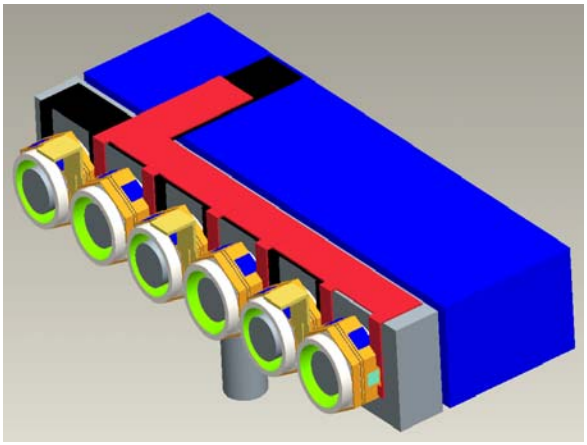

Fig. 3. Single-chip-deep annulus design.

During the development of the design in Fig. 3, the dc and phase interconnects were discovered to be problematic. One way to improve upon this design and potentially reduce electromagnetic interference is to investigate a ceramic substrate that contains the entire phase leg instead of just one switch set. A preliminary model was run for an octagonal substrate with two chip sets and is shown in Fig. 4.

The model parameters used were the updated ones found during the pressure drop testing. Also, the copper layer is only 0.020 in. thick. This design, also using 105°C WEG coolant, maintains the IGBT at

163°C, the diode at 160°C, and the coolant fluid maximum at 130°C. These temperatures are on the edge of the design limits, so future work needs to be done to make this idea more feasible.

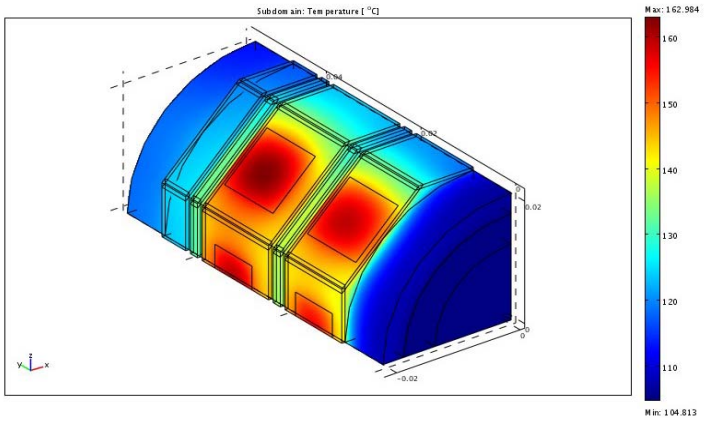

Fig. 4. Two-chip-deep annulus design.

The two-chip-deep substrate resulted in a simpler inverter concept. This design, shown in Fig. 5, contains the two-chip-deep annulus design, flow headers, capacitor, dc power connections, and buss structures. One flow header is removed for clarity. This design has a total volume of 4.1 L at a maximum designed power level of 55 kW, which equates to a 13.4 kW/L power density. This design exceeds the 2015 FreedomCAR goal of 12 kW/L.

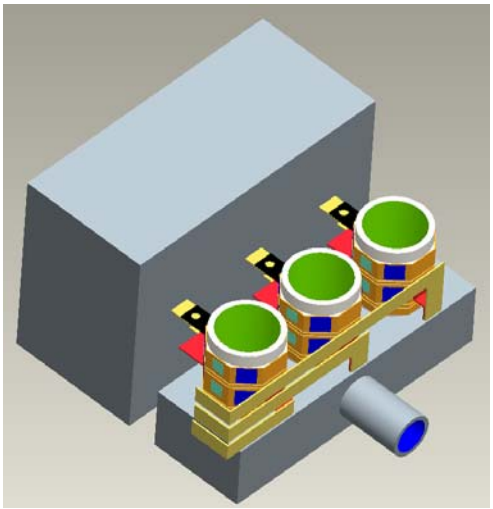

Fig. 5. Two-chip-deep annulus design.

Conclusion

The results of this research indicate that directly cooling an Al_2O_3 ceramic substrate with 105°C coolant to maintain IGBT temperatures below their maximum operating temperature is viable. The shape of the substrate, the size and shape of the capacitor, the coolant flow channels, a thermal enhancement material placed within the flow channels, and the chip population on the substrate all play key roles. The unique shape of the designs was chosen because the required surface area could be obtained within the smallest package volume. Additionally, the unique structure of the shape is far easier to seal from the coolant than other types of planer structural shapes.

The addition of a thermal enhancement material to the flow channels provided a greater surface area within the flow channels and a better profile to remove the waste heat more efficiently. This thermal enhancement material has a much higher structural integrity compared with other types of microstructures and provided a simple means of manufacture that also met the "greater than 1mm" orifice requirement imposed by car manufacturers to protect against loose particles causing blockages.

The capacitors necessary to complete the inverter design consume the majority of the total volume of the direct cooled power electronics inverter. Because this component has a larger volume than many of the other required components, volume reduction is limited by its size. With the lower cost Al_2O_3 substrate, the power density approaches 12.5 kW/L when the modules are packaged with a brick type capacitor. The use of hollow cylindrical capacitors did not yield any benefit to this particular design.

Performance testing of the preferred designs was performed to validate the FEA results. Although there were manufacturing issues with the design, the prototype that was built still provided the necessary architecture to validate the FEA model.

Publications

1. R. H. Wiles, C. W. Ayers, A.W. Wereszczak, K.T. Lowe, *Preliminary Testing Results for the Direct Cooled Power Electronics Substrate,* ORNL/TM-2009/204, Oak Ridge National Laboratory, 2009.
2. Kirk T. Lowe and Rao V. Arimilli, *Application of Solution Mapping to Reduce Computational Time for Actively Cooled Power Electronics,* 4th Annual COMSOL conference, 2008.

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1. R. H. Wiles, et al., *Preliminary Testing Results for the Direct Cooled Power Electronics Substrate,* ORNL/TM-2009/204, Oak Ridge National Laboratory, 2009.
2. R. H. Wiles, et al., *Direct Cooled Power Electronics Substrate,* ORNL/TM-2008/112, Oak Ridge National Laboratory, 2008, Tables 7–13.
3. J.-P. Bonnet, F. Topin, and L. Tadrist, "Flow Laws in Metal Foams: Compressibility and Pore Size Effects," *Transport in Porous Media*, Vol. 73, 2008, pp. 233–254.
4. A. Amiri and K. Vafai, "Transient analysis of incompressible flow through a packed bed," *International Journal of Heat and Mass Transfer,* Vol. 41(24), 1998, pp. 4259–4279.

Patents

R. H. Wiles, et al., "Direct Cooled Power Electronics Substrate," US 2009/0231812 A1, September 17, 2009.

2.2 Advanced Thermal Interface Materials for Power Electronics Applications

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Objectives

Thermal interface materials (TIMs) pose a major bottleneck to heat removal from the insulated gate bipolar transistor (IGBT) package. In a typical automotive IGBT package, the copper baseplate is attached to the aluminum heat sink via a thermal grease, which is a major contributor to the thermal resistance in the package. The performance of this grease layer degrades over time and results in even higher resistance to heat flow. In addition, for the conventional die-attach solder layer, there are concerns about their high temperature capability and thermomechanical reliability over large temperature cycling. A high-thermal performance, reliable, and cost-effective TIM would help in dissipating higher heat fluxes, which, in turn, could enable reduced die size or fewer switching devices. Reducing the thermal resistance of the TIM can also help us achieve the DOE Vehicle Technologies Program's FreedomCAR goals to use glycol water at 105°C or even air cooling. All these would help reduce the cost, weight, and volume of power electronics, which is the main goal of the FreedomCAR program area.

A project was initiated in FY 2007 to thoroughly characterize the state-of-art conventional interface materials as well as novel materials and to recommend a suitable candidate material for automotive power electronics applications.

The specific objectives for FY 2009 were as follows:

- Evaluate industry requirements for TIMs and decide on future direction(s) of the project. One conclusion from FY08 study was that existing conventional TIMs did not satisfy the thermal performance target of 5 mm^2K/W at a bondline thickness of about 150 microns. This evaluation resulted in the identification of promising bonded interfaces as an area for investigation.
- In conjunction with Virginia Tech, characterize thermal resistance/performance, using the NREL ASTM steady-state approach, of novel sintered materials based on silver nanoparticles.
- In conjunction with Btech, characterize thermal resistance/performance, using the NREL ASTM steady-state approach, of novel thermoplastics with embedded carbon fibers.
- Establish the transient thermal tester (T3ster) for in-situ package thermal resistance measurements at NREL.

Approach

- We conducted a detailed quantitative assessment of the power electronics industry's requirements for TIMs. This assessment, which included interactions with original equipment manufacturers (OEMs) such as General Motors and Ford, and suppliers such as Delphi, Infineon, and Semikron, led to the development of a FY 2010 project at the National Renewable Energy Laboratory (NREL) on bonded interfaces, in situ package performance, and the reliability of the interface.

- In conjunction with Virginia Tech, we performed initial thermal resistance characterization, on the NREL ASTM test apparatus, of sintered and soldered (lead-free) interfaces between 31.8 mm (1.25 inches) diameter copper and aluminum disks.
- In conjunction with Btech and Delphi, we performed initial thermal resistance characterization, on the NREL ASTM test apparatus, of 31.8 mm diameter copper disks bonded together with thermoplastic having embedded near-vertical carbon fibers.
- The NREL ASTM TIM test results are based on experiments on a small area (less than 8 cm^2) under controlled loading conditions. It is important to understand the thermal performance of TIMs applied over a much larger area in an-situ package configuration under more realistic loading conditions. Hence, we established the transient thermal tester (T3ster) for in-situ package thermal resistance measurements. In conjunction with a benchtop environmental chamber established at NREL, the thermal transient tester also enables study of TIM reliability in an in-situ package configuration.

Major Accomplishments

The following are the main accomplishments of this project in FY 2009:

- Via interactions with OEMs and suppliers, identified bonded interfaces as a promising avenue for further investigation. Provided they are reliable, bonded interfaces are also desirable from a packaging perspective.
- In conjunction with Virginia Tech, established a thermal performance of 5 mm^2K/W for a 65 microns sintered interface (based on silver nanoparticles) between 31.8 mm diameter copper disks; a soldered (lead-free) interface of 200 microns between 31.8 mm diameter copper disks yielded a thermal resistance of 4 mm^2K/W. All these results were obtained on the NREL ASTM steady-state test apparatus. These initial thermal results for sintered interfaces are promising from a viewpoint of applicability in power electronics packages. For perspective, a thermal resistance of 5 mm^2K/W for a 150 microns bondline thickness was set as a target because the TIM stops being a bottleneck to heat transfer at these resistance values. The initial performance of the soldered interface is very promising; however, there are concerns with thermomechanical reliability of soldered joints. Comprehensive reliability data (thermal performance) for the Virginia Tech synthesized material remains to be investigated.
- In conjunction with Btech, established a thermal performance of 12 mm^2K/W for a 100 microns thick HM2 thermoplastic (with embedded carbon fibers) between two 31.8 mm diameter copper disks. These again are very promising results.
- Tested a number of materials (via NREL ASTM approach) for other industry partners under a work-for-others agreement or other DOE project funding.
- Established the transient thermal tester in the power electronics laboratory at NREL. Performed initial experiments to characterize the thermal resistance of a Dow TC5022 grease placed between a Semikron package and a cold plate.

Future Direction

The following activities are planned for FY 2010 and beyond:

- We will work with Btech, Delphi and NREL materials scientists to improve the performance of the HM2 thermoplastic with embedded carbon fibers. We will also extract the contact resistance and bulk thermal conductivity of the material.
- We will work with Virginia Tech to extract bulk thermal conductivity and contact resistance of sintered/soldered materials. We will explore techniques to lower the bonding temperature and pressure for the material, alternative less expensive (to silver) particle formulations, as well as formulations with reduced curing times.
- We will work with Btech, Delphi and NREL materials scientists to characterize thermomechanical reliability of bonded thermoplastic interfaces - preferably in an in-situ package framework.

- We will work with Virginia Tech to characterize thermomechanical reliability for both sintered and soldered joints – preferably in an in-situ package framework.
- Working with partners, we will characterize appropriate mechanical properties of bonded interfaces.
- We will continue interactions with industry to better understand applications, material requirements and transfer results to industry.

Technical Discussion

Background

Thermal interface materials are a major obstacle to heat removal in electronic packages. Figure 1 shows a typical power electronics package. Three of the interfaces in the package need to be improved — the two solder layers (from a reliability viewpoint) and the TIM layer.

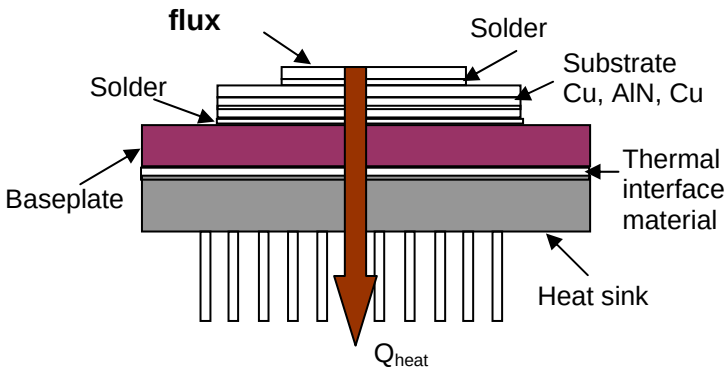


Fig. 1. A typical power electronics package

During the past three years, work at NREL [1, 2] has focused on establishing a consistent, objective, and high-accuracy database, via the ASTM steady-state approach [3], on the thermal performance of conventional as well as novel thermal interface materials. The conventional materials include greases, gels, phase-change materials, indium, and filler pads. Some novel materials based on carbon nanotubes, thermoplastics with embedded carbon fibers, and sintered materials based on silver nanoparticles have also been explored. Interactions with industry revealed an inconsistency in prevailing TIM performance data in the open literature, and the need for an objective and consistent database of TIM thermal performance. There are a number of techniques for measuring the thermal resistance of materials, and typically, different TIM manufacturers provide material performance specifications using different techniques. The work at NREL has provided an objective, consistent and high-accuracy [4] database of the thermal resistance/performance for an array of TIMs using the ASTM steady-state technique. Comparisons have been made between the NREL steady-state approach and the laser flash method used by Delphi for a number of materials. The match between the results from the two methodologies has been good (within 10% for a majority of cases). In addition, good match (within 5%) has also been shown between the thermal conductivity results, for a NIST reference material (yttria-stabilized zirconia), obtained from the NREL ASTM test apparatus and the NIST guarded-hot plate approach. In view of these results, we have developed strong confidence in the results from the NREL test apparatus.

The objective database established at NREL is directly helping industry partners make product development decisions. In particular, NREL has provided feedback/results to Delphi, Semikron and UQM, on a number of TIMs of interest to these companies. Significant interactions with the staff at Delphi have been very helpful in the identification of requirements of TIMs. The results for a number of

materials have also been communicated to the technical staff at Ford. In FY2009, NREL has begun interactions with GM and Virginia Tech on establishing the thermal resistance/performance of interfaces based on sintered materials (material based on silver nanoparticles). In doing so, we have responded to an industry request to develop an objective, detailed, high-accuracy database on the performance of sintered interfaces – similar to what we have done in the past with other TIMs. We also initiated closer collaborations with Btech, a small company based in Colorado, to investigate thermoplastics with embedded carbon fibers. This material is another example of a bonded interface. There is an industry trend towards bonded interfaces in part due to its advantages from a packaging perspective. However, there is limited data in the open literature on the thermal performance and reliability of these interfaces. The work initiated at NREL seeks to address this gap. A report on the evaluation of industry requirements for TIMs has been provided to DOE by NREL [5].

Concerns with solder interfaces

Solder is the most predominantly used bonded interface material in a power electronics package. Typically, solder is used to attach the silicon die to the substrate (either direct-bond copper (DBC) or direct-bond aluminum (DBA) substrate). However, solder (even lead-free) is believed to undergo degradation at elevated temperatures above 120°C. In addition, solder joint fatigue can occur over smaller temperature range cycling over a period of several years. The larger the area of the joint, the more likely that the failure of the joint will occur when the adjacent substrates have different coefficient of thermal expansion. This is the reason why a solder attachment between the DBC or DBA substrate and the baseplate is more susceptible to failure than the silicon die-attach solder layer. Typically, in industry, the temperature cycle testing is an accelerated test – with the solder joint subjected to a cycle ranging between -40 and 150°C. It is due to these concerns that a high-thermal performance, low-cost, reliable bonded interface material continues to be an area of investigation.

Sintered interfaces

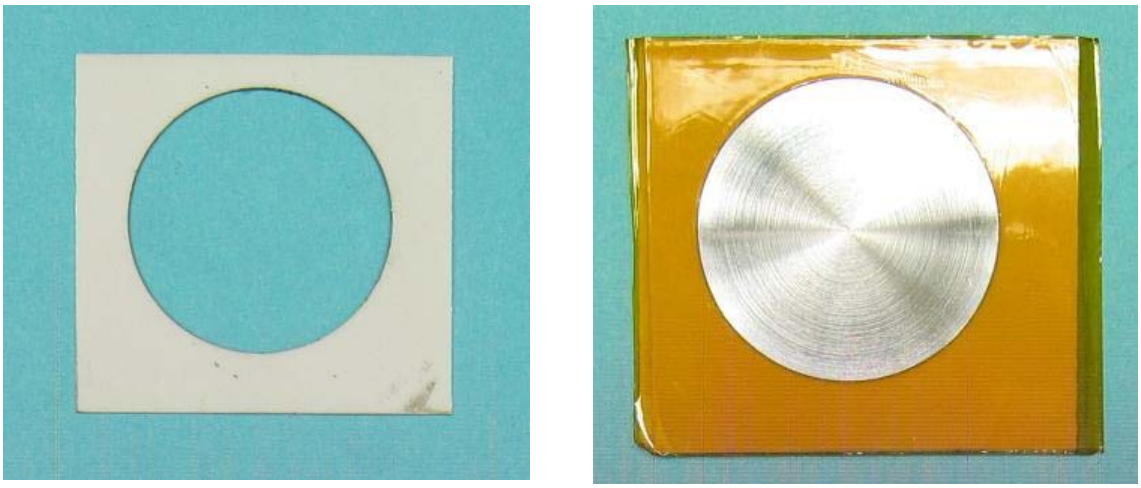
Sintered interfaces are beginning to be used in advanced power electronics packages [e.g. 6]. However, in the technique referred to in [6], the silver particles for the sintered interface are likely in the micron range due to which very high pressure (~40 MPa [6]) is required to keep the maximum sintering temperature at 280°C. In addition, there are questions about the optimal material composition, thermal performance, mechanical properties and reliability of these interfaces. In the work presented here in collaboration with Dr. G.-Q. Lu at Virginia Tech, novel silver nanoparticles-based paste [7-9] has been used due to which the sintering pressure is on the order of only 3 MPa with the maximum sintering temperature at 275°C. Sintered interfaces were synthesized between 31.8 mm diameter copper and aluminum disks. For the results reported here, a nickel coating (~ 2 μm) followed by a pure silver coating (again ~ 2 μm) was applied on the copper and aluminum disks prior to the sintering process. The intent of the silvering the disks is to promote a good diffusion bond between the disks and the silver-based paste. A description of the synthesis, which was performed by Dr. Lu's group at Virginia Tech, is given below. In this description, two plain aluminum disks (i.e. without any silver coating) have been sintered together. This is only for the demonstration of the process; results are presented for silvered disks sintered together.

Stencil printing of nanoscale silver paste

Alumina (Al_2O_3) stencil is firstly fabricated to (1) mount the metal disk; and (2) stencil print nanoscale silver paste. Figure 2 shows an example alumina stencil. By placing different number of Kapton tapes under the alumina stencil, the printing thickness of the silver paste can be controlled. Figure 3 shows an example of an aluminum disk before and after printing of the silver paste.

Sintering of Ag paste

Figure 4 shows the heating profile used to sinter the silver paste. The formation of the sintered attachment can be considered to occur in two stages: (a) low-temperature (room temperature to 125°C) drying of solvent, and (b) high-temperature (275°C) organic binder burnout and the simultaneous sintering of silver particles. Since the attachment area is considerably large, the "double-print" technique is applied to achieve better sintering of the silver paste, and also helps in better controlling the paste's thickness. After one layer of the silver paste, typically between 40 µm and 100 µm, was printed on the metal disk, it firstly went through the drying process up to 125°C, so that most of the organic solvent was evaporated uniformly without cracking the paste layer. Before mounting the topside metal disk, a second paste layer, between 10 µm and 50 µm was printed on top of the dried paste layer, to increase the bonding thickness and provide better adhesion layer to the topside metal disk.



(a) (b)

Fig. 2. Alumina (Al_2O_3) stencil for disk attachment: (a) fabricated alumina stencil, with 31.8 mm diameter hole; (b) aluminum disk mounted in the alumina stencil.

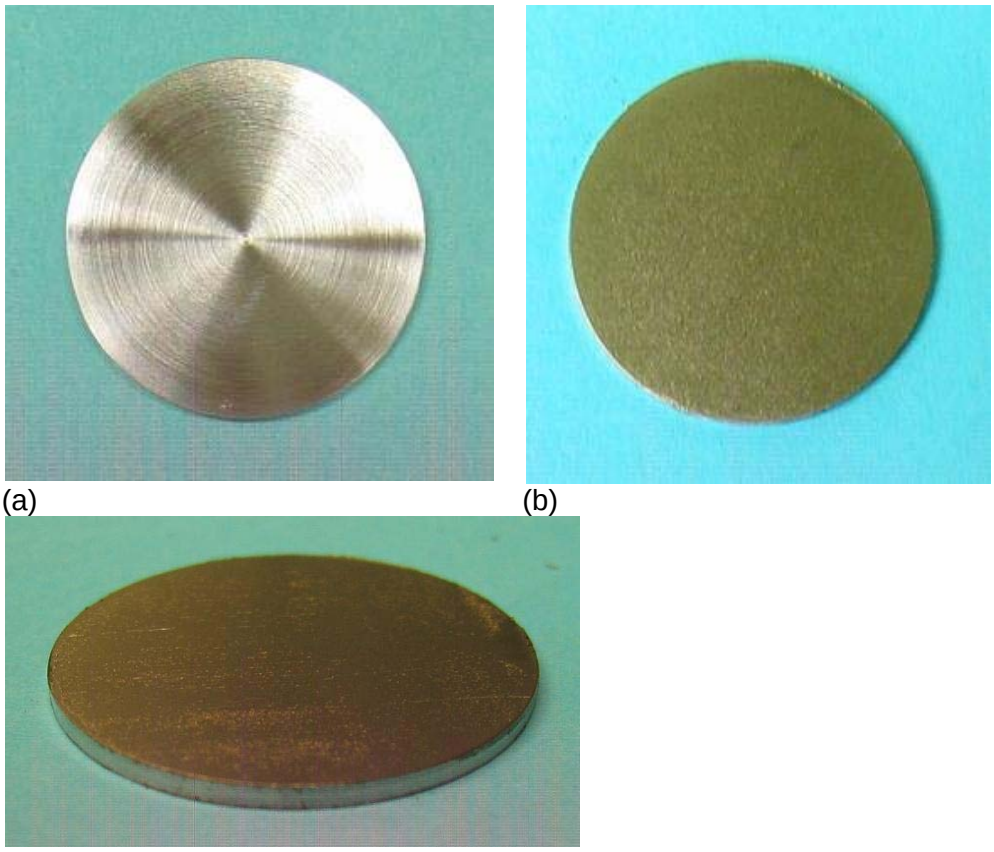


Fig. 3. Aluminum disk: (a) before stencil printing of silver paste; (b) after printing of silver paste; (c) side view of aluminum disk after printing of silver paste.

An external mechanical pressure (3 MPa) was applied during the sintering stage of the silver paste to ensure good contact between the substrates and the paste. This pressure was also beneficial in counteracting the opposing force caused by the outgassing of the organic components, and helped in forming a denser silver microstructure after sintering. Figure 5 shows the hot-press that was used to provide heat and pressure during the final sintering stage (Figure 4).

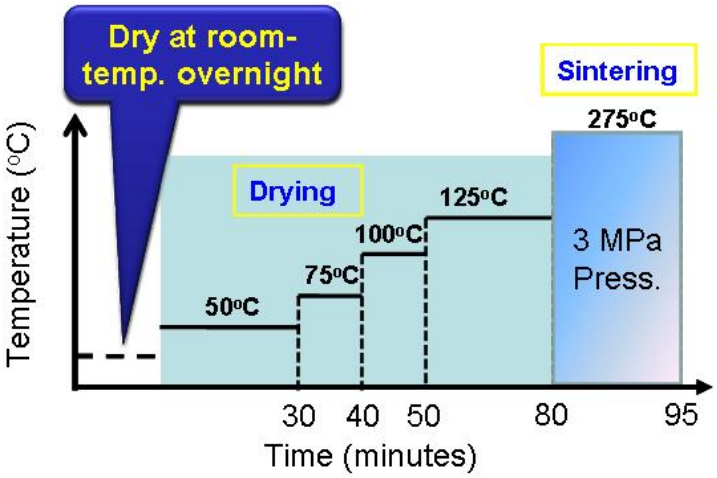


Fig. 4. Heating profile to synthesize the sintered attachment.

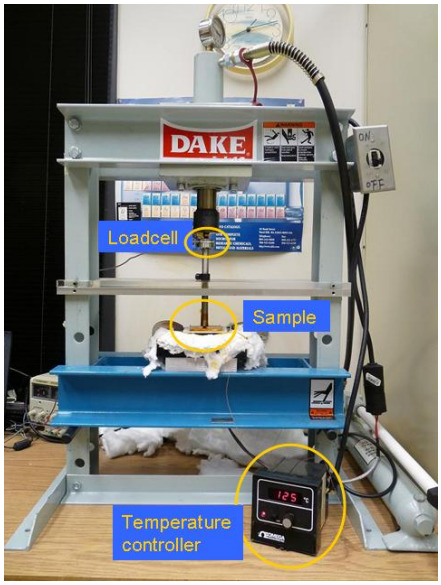


Fig. 5. Hot press.

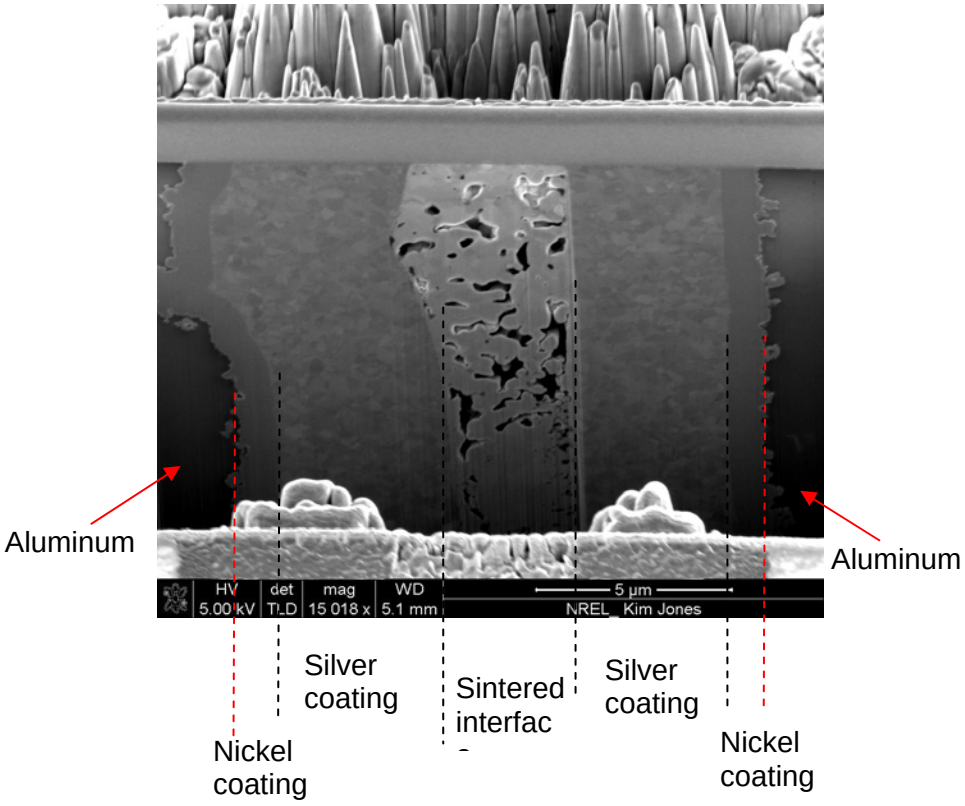


Fig. 6. SEM micrograph of a silvered Al-Al sintered interface showing porous microstructure

Results for sintered and lead-free solder interfaces

The thermal resistance results of the sintered and lead-free solder (SN100C containing Sn (Tin), Ni (Nickel), Cu (Copper), Ge (Germanium)) interfaces were obtained using the NREL ASTM steady-state approach which has been described in [1, 2]. The lead-free solder joint (also synthesized between copper disks by Dr. Lu's group at Virginia Tech) was investigated to provide a baseline for comparison with the sintered joint results. Figure 6 shows the SEM micrograph of one of the sintered Al-Al (aluminum) samples. This shows clearly the porous microstructure of the sintered interface. This is the rationale for using a sintered interface as opposed to a soldered joint [7-9]; soldered joints are believed to have poor thermomechanical reliability during cycling over a large temperature range. The preliminary thermal resistance results for the various sintered and soldered interfaces are shown in Table 1. The thickness of the sintered/soldered layers was determined by taking micrometer measurements of the disks before and after the sintering/soldering process. Some of these thicknesses were also confirmed via microscope imaging of the edges of the samples. There is a need to develop multiple such samples in order to observe the impact of preparation techniques on the sample thickness. During the experiments at NREL with the apparatus described in [1, 2], the sintered/soldered disks were placed between two measuring blocks, and a 25 micron thick Dow TC5022 grease layer was used as an interface between the disks and the measuring blocks. The resistance of the two grease layers as well as the two disks (either copper or aluminum) was subtracted out from the total measured resistance in order to get the resistance of the sintered layer. Due to this subtraction process, it is expected that the uncertainty in the thermal resistance results could be of the order of ±1 mm^2K/W (uncertainty in the grease layer resistances). All results discussed below are for an average sample temperature of 65°C and a pressure of 276 kPa.

The results in Table 1 show consistent results for the silvered Cu-Cu sintered layers, though there is no clear trend of overall thermal resistance with thickness of the sintered layer. It is possible that the contact resistance for the different samples is different, thereby precluding a clear trend of resistance versus thickness. Still, the overall resistances of all samples are below 8 mm^2K/W, with the 64 micron thick sample resistance at 5.4 mm^2K/W - which is a very promising thermal performance. For two of the silvered Al-Al sintered samples, the sintered interface resistance is high (14.9 and 25.2 mm^2K/W). This suggests some compatibility issues in the sintering process involving silvered Al and silver paste. This is an aspect which certainly needs to be explored further, because Al is a very commonly used material in power electronics packages.

Table 1: Sintered and soldered interface thicknesses along with thermal resistance results

Samples	**Thickness (μm)**	**Resistance (mm^2K/W)**
Silvered Cu-Cu sintered interface	20	5.8
Silvered Cu-Cu sintered interface	27	8.0
Silvered Cu-Cu sintered interface	64	5.4
Silvered Al-Al sintered interface	28	14.9
Silvered Al-Al sintered interface	103	25.2
Silvered Al-Al sintered interface	144	5.0
Cu-Cu soldered interface	80	1.0
Cu-Cu soldered interface	150	4.8
Cu-Cu soldered interface	200	3.7

The lead-free soldered interface resistance results look very promising with all thicknesses upto 200 microns yielding thermal resistances less than 5 mm^2K/W. This brings up the issue of the advantage of sintered joints over lead-free solder joints. The rationale for exploring alternative options to lead-free solder has often been the poor thermomechanical reliability of solder joints over large temperature cycling [7-9], leading to thermal stresses due to the coefficient-of-thermal-expansion mismatch between the bonding layers, and consequent cracking in one of the layers. It is hypothesized [7-9] that sintered materials are more porous and compliant than solder, and hence the thermal stresses due to cycling in packages with sintered layers may not be as high as those in packages with solder joints. We plan to thoroughly explore these aspects related to reliability in an in-situ package framework.

If we want to extract bulk thermal conductivity via this ASTM technique, we may have to synthesize sample (i.e. either soldered or sintered interface) thicknesses spanning a much wider range of thicknesses (perhaps 0.5 to 2.5 mm thick). Then the thermal conductivity can be extracted from the resistance versus sample thickness curve. An alternative may be to explore techniques like the time-domain transient

thermoreflectance [10] approach for extracting both the contact resistance as well as the bulk thermal conductivity of the sintered/soldered material in a single experiment.

Bonded interfaces based on thermoplastics with embedded carbon fibers

Another class of bonded interfaces we explore is thermoplastics (polyamide) with embedded carbon fibers. There is work done in the literature [11, 12] with adhesive/bonded joints based on carbon nanotubes embedded in epoxy. The work we present here in collaboration with Btech, a small company based in Colorado, is based on cost-effective pitch carbon fibers embedded in a polyamide matrix. The volume fraction of the fibers, which are 8 to 10 microns in diameter, is 40%. Figure 7 shows a SEM image of the ends of the pitch carbon fibers embedded in the polyamide. The collaboration with Btech is geared towards synthesizing a bonded interface material which would meet the thermal performance goals in a power electronics package, be reliable, cost-effective, and be easily integrated into the power electronics package fabrication process.

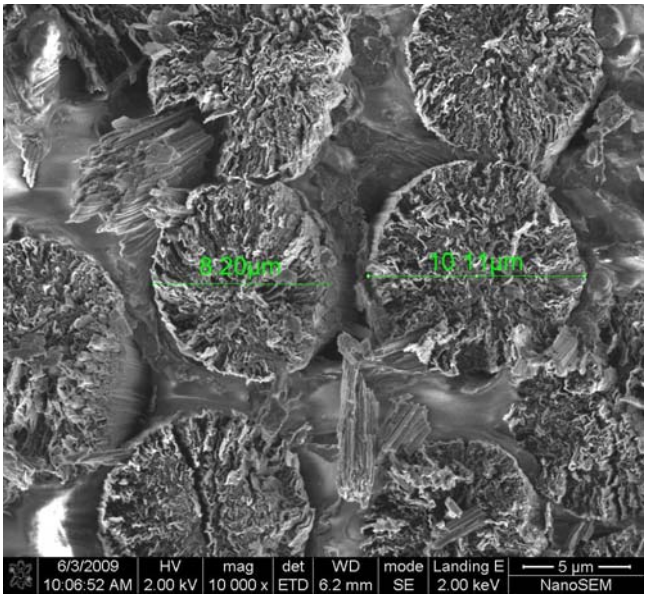


Fig. 7. SEM image of pitch carbon fibers embedded in thermoplastic.

We have bonded the Btech HM2 thermoplastic films between 31.8 mm diameter copper disks. Figure 8 shows the bonding procedure at NREL. The thermoplastic film is placed between two 31.8 mm copper disks, subjected to a load (310 kPa - Figure 8(b)), and then heated in an oven/chamber till the temperature of the film reaches 175°C. After this temperature is reached, the sample is allowed to cool back down to room temperature. When the temperature of the film reaches 175°C, the thermoplastic changes phase and during the cooling down process, the bond is formed. The temperature of the sample is monitored via a thermocouple.

Results for the thermal resistance of the samples are presented in Table 2. All results are obtained for an average sample temperature of 65°C and 276 kPa pressure.

Table 2: Thermal resistance results for HM2 thermoplastic with embedded carbon fibers.

Thickness (µm)	Resistance (mm^2K/W)
48	28.1
96	11.8
174	16.9

The final thickness of the samples after bonding is measured via a microscope and these are the thicknesses reported in Table 2. Typically under a load of 310 kPa, the films undergo a reduction in thickness of the order of 15% with respect to the original thickness during the bonding process. Clearly, there appears to be a problem with the bonding of the sample with 48 microns thermoplastic film thickness – as indicated by the relatively high thermal resistance value of this sample. The thermal resistance values of the 96 and 174 microns thick film are promising. But there is a potential for further improvements in the performance of these films. We continue to work with Btech and NREL materials scientists to treat the fiber ends as well as substrates in order to further cut down on the interfacial resistance, as well as explore alternative resins.

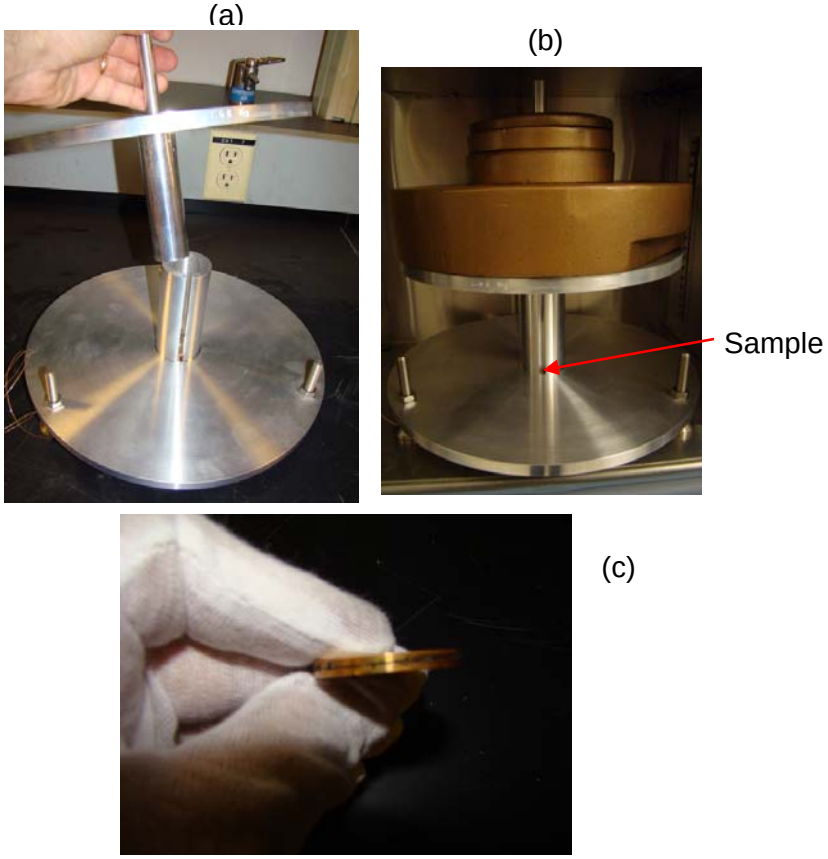


Fig. 8. Bonding of thermoplastic sample, (a) Fixture in which disks with thermoplastic film in between are placed, (b) Application of load and heating in the environmental chamber, (c) Bonded disks.

Implications of results for power electronics packages

The thermal results in the previous sections are promising. Figure 9 shows the temperatures in a typical power electronics package; these results have been presented in [1, 2]. Mainly the results indicate that when the resistance of TIMs approaches 5 mm^2K/W, TIMs are no longer a bottleneck to heat transfer, as evidenced by the very small temperature rise across the TIM.

Transient thermal resistance measurements with T3ster

The transient thermal tester (T3ster – [13, 14]) capability has been established at NREL. Figure 10 shows tests being conducted on a Semikron package. Initial tests are being performed to characterize the thermal resistance of the Dow TC5022 grease placed in between the Semikron package and the cold plate. Results will be presented in the near future. The intent of establishing T3ster in the laboratory was to test the thermal resistance of promising materials (such as those presented in the previous sections) and also characterize the impact of aging and thermal cycling on the thermal resistance in a realistic in-situ power electronics package framework.

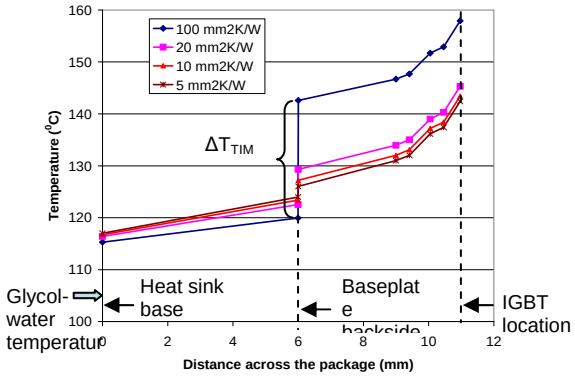


Fig. 9. Temperature across a representative power electronics package [1, 2].

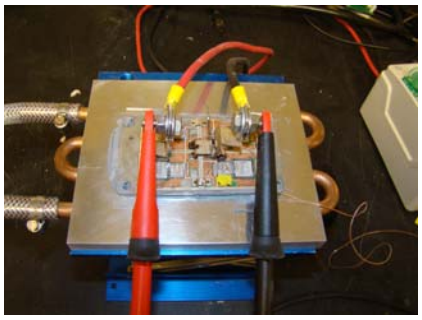


Fig. 10. A Semikron power electronics package being tested via the transient thermal tester.

Conclusions and Next Steps

An evaluation of industry requirements revealed a need to investigate thermal performance and thermomechanical reliability of novel bonded thermal interfaces. A preliminary investigation, based on the ASTM steady-approach, was performed to evaluate the thermal performance/resistance of sintered interfaces based on silver nanoparticles, and thermoplastics with embedded micron-sized carbon fibers. Promising results were obtained for both sintered interfaces and thermoplastics – approaching the target thermal performance of 5 mm^2K/W.

Work in FY2010 will focus on the following:

1. Working with the 31.8 mm diameter samples, extract bulk thermal conductivity and contact resistance of sintered and soldered samples.
2. Establish sintered interfaces between layers in a realistic-size power electronics package and test the resistance of the various layers including the sintered layer via the transient thermal tester established at NREL.
3. Cycle the package (with the sintered layer) in a benchtop environmental chamber, and then test (via the transient tester) the thermal resistance after certain cycles (establish reliability).
4. Test mechanical properties of the sintered interface (shear strength, various moduli, and performance under fatigue load testing).
5. Fabricate lower synthesis temperature (~ 180-200°C) sintered interface – between 31.8 mm diameter silvered copper disks, and test thermal performance (via our ASTM tester).
6. Explore other alternative material formulations for bonded interfaces. This includes alternative particles systems to silver, as well as different synthesis techniques for establishing a bonded interface.
7. Working with Btech and NREL materials scientists, modify and improve the thermal performance of the HM-2 thermoplastic material through understanding and eliminating the interfacial thermal resistance between the film and the substrate. In addition, also explore use of resins with lower viscosity.
8. Repeat steps 1 through 4 for the novel thermoplastic material.

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2.3 Characterization and Development of Advanced Heat Transfer Technologies

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Objectives

The overall objective of the advanced heat transfer technologies task is the development of the cooling methodologies to enable high heat flux dissipation while maintaining low die operating temperatures, with the aim of achieving the APEEM goals of cost, volume, mass, and life. One approach involves the use of aggressive cooling methods that include jet impingement and spray cooling amongst others. The second approach and that which is addressed in this report, is one that evaluates and utilizes materials in the confines of an electronic package, in order to meet the thermal performance, cost and weight targets. The two approaches are intimately linked. The power electronics package, which includes the device layout, material selection, and topology define the overall package thermal resistance, the required heat flux levels, and the induced thermal stresses. Conversely, aggressive heat transfer performance may enable higher power densities and novel package designs.

With respect to the materials approach subtask, a long term objective involves the development of a methodology to quantify the thermal, cost and weight impact of a particular material set taking into consideration the package design and cooling method employed. In this regard, the aspiration particular to this year was a preliminary investigation of materials that may affect performance benefits.

Approach

- Identify different layers in an electronic package and their functionality
- Survey literature for legacy, present and advanced materials
- Tabulate relevant thermo-mechanical properties of select materials.
- Isolate the relevant material property metric to assist in comparison

Major Accomplishments

- Identified materials that may be incorporated in the package so as to meet performance/weight/cost goals.
- Explored the use of optimization routines so as to minimize material use and consequently reduce raw material cost.

Future Direction

- Develop a modeling methodology incorporating numerical code to establish the impact of the material set selected, on thermal and thermo-mechanical performance.
- Employ commercial code to assist in the material selection process.

- Understand the details and assumptions involved in the optimization routines so as to implement them appropriately.

Technical Discussion

Introduction

This report serves as a preliminary assessment of materials that may affect performance benefits with respect to an power electronic package. The report is organized as follows: The motivation behind this material study is briefly stated, following which a generic material selection strategy is laid out to set the tone for the paper. The basic functions of the components of a generic electronic package are then presented so as to appreciate the material requirements. In parallel, the legacy materials used at each constituent layer are made known. Thereafter, materials that have been identified as 'advanced' are mentioned and tabularized. Next, the use of topology optimization as a method to reduce material use is presented.

The primary drivers in the widespread use of electric power train based vehicles are cost and efficiency. One way of addressing both aspects is that of weight reduction in a vehicle, wherein the challenge lies in reducing weight without sacrificing performance. It is in this light that this study is conducted with the goal of reducing the weight and cost of the power electronics packages and subsystem, with an emphasis on enhancing the thermal dissipation capability. To this goal two approaches are evident. The first involves the use of lighter and better performing materials, while the second applies optimization of designs so as to minimize the quantity of the material used while maintaining the thermal/structural integrity of the component. The first approach is addressed next.

Past work within the group (Abraham, 2008) identified several alternative materials for three different package topologies. A combinatory exercise was conducted to explore the effect of the materials on the maximum junction temperature at the diode though numerical means, and estimate cost based solely on bulk material cost. The substrate and cold plate were further identified as layers of greatest potential cost reduction. This study builds upon the previous work, but includes a wider range of advanced materials, establishes a thermo-mechanical metric for evaluation, and in the future seeks to establish a better measure of cost.

Material selection is an integral part of the design process of any component and may be thought of as a constituent of the function, shape, and process parameters involved in a design (Ashby, 2005). It is the interaction between the above mentioned four areas that lends itself to the subtleties and complexities of material selection. This being said, a formalized framework may be adopted to help reduce the plethora of viable material candidates to a manageable few. As adopted from Ref (Ashby, 2005), the first of the steps involves the translation of the requirements of the element to that desired in the material. This more tangibly is presented as stating the function, constraints, objective, and free variables in the design. The second step entails the screening of materials that immediately do not meet the constraints specified above. The third step and a key one at that, involves the development of relevant material indices that may be used as measure of performance. It is this metric that is maximized or minimized as the problem is defined, so as to determine the materials that optimize the solution. The fourth and final step involves a detailed investigation of the reduced set of materials obtained thus far, in terms of evaluating the cost, manufacturing process, interaction between materials amongst others.

Electronics Package and materials

It is clear from the above description the component function is intrinsically tied into material selection. With the gamut of electronics package designs available (Myer, 2006), it is not possible to set down a fixed material list. Thus, we present a generic electronics package that contains all the functionality of present day packages, identify the function of the constituent layers, and then list the legacy and advanced

materials employed. With some small further effort, this may be translated to the other package topologies.

An electronic package is comprised of following layers (Figure **1**): semiconductor, die attach, substrate, substrate attach, base plate, thermal interface material, and heat sink.

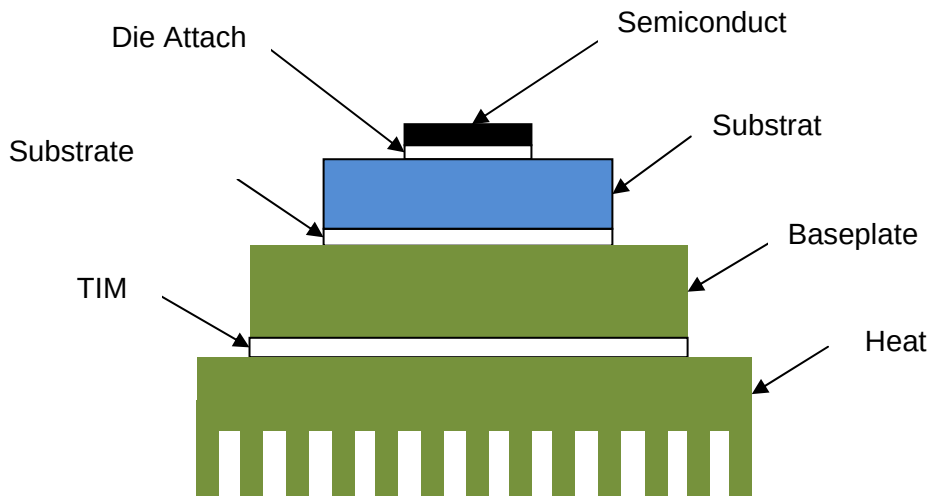

Figure 1. Sample stack up of a generic electronic package.

The semiconductor is the core of the package and contains the circuitry required to perform the desired electronic functions. Traditionally germanium and silicon were employed as semiconductor materials, with silicon being the dominant material of present day devices. So as to perform at higher temperatures and switching frequencies, compound semiconductor such as gallium arsenide and silicon carbide are made use of. With the reduction of transistor size and increased power density, the semiconductor material must maintain electrical integrity, and from a thermal perspective exhibit the capacity to dissipate heat. This translates directly to a material with a desired high thermal conductivity. Table 1, lists the thermal conductivity of select semiconductor materials. Control of the semiconductor material is beyond the scope the program. However, once it has been selected its coefficient of thermal expansion (CTE) plays a significant role in selecting the rest of the materials in the stack up on account of the thermo-mechanical stresses that develop due to CTE mismatch.

Table 1. Semiconductor materials

Semiconductor Materials	Thermal Conductivity (W/mK)
Silicon	150
Silicon Germanium	150
Silicon Carbide	155
Gallium arsenide	45
Indium Phosphide	97
Germanium	77
Gallium Phosphide	133
Gallium Antimony	33
Gallium Nitride	16–33
Indium Arsenide	35
Indium Antimony	19

The die attach serves to couple the die to the substrate. With the exception of flip-chip technology, the active side of the die faces up, while some adhesive material serves to affix the surfaces. In primarily serving a mechanical function, the die attach serves as a medium to reduce the stresses brought about by differential thermal expansion of the die and substrate and is thus prone to fatigue failure. Both hard and soft attach material exist, with polymer and lead based solders being examples of the former, and gold-based eutectics as those of the latter. With the above stated functionality of the die attach, a high thermal conductivity, and a CTE intermediate between the die and the substrate are desired properties. Filler materials such as silver are additionally incorporated into organic adhesives to enhance the aforementioned properties. Table 2, lists the thermal conductivity and CTE of select die attach materials. Once a substrate and die have been selected an appropriate die attach may be selected or even tailored.

Table 2. Die attach materials

a	Thermal Conductivity (W/mK)	CTE (ppm)
Sn63	51	25
Gold-silicon	27	12.3
Indium-lead	38	28
Indium-silver	73	22
Silver Glass	60- 80	16-21
Organic Adhesives	0.8-60	-

The substrate serves as a thermal pathway and as an electric insulator in the stack up. They may be insulated metals, organics, or ceramics. The upshot of their primary functions is a high electrical resistivity, high thermal conductivity and a CTE that closely matches both that of the die and the base plate. It is now starting to be evident as we progress that the selection of the materials in each constituent layer is highly dependent on materials used in other layers. The flexibility of the overall package design permits a variety of different substrate types. One type are ceramic based substrates, the most prevalent of which are alumina based multi-layer substrates (e.g. Direct Bond Copper (DBC), Low Temperature Co-fired Ceramics (LTCC)), and aluminum nitride. Substrates may contain metal and dielectric layers, as well as possible metallic vias that all serve to enhance the functionality of the substrate, and thus the

thermal properties are highly dependent on the constituent design. Table 3, lists the thermal conductivity and CTE of select substrate materials. LTCC, AlN and diamond show desirable qualities in that they do exhibit high thermal conductivity as well as CTE's that are comparable to Si.

Table 3. Inorganic Substrates[

Inorganic Substrate	Thermal Conductivity (W/mK)	CTE (ppm)
Alumina (92-99.99%)	17-30	6.3-7.4
Beryllium oxide 99.5%	248	6.4
Aluminum nitride	170	4.2
LTCC	2.0–4.4	4.5–8.0
CVD diamond	1300–2000	2

The substrate attach as the name suggests affixes the substrate to the package. Depending on the design, the substrate attach may be either electrically conductive or not. The most commonly used are solders (e.g. Sn-63), however polymeric thermoplastics/thermosets are also used. Table 4, lists commonly employed organic substrate attach materials.

Table 4. Organic adhesives

Organic Adhesives	Thermal Conductivity (W/mK)
Thermoset-conductive	1.6-60
Thermoset-nonconductive	0.8
Thermoplastic-conductive	1.6-20
Thermoplastic-nonconducting	1.6-12

The purpose of the base plate in non flip-chip packaging is primarily to provide mechanical support and heat dissipation. Several of the legacy and more advanced materials that are of relevance to base plate design are given in Table 6.

Thermal Interface Materials (TIM) primarily serve to reduce the thermal resistance that arises due the lack of planar contact between two interfaces and the low thermal conductivity of air present in the interfacial imperfections. In serving to also reduce the thermo-mechanical stresses that may develop between the base plate and heat sink, Young's modulus and CTE are important metrics to be considered besides thermal conductivity. Solder, thermal greases, elastomers, thermally conductive adhesives, and phase change materials are presently employed as TIM's. Properties of select TIM's are mentioned in Table 6.

The heat sink once again comes in a variety of designs, based on the highest-level thermal management method utilized. Irrespective of whether fin/forced convection, or impingement cooling methodologies are employed, high thermal conductivity materials are desirous in this region. Additionally, low-density materials contribute towards the reduction in weight goal. Traditionally finned heat sinks have been fabricated from copper and aluminum alloys. More importantly, the volume and mass of the heat sink employed bestows the possibility of the greatest reduction of weight and volume amongst the six previous mentioned layers.

Table 5. Thermal Interface Materials

TIM	Thermal Conductivity (W/m-K)
Thermal grease	0.7
Sn 63	50
Mica	0.71
Phase change	4
Elastomer	6
Gap filler	1.5
Epoxy film	6.5
Diamond-filled epoxy	11.6
Underfill	0.25–1.1
Adhesive tape	0.6
Ceramic wafers	-
Alumina wafer	25
Aluminum nitride wafer	170
Beryllia wafer	217

Advanced Materials

Most of the previously noted materials may be considered legacy materials. For most purposes from a thermo-mechanical viewpoint a material with a high thermal conductivity and a matching CTE is ideal. Most legacy materials do not meet both requirements. With the constant advancement of material development, materials that possess both these properties along with low densities have been tailored. Furthermore, some of them have exhibited low bulk and fabrication costs, and have been put to use in commercial packages. A metric used in weight sensitive applications is the specific thermal conductivity defined as the thermal conductivity divided by the specific weight of the material (Zweben, 2007). This metric suggest that some advanced composite materials posses specific thermal conductivities 10 times greater than copper and aluminum.

One classification of advanced electronics packaging materials involves 6 categories (Zweben, 2007). They include monolithic carbonaceous materials (MCM's), metal matrix composites (MMC's), carbon-carbon composites (CCC's), ceramic matrix composites (CMC's), polymer matrix composites (PMC's) and advanced metallic alloys. We will briefly address each type now, with Table 7 detailing the properties of particular advanced materials. MCM's include graphite, its variants, and diamond films amongst others. They are highly anisotropic; however their in-plane thermal conductivity exceeds that of copper with both lower densities and CTE's. MMC's comprise of matrices that include aluminum, magnesium, copper, cobalt and silver with both particle and fiber reinforcements in the form of carbon, graphite, silicon carbide, and diamond. The most commonly use MMC is aluminum silicon carbide. The previous advantages are once again observed in MMC's, with it being used commercially in RF and photonic packages. CMC's include silicon carbide reinforced with diamond, which has particularly been used in heat spreaders. PMC's include polymers reinforced with glass fiber. While most PMC's do not have thermal conductivities as high as the other materials mentioned previously, they do offer ease of manufacturing, low densities and cost. These composites have been employed commercially in electronic packages, going to show that they are viable alternatives.

Table 6. Advanced Materials (Zweben, 2007)

Reinforcement	Matrix	Thermal Conductivity (W/mK)	CTE (ppm)	Specific Gravity (γ)	K/γ
	Aluminum	218	23	2.7	81
	Copper	400	17	8.9	45
-	Silicon	150	4.1	2.3	65
-	Alumina	20	6.7	3.9	5.1
-	Epoxy	1.7	54	1.2	1.4
-	Kovar	17	5.9	8.3	2
Copper	Tungsten	157-190	5.7-8.3	15-17	9-13
Natural Graphite	Epoxy	370	-2.4	1.94	190
Cont. Carbon Fibers	Polymer	330	-1	1.8	183
Disc. Carbon Fibers	Copper	300	6.5-9.5	6.8	44
SiC Particaes	Copper	320	7-10.9	6.6	48
Cont. Carbon Fibers	SiC	370	2.5	2.2	170
	CVD Diamond	500-2000	102	3.52	142-570
-	HOPG	1300-1700	-1	2.3	740-850
-	Natural Graphite	150-500	-1	1.1-1.8	136-278
-	-	700-800	-0.5	1.8	390-440
Cont. Carbon Fibers	Copper	400-420	15.5	5.3-8.2	49-79
Cont. Carbon Fibers	Carbon	400	-1	1.9	201
Graphite Flakes	Aluminum	400-600	4.5-5	2.3	174-260
Diamond particles	Aluminum	550	7-7.5	3.1	177-194
Diamond & SiC Particles	Aluminum	575	5.5	-	-
Diamond and SiC particles	Copper	600-1200	5.8	5.9	330-670
Diamond Particles	Cobalt	>600	3	4.12	>145
Diamond Particles	Magnesium	550	8	-	-
Diamond Particles	Silver	400-600	5.8	5.8	69-103
Diamond Particles	Silicon	525	4.5	-	-
Diamond Particles	SiC	600	1.8	3.3	182
-	Pyrolityic Graphite	1600-1700	-1	2.3	700-740
Copper	Tungsten	167	6.5	16.6	10
Copper	Molybdenum	184	7	10	18
Beryllium	Aluminum	210	13.9	2.1	100
E-glass Fibers	Epoxy	0.16-0.26	11.0-20.0	2.1	0.1
Invar	Silver	153	6.5	8.8	17
Cont. Carbon Fibers	Epoxy	330	-1.1	1.8	183
Cont. Carbon Fibers	Aluminum	290	6.5	2.5	116
Discont. Carbon Fibers	Aluminum	185	6	2.5	74
Discont. Carbon Fibers	Polymer	20-330	4.0-7	1.6-1.8	12-183
SiC Particles	Aluminum	170-220	6.2-7.3	3	57-73
Silicon	Aluminum	126-160	6.5-13.5	2.5-2.6	49-63

Reinforcement	Matrix	Thermal Conductivity (W/mK)	CTE (ppm)	Specific Gravity (γ)	K/γ
Diamond Particles	Copper	420	5.8	5.9	71
Beryllia Particles	Beryllium	240	6.1	2.6	92

The rather large material subset to select from advocates the use of a computer database for this screening process. Several such software exists, an example of which is the Granta Cambridge Engineering Selection (CES) software (Granta Material Intelligence) which has the capability to query a large database of materials based on given criteria. Figure 2, shows an example of a two property material selection chart that may be evoked in the software. The possibility of using several metric along with certain parameter limits to automate the material down selection process would possibly expedite the process in the future. It is recognized that fabrication, assembly and interaction issues play an equally important role in material selection. Thus once a subset of materials is selected a detailed rigorous evaluation is required.

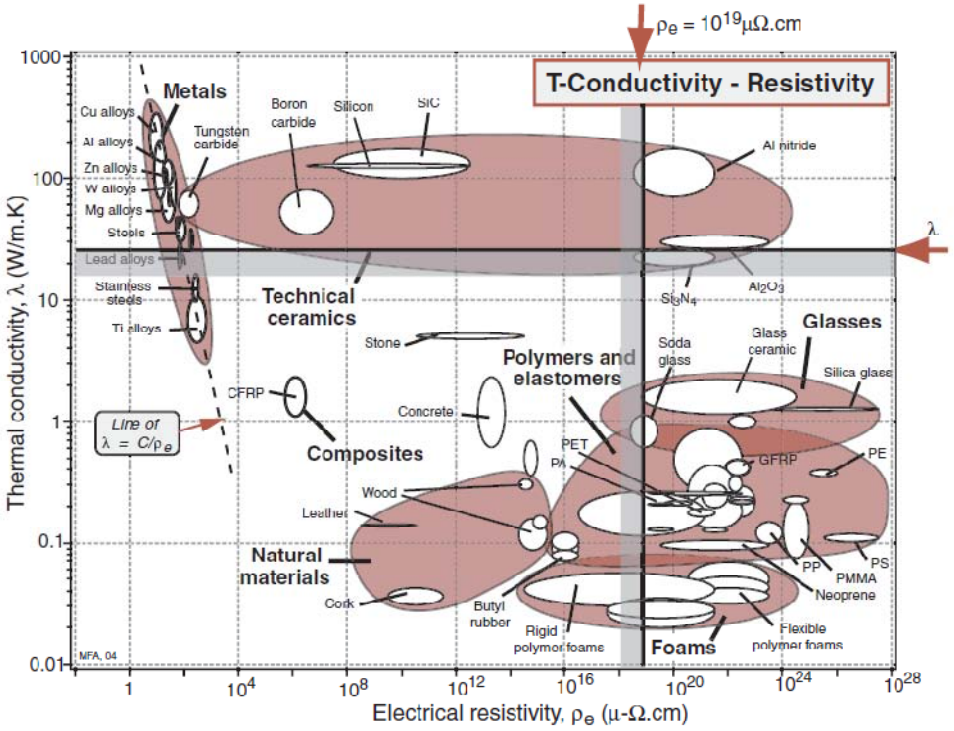

Figure 2. A two property material selection chart and selection limits, that are evoked in the CES material selection software (Granta Material Intelligence)

Cost

Cost is the most important driver for the commercial realization of a technology. With respect to the electronic package, cost estimation is not a trivial issue due to the different parameters involved and their interactions. While bulk cost is indeed one component, fabrication, assembly and ownership costs may be equally important or dominate the total cost. Each of the above are highly dependent on the maturity of the material and process involved. Further, costs associated with reliability must be given due consideration and evaluate appropriately. Particular to package cooling, it should be noted that using a highly aggressive cooling scheme may offset the use of a high cost material, or warrant the use of lower

cost, lower performance material. In this regard, one of the next steps in this material selection subtask involves creating a quantitative method of assessing cost.

Material Use Optimization

Thus far we have addressed the problem of weight reduction by evaluating materials properties. We now address this issue from a design perspective, in terms of optimizing the design of a component in order to reduce weight while maintaining the integrity of the device. This optimal use, would result in employing a material only where necessary.

Topology optimization problems may be broadly defined as determining an optimal distribution of materials (through contour and connectivity variation) in a domain where some performance function is maximized subject to constraints (Spillers & MacBain, 2009). A subset of topology optimization is shape optimization where the contour of the domain is optimized with no change in connectivity. Figure 3 shows the result of optimization (e.g. the objective is to minimize stress) of a structure subject to a load and boundary conditions. We can clearly see that a great deal of redundant material has been removed which as a consequence reduces cost.

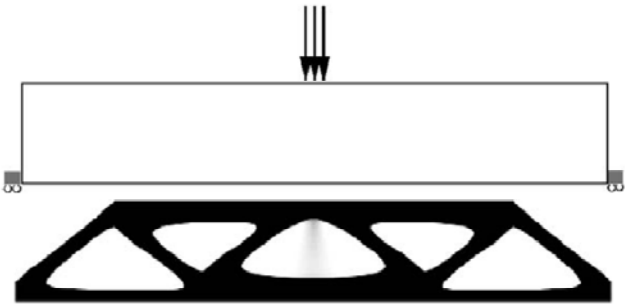

Figure 3. First picture: Initial design; Second picture: Optimized design subject to constraints (Spillers & MacBain, 2009)

While several algorithms and schemes for topology optimization exist, a few methods that have received recent attention are what may be termed evolutionary design methodologies. These include constructal theory (Bejan & Lorente, 2006) and biologically inspired methods (cellular automata (Boichot, Luo, & Fan, 2009), bionic (Xinguang, Zhixin, & Zengyuan, 2003)). These methods build upon fundamental mathematic algorithms and apply and scale them towards structures with high performance characteristics. These methods have been successfully been employed in structural, thermal and fluid domains to reduce weight, thermal resistance, and pressure drop, respectively.

Optimization routines have direct applicability to the electronic packaging domain. Within the packaging hierarchy the possibility of employing optimization routines exits at different levels. Through the package stack up prior to the heat sink, heat conduction is the dominant transport phenomena. Dendritic patterns have shown to minimize thermal resistance when the objective is transfer heat from a volume heat source (die) to a point source in the periphery (next level of packaging) (Bejan & Lorente, 2006). The method in essence allows us to answer the question: Given some quantity of high conductivity material, what is the optimal position of that material within a low conductivity domain. Figure 4 shows such an example where the objective is to most effectively distribute a limited material so as to transfer heat away from the heat source on the left to the periphery most effectively (Boichot, Luo, & Fan, 2009). The configuration evolves by positioning in regions of low temperature gradients, high thermal conductivity material, with the final result of minimizing both the gradients and maximum temperature distribution within the domain (Figure 5).

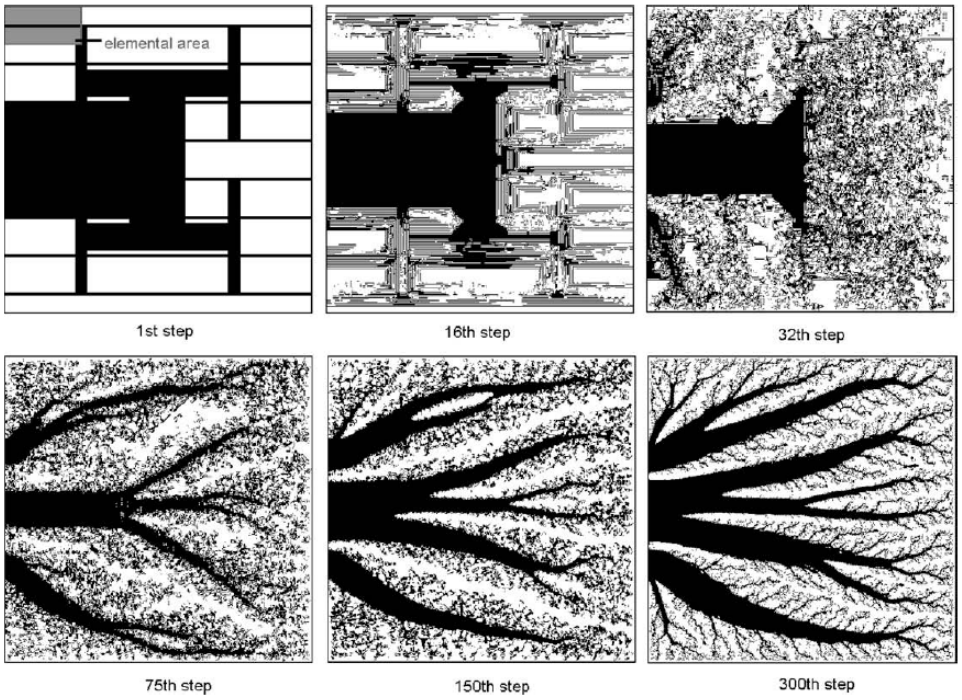

Figure 4. Evolution of the distribution of high thermal conductivity material (dark) in order to minimize thermal resistance of an area to point conduction problem (Boichot, Luo, & Fan, 2009)

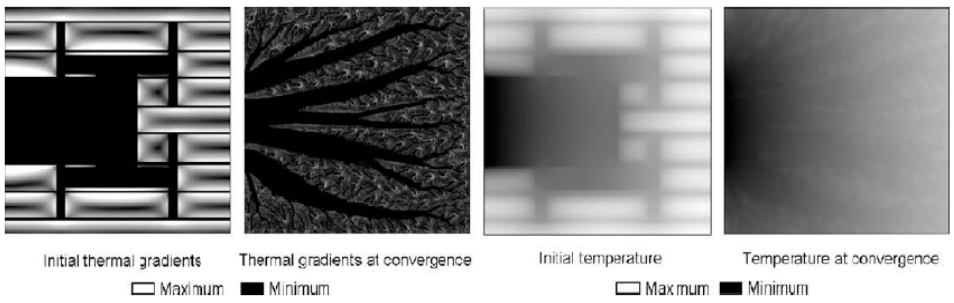

Figure 5. Thermal gradients and temperature distribution in initial and final configurations

At the heat sink level, convection transport mechanisms become dominant and once again lend itself to the general methodology employed above. In the case of air cooled finned sinks, a design that minimizes the temperature gradient with the fins, the amount of material used and the pressure loss due to the fluid flow through the passages will meet performance, cost and weight goals. Another potential application lies in heat exchanger design. Optimization methods mentioned above have been employed so as minimize overall flow resistance, which translates to reduction in pressure drop and pumping power (Bejan & Lorente, 2006). For example in Figure 6, both the shape and location of fins in a heat exchanger may lend themselves to this methodology.

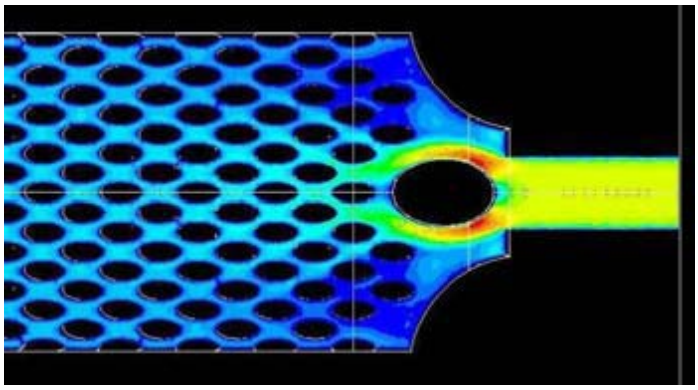

Figure 6. The temperature distribution in an elliptical pin finned heat exchanger (Kelly, 2009)

In the structural domain any load bearing structure (e.g. the enclosures, part of heat sinks) whose purpose is not particularly to serve as a thermal path, lends itself to a minimization problem of weight or volume, while constraining its stiffness or stress, thereby reducing redundant material.

The plethora of applications within the packaging arena clearly suggests that employing multi objective optimization routines in parallel with judicious material selection will further our progress in meeting cost/weight/performance goals.

Conclusion/Future Work

This report presents an initial investigation and overview of material selection, and topology optimization. Due to the variety of package topologies, a generic package topology is employed to broadly identify both, materials currently being used in the industry and that which may show promise in the future. Consistent with previous work the substrate and heat sink layers offer the greatest opportunity in meeting weight/cost/performance goals. Thermo-mechanical metrics for material selection process are identified. Advanced composite materials have show great promise in terms of both specific thermal conductivity and tailorable CTE's. A metric for cost was not identified as it is not trivial due to its rather involved nature, and will be studied in the future

Topology optimization is identified as an important way to meet goals by reducing material usage. The thermal, fluid and structural domains are all amenable to an optimization routine. Contructal and bioinspired methods are identified as new avenues to pursue due to the promise shown.

Future activities include a more rigorous, thorough investigation of the materials set, quantifying the impact of the package topology and cooling mechanism on material selection through numerical modeling. With regard to optimization, it would behoove us to look at every single component with the package and ask ourselves 'can we use an optimization routine to minimize weight, material use, pressure drop, thermal resistance and the like ?'. Further understanding of the theoretical basis for the new optimization routines so as to apply them judiciously is also warranted.

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2.4 Power Electronics Thermal System Performance and Integration

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Objectives

Electric drive systems, which include electric machines and power electronics, are a key enabling technology for advanced vehicle propulsion systems that reduce the transportation sector's petroleum dependence. To have wide application, electric drive technologies must be economical in terms of cost, weight, and size while meeting performance and reliability expectations. The push to reduce the cost, weight, and size of critical electric drive components presents significant challenges related to thermal management and system integration. The integration of thermal management technologies with electric drive components must be done at a system level instead of as an afterthought at the end of the design process. The systems approach requires a thorough understanding of the interactions between hardware design and thermal management technologies. This project will develop techniques to understand and improve the design of both hardware and thermal management into integrated systems. The end result will facilitate the integration of advanced power electronics thermal management technologies into commercially viable advanced automotive systems, including hybrid electric, plug-in hybrid electric, electric, and fuel cell vehicles.

Approach

The Power Electronics and Electric Machines (PEEM) activity in the Department of Energy (DOE) Vehicle Technologies Program (VTP) is currently developing a suite of advanced thermal cooling technologies and performance data, including single-phase and two-phase jet impingement, air cooling, low thermal resistance insulated-gate bipolar transistor (IGBT) structures, improved thermal interface materials, and direct-cooled substrates. In order to evaluate, design, and develop thermal cooling systems that enable commercially viable products, a systems approach is required. In this project we use a systems design approach focusing on two areas. First, we look at how the system is used to match performance targets to actual use. Second, we look at techniques to simultaneously optimize the hardware design and thermal management to develop more effective system designs. As the system design techniques are developed, they will be used to support research in the PEEM program area. In addition, efforts will be made to review and implement the developed systems analysis techniques with industry through partnerships and collaborative arrangements. Working with industry will provide an understanding of technology trends and practical considerations for the implementation of technologies into viable automotive systems.

This year, NREL researchers primarily focused on the development of analytical capabilities and models to support the system optimization area highlighted above. Work also included collaboration with industry and other VTP areas such as the Vehicle Systems Analysis (VSA) activity. This year's efforts focused on the following topics as summarized in more detail in the technical discussion.

1. Integrated Power Electronics Packaging and Heat Exchanger Thermal Characterization
   a. Collaborated with an industry partner (Delphi) to develop and apply a technique for characterizing power semiconductor thermal performance in terms of package configuration and heat exchanger performance.
   b. Presented and published a generalized version of the approach as applied to an innovative commercially-available package enabling cooling on each side of the package (double-sided cooling).
   c. Initiated collaboration with Oak Ridge National Laboratory (ORNL) on a current power semiconductor packaging research project.
2. Parametric Capacitor Thermal Model
   a. Continued work on developing a parametric capacitor thermal model to support research and development needs within the Advanced Power Electronics and Electric Machines (APEEM) activity.
3. Vehicle Systems Analysis (VSA) Activity Collaboration
   a. Collaborated with VSA funded activity for integrated thermal management and waste heat utilization to provide APEEM context related to thermal management.

Major Accomplishments

The key accomplishment for FY 2009 included the development of a methodology to characterize the performance of integrated power semiconductor packages and heat exchanger technologies. This included:

- NREL researchers worked closely with engineers at Delphi Corporation to develop and apply a technique for characterizing power semiconductor thermal performance in terms of package configuration and heat exchanger performance. The collaboration assisted in down-selecting heat transfer techniques for the specific Delphi package as part of their DOE funded activity to develop a high temperature inverter.
- A generalized version of the approach was demonstrated using an innovative commercially-available package to illustrate the process. Results were presented at the 2009 IEEE Vehicle Powertrain and Propulsion Conference. The combined analysis helped reduce overdesign of the thermal management system to promote improvements in cost, weight, and volume. The techniques provided a consistent method for comparing the thermal performance of alternative package configurations and cooling technologies.
- The developed techniques will support new collaboration efforts between NREL, industry, and ORNL related to cooling alternatives for new power electronics packaging technologies.

Other major accomplishments for FY09 included:

- The development of a parametric capacitor model incorporating anisotropic properties and non-uniform heat generation.
- The collaboration with the VSA activity within the Vehicle Technologies Program to provide APEEM thermal context to a VSA funded milestone titled *Integrated Vehicle Thermal Management Systems Analysis/Modeling.*

Future Direction

The future direction of the thermal systems research through FY 2010 as it relates to power electronics includes the following:

1. Integrated Power Electronics Packaging and Heat Exchanger Thermal Characterization
   a. Collaborate with ORNL on the new FY10 APEEM focus area for power electronics packaging and apply developed techniques on new packaging configurations.
   b. Compare integrated thermal performance trade-offs across multiple package configurations and heat exchanger technologies.

   c. Conduct hardware validation of integrated thermal performance for down-selected power semiconductor and thermal management technologies.
2. Parametric Capacitor Thermal Model
   a. Refine thermal model and collaborate with industry to validate and apply model. Use model for design trade-off studies of various form factors and their application in alternative packaging designs.
3. Vehicle Systems Analysis (VSA) Activity Collaboration
4. Investigate results and proposals for PEEM integrated thermal management to determine interest in further concept development with industry involvement.

Technical Discussion

Addressing goals associated with performance, cost, weight, and volume requires investigation into multiple thermal management technology pathways that involve the vehicle propulsion configuration (such as HEV or PHEV), component use (vehicle drive cycles), cooling system configuration, power electronics package configuration, and heat exchanger design as highlighted in Figure 1. A systems approach is necessary to investigate the multiple options and trade-offs associated with the items mentioned above. Analysis techniques are needed that allow researchers to quickly investigate the system-level impacts of potential technologies and evaluate trade-offs to understand the design space. For FY09 researchers focused on the two areas highlighted in Figure 1 related to evaluating the power electronics cooling system and package configuration.

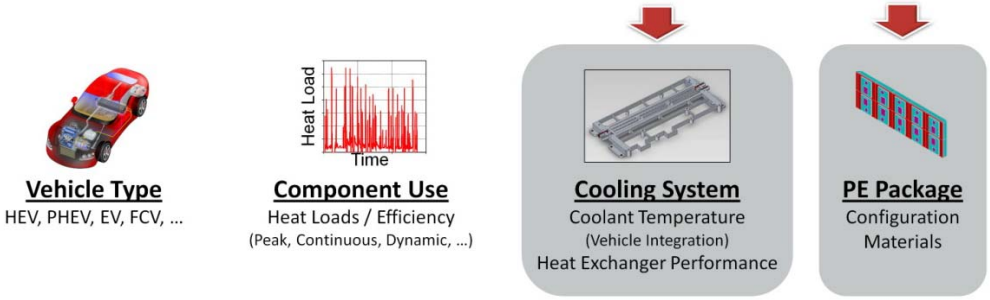

Figure 7: Power electronics systems and integration focus areas.

Integrated Power Electronics Packaging and Heat Exchanger Thermal Characterization

The primary focus through FY09 was the development and application of a method for investigating the system-level performance of power semiconductor package configurations and heat exchanger technologies. The methodology was developed and applied with an industry partner, and the generalized approach was published. An application of the technique was also initiated on a new packaging concept under development at ORNL.

Industry Collaboration for Methodology Development

NREL researchers worked closely with engineers at Delphi Corporation to develop and apply a technique for characterizing power semiconductor thermal performance in terms of package configuration and heat exchanger performance. The collaboration assisted in down-selecting from multiple heat transfer techniques for the specific Delphi package under development for the DOE APEEM industry award to design a high temperature inverter.

The developed methodology, shown in Figure 2, merged two paths to enable the evaluation of system performance and trade-offs. The first path required characterization of the heat exchanger technology in terms of heat transfer and fluid flow, and it consisted of three primary steps. Step one was the selection of the desired cooling technologies which included: standard fin geometries with liquid and air,

microchannels with liquid and air, submerged liquid jets, and alternative heat exchanger materials. Step 2 required identifying the cooling performance of the selected technologies in terms of convection coefficient (h or UA) and pressure drop (ΔP). The analysis involved the development of programs for each cooling technology based on a combination of CFD results, experimental correlations, and analytical solutions. The programs enabled sensitivity studies related to the impact of key parameters on the overall cooling performance objectives. Step three involved the conversion of the cooling performance results into a heat exchanger thermal resistance value following established heat exchanger theory (Effectiveness- NTU method)[1].

The second path also consisted of three steps, and it involved characterizing the power electronics package thermal performance. Step one required selection of the package configuration. The package configuration was primarily fixed, but alternative designs included double and single-sided cooling along with alternative heat exchanger interfaces. Step two included converting a detailed thermal finite element analysis (FEA) model into a parametric 3D thermal FEA model enabling relatively quick sensitivity studies. The primary parameter for the sensitivity study was the heat exchanger thermal resistance. Step three included the evaluation of the heat flux limitations over a range of heat exchanger thermal resistance values for a range of temperature specifications on the silicon devices and coolant inlet temperature. The results were presented as package specific curves of heat flux versus heat exchanger thermal resistance for a set temperature specification.

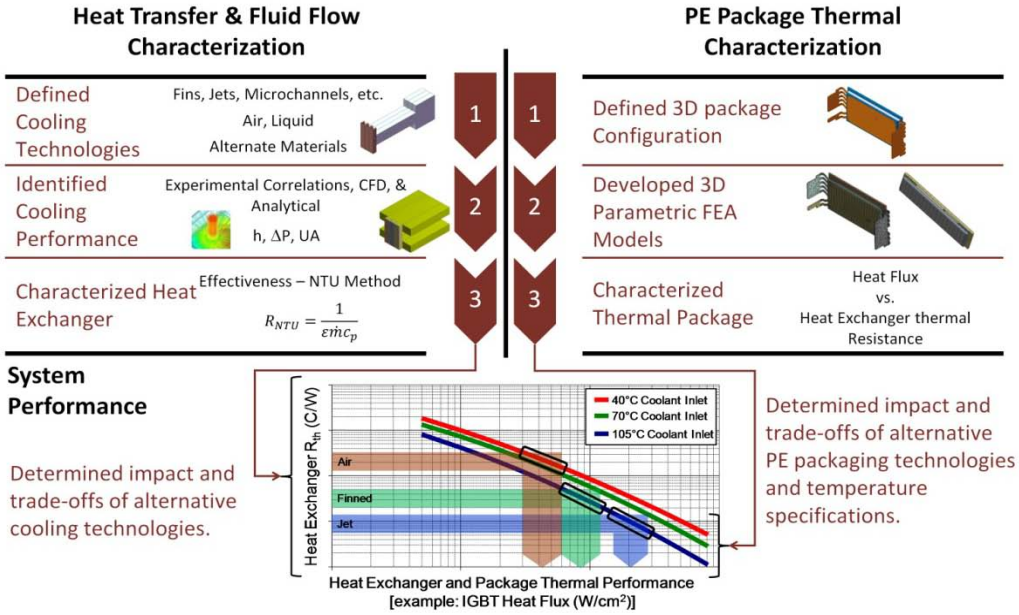

Figure 8: Power electronics thermal package system performance characterization process. Air, finned, and jet performance bands are for illustration (Images used with permission of Delphi).

The parallel paths merged to understand the integrated system performance as shown in the graph at the bottom of Figure 2. The integrated analysis allowed a comparison of the relative benefits of alternative heat exchanger designs and package configurations. The combined analysis helped to eliminate unnecessary cost, weight, and size by ensuring that one area of the system was not overdesigned. The techniques provided a consistent method for comparing the thermal performance of alternative package configurations and cooling technologies.

Application to Commercial Double-Sided Power Electronics Package

A generalized version of the approach illustrated in Figure 2 was demonstrated using an innovative commercially-available package, and the results were presented at the 2009 IEEE Vehicle Powertrain and Propulsion Conference [2]. First (as shown at the right of Figure 2), a double-sided package for a power semiconductor module was selected that consisted of one IGBT and one diode [3,4] as shown in Figure 3. The package was selected because it was used in a commercial HEV and allows cooling on both sides of the package. A double-sided package was of interest because previous analysis showed the potential benefit of double-sided cooling for power semiconductor packages [5]. The package was also of interest because it was part of an APEEM benchmarking effort conducted by ORNL [6]. Figure 3c shows an exploded view of the layers, and additional information related to the package is available in [2] that was obtained from ORNL through its benchmarking work and from published reports [3,4].

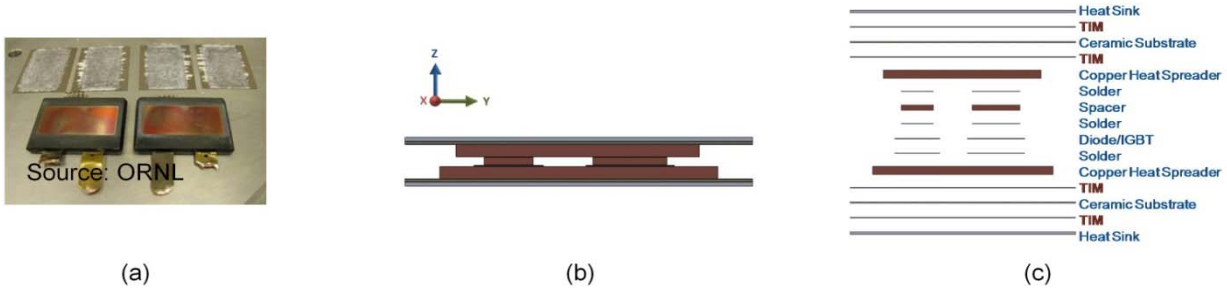

Figure 9: Selected double-sided package. (a) Actual hardware (Image curtesy of ORNL); (b) 3D CAD model for thermal FEA model; (c) Exploded layers (multiple thermal interface material (TIM) layers are highlighted).

To illustrate the impact of alternative package configurations, a range of thermal interface material (TIM) thermal resistance values were included in the analysis. A baseline TIM material with a thermal resistance of 66.7 mm^2-K/W was selected from information generated as part of NREL's characterization of TIM thermal performance [7]. To see the impact of improvements to the thermal interfaces, a 5X and 10X improvement in the interface thermal resistances (13.3 mm^2-K/W and 6.7 mm^2-K/W) were also considered.

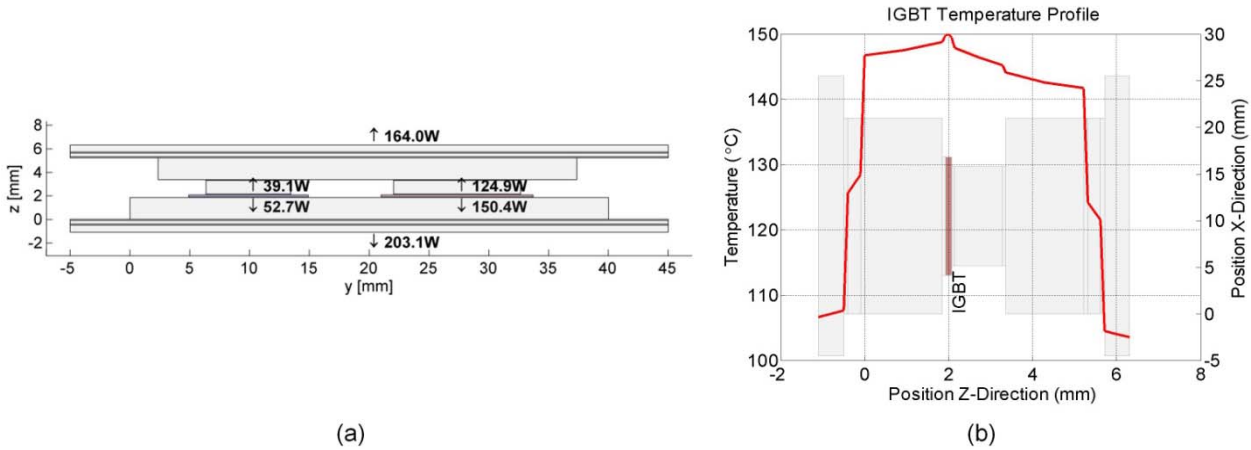

Figure 10: Results of single test condition (coolant temperature 70°C, IGBT junction temperature 150°C, net effective heat exchanger thermal resistance applied to each side 0.10 K/W, IGBT heat flux 170.7 W/cm^2, and IGBT to diode loss ratio 3:1). (a) Heat flow paths from ANSYS FEA model; (b) Straight line IGBT temperature profile through package to the heat sink base from ANSYS FEA model. The z axes scale is magnified to show detail.

The second step in the package characterization (shown in Figure 2) included developing a 3D parametric FEA thermal model. The CAD software "SolidWorks" was used to construct a three-dimensional solid model of the package. The geometry was then imported into the software "ANSYS Workbench" for thermal analysis. For this analysis, a constant IGBT to diode loss ratio of 3:1 was used (see Figure 4a). The IGBT and diode heat loads were applied with volumetric heat generation for each device. A convective heat transfer coefficient was applied to the top and bottom surfaces in Figure 3b to generate the desired net heat exchanger thermal resistance at a specified fluid temperature. To determine the maximum allowable IGBT heat flux for a given heat exchanger thermal resistance value, an iterative approach was used within "ANSYS Workbench DesignXplorer." The volumetric heat load of the IGBT was determined based on the targeted maximum temperature limit of the IGBT device. This temperature limit is referred to as the maximum junction temperature (Tj) throughout this paper. Figure 4 illustrates a sample solution for one design point. The large temperature changes in Figure 4b are a result of the TIM layers.

Once the maximum allowable heat load was determined, the process was repeated for another heat exchanger boundary condition as listed in step 3 of Figure 2. Two junction temperature limits of 150°C and 175°C were used for the analysis. In addition, two coolant temperatures were used (70°C and 105°C). The 70°C coolant temperature was based on current coolant loops used in HEV applications, and 105°C was based on the upper temperature limit target from DOE's APEEM R&D team [8].
The parametric ability of the FEA thermal model allowed for sensitivity studies associated with multiple aspects of the package design and not just the heat exchanger performance and temperature specifications. For this demonstration, the package performance curves were also generated using different material properties for the TIM. The results of the sensitivity study and the package thermal performance curves are shown in Figure 5.

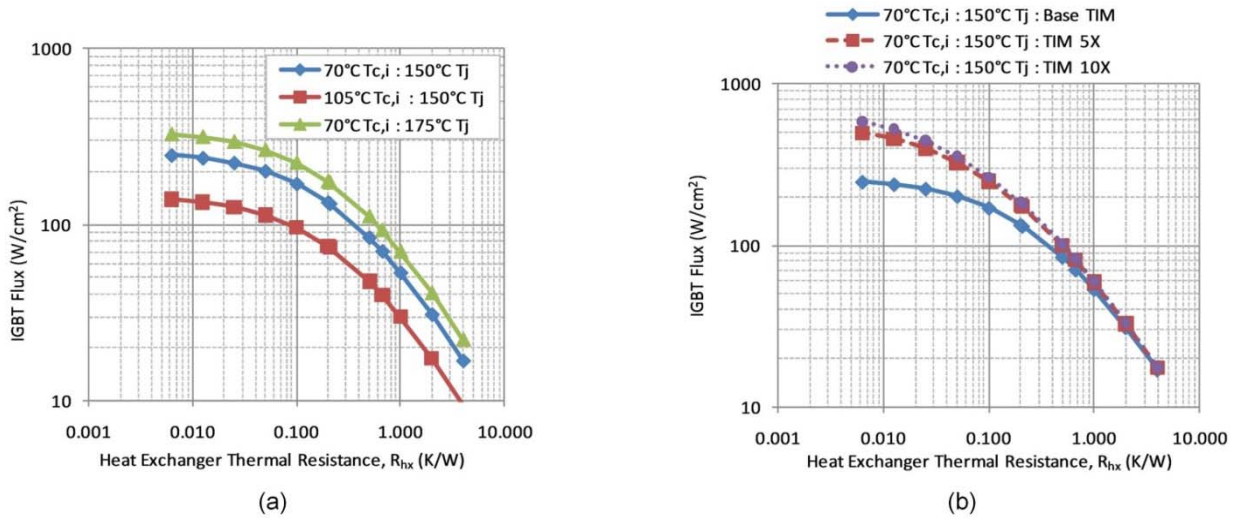

Figure 11: Package specific thermal performance curves showing IGBT heat flux vs. heat exchanger thermal resistance. (a) Thermal performance curves as a function of alternative temperature specifications; (b) Thermal performance curves as a function of alternative package configurations or TIM properties.

The first step in the characterization of the heat exchanger technologies was the selection of the cooling technologies. The first selected thermal management technique approximates the actual finned heat exchanger used in the 2008 Lexus LS 600H Hybrid Synergy Drive System (Figure 6a). Additional details associated with key fin parameters and fluid flow assumptions are highlighted in the published report [2]. The coolant fluid was assumed to be a 50/50 (by mass) mix of water ethylene glycol with properties based on [9]. The second cooling technology used submerged liquid jets (Figure 6b). The submerged liquid jet

technology was selected to illustrate the use of experimental correlations, while the fin heat exchanger was selected to illustrate the application of computational fluid dynamics (CFD) results and analytical solutions. Each of these methods, with the associated approach and assumptions, are described in detail in the published report [2]. Tables 1 and 2 list the results, in terms of heat exchanger thermal resistance (R_{hx}) using the effectiveness-NTU heat exchanger analysis method, for the fin and submerged jet configurations.

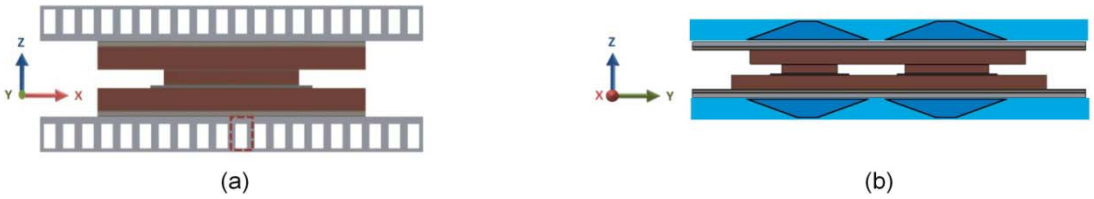

Figure 12: Selected sample cooling technologies. (a) Fin with liquid coolant; (b) Submerged liquid jet.

Table 7: Fin heat exchanger thermal performance comparison between CFD results and analytical solution.

Parameter	CFD Value (CFX)	Analytical Value
System flow (L/min) [3,4]	12	12
$T_{c,i}$ (°C)	70	70
h (W/m^2-K)	1877	1241
∆P (Pa)	267	271
$R_{hx} = \frac{1}{\varepsilon \dot{m} c_p}$ (K/W)	0.11	0.16

Table 8: Submerged liquid jet heat exchanger thermal performance comparison between two effective area extremes.

	Two Jets per Side		Two Jets per Side 2X Area Enhancement	
System flow (L/min)	24	24	24	24
$T_{c,i}$ (°C)	70	105	70	105
Flow per Jet (L/min)	0.5	0.5	0.5	0.5
h (W/m^2-K)	30000	37000	30000	37000
Cooled Area (m^2)	2.53E-04	2.53E-04	5.07E-04	5.07E-04
$R_{hx} = \frac{1}{\varepsilon \dot{m} c_p}$ (K/W)	0.140	0.115	0.074	0.062

Note: It should be noted that these results are approximations due to the large variation in the local heat transfer coefficient of jets over a target surface. The average heat transfer coefficient over the full target surface depends on the size of the cooled surface.

Since the selected package is part of an existing HEV application, the estimated system performance from this analysis was compared against publicly available information [3,4]. For this comparison, the total thermal resistance (R_{tot}) from junction to fluid inlet was calculated using Equation 1 with the fluid temperature ($T_{c,i}$) at 70°C, junction temperature (T_j) at 150°C, and q_{tot} set to the combined IGBT and diode heat load. The total thermal resistance using the estimated finned heat exchanger thermal resistance of 0.11 K/W is 0.219 K/W. For comparison, the published maximum thermal resistance of the package is 0.203 K/W [3,4]. The difference is within 8% of the published value in [3,4]. Figure 7a shows how the total thermal resistance varies with the heat exchanger thermal resistance.

$$R_{tot} = \frac{T_j - T_{c,i}}{q_{tot}}, \quad (1)$$

With the generated package performance curves and the completed heat exchanger analysis, the final step combines the two results to the look at the total system performance as shown in the general process diagram of Figure 2. This was done by overlaying the heat exchanger performance in terms of its effectiveness-NTU thermal resistance on top of the generated package thermal performance curves, as shown in Figure 7b. The system performance graph allowed a comparison of the combined system and an understanding of how improvements in the heat exchanger performance affect the system performance.

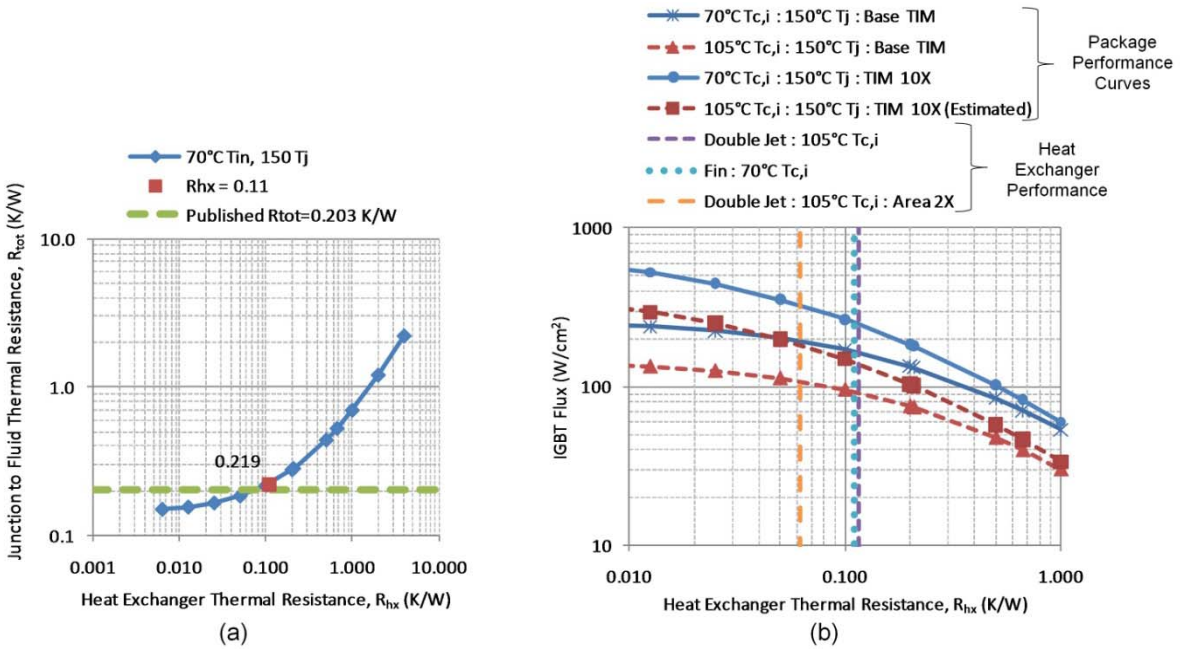

Figure 13: (a) Total thermal resistance comparison; (b) System performance showing package thermal performance curves with estimated heat exchanger performance.

Figure 7b highlights four package performance curves. The first is the baseline system with the base TIM, inlet coolant temperature of 70°C, and a maximum junction temperature of 150°C (solid line with star marker). The second curve is the same package with an inlet coolant temperature of 105°C (dashed line with triangle marker). The third curve is the same as the baseline system, except the TIM thermal resistance is reduced by a factor of 10 (solid line circle marker). Finally, the fourth performance curve included the 10X improved thermal interface material and an inlet coolant temperature of 105°C (dashed line with square marker). The heat exchanger performance is shown by the vertical lines. Three representative heat exchangers are shown. The first is the double jet at the lower limit of the effective heat exchanger area (short dashed line). As can be seen, its thermal performance is close to the baseline finned heat exchanger at a 70°C inlet coolant temperature (dotted line). Although not shown, the thermal resistance of the finned heat exchanger at 105°C is similar. Finally, the third heat exchanger shows the potential of a two times improvement in the heat exchanger area for the double jet system (long dashed line).

In the case of the baseline system, one can see that the benefit of increasing the heat exchanger performance beyond the fin design is of less value because of the limitation related to the package thermal performance. This is because of the relative leveling off of the curve at lower R_{hx} values as compared to alternative packages with improved TIM properties. Figure 7b also shows the impact of increasing the coolant temperature and reducing the package thermal resistance. While the system at 70°C coolant is capable of operating at about 165 W/cm^2, this is decreased to 93 W/cm^2 when forced to operate with a coolant temperature of 105°C (a drop of 44%). This assumes similar performance for the finned heat

exchanger at 70°C and 105°C. When an improved heat exchanger (represented by the jet with the 2X effective area) is applied to the base package with a coolant temperature of 105°C the overall performance increases by 17% to 109 W/cm^2. As shown in Figure 7b, the package with the improved TIM is able to take advantage of a higher performance heat exchanger. Assuming similar fin heat exchanger performance at 105°C the 10X improved package is capable of 142 W/cm^2, which is only slightly less than the base package at a 70°C coolant temperature. When the same improved jet heat exchanger is applied, the performance increases 30% to 184 W/cm^2.

The results highlight the importance of matching the heat exchanger thermal performance (R_{hx}) with the package thermal performance. The optimal heat transfer mechanism is highly dependent on the package configuration, which leads to the need to evaluate the package and heat exchanger as an integrated system. The combined analysis helps reduce overdesign of the thermal management system to promote improvements in cost, weight, and volume. The work described in this paper illustrates the need for integrated system analysis on new innovative power semiconductor package configurations and proposes techniques for understanding the trade-offs associated with an integrated system.

Application to ORNL Package

The developed process was initiated, in collaboration with Oak Ridge National Laboratory (ORNL), for a power electronics package configuration under development at ORNL [10]. Two configurations setup for analysis are shown in Figures 8a and 8b. The overall objective of the packaging concept is to reduce the size and weight of the power electronics package through elimination of the conventional heat exchanger. The concept directly cools the insulating substrate of the power electronics package by including cooling channels in the substrate [10]. Parametric 3D FEA thermal models were developed for each configuration to match the geometry and heat load conditions provided by ORNL. Each package consists of six silicon devices of the same size (7.8 mm x 7.8 mm) and heat load (37 W per device). The heat load was applied as a volumetric heat load for each device. ORNL provided heat exchanger performance data for each configuration broken up into three sections as shown in Figure 8c. The information was used to develop an overall heat exchanger thermal resistance value to apply to the heat exchanger surfaces listed in Figures 8a and 8b.

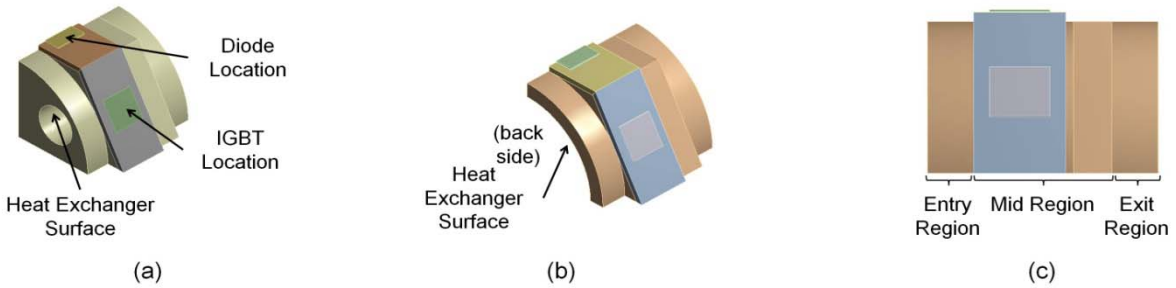

Figure 14: (a) ¼ section of 4 hole package configuration; (b) ¼ section of annulus package configuration; (c) Sections for provided heat exchanger performance data.

The results of the developed model are listed in Table 3 and compared against simulated temperature data provided by ORNL. The generated peak temperature results from the developed model are higher, but they are within 3.6% of the results provided by ORNL. One reason for the increase in temperature is that the developed model includes solder layers, while the data provided by ORNL was obtained from models that excluded the solder layer. This would account for part of the difference. With the relative agreement between model results, the next step will evaluate the impact of various design parameters associated with the heat transfer performance. The primary objective is to identify design trade-offs related to package thermal performance. To accomplish these goals the size of the IGBT devices will be increased to

represent the actual IGBT size for the design, and the loss ratio between the IGBT and diode will be adjusted to represent a typical operating condition (3:1). The 3:1 loss ratio will make the analysis consistent with developed packaging thermal characterization process that has been applied to other systems.

Table 9: ORNL package configuration peak temperature model results.

4 Hole Design	Developed Package Model	ORNL Comparison Data	Percent Difference
Diode Peak Temperature (°C)	153.3	148	3.6%
IGBT Peak Temperature (°C)	146.3	141.6	3.3%
Annulus Design	**Developed Package Model**	**ORNL Comparison Data**	**Percent Difference**
Diode Peak Temperature (°C)	149	144	3.5%
IGBT Peak Temperature (°C)	149	144	3.5%

PE System Thermal Management

Work was also done to extend beyond semiconductor devices to look at other aspects related to power electronic system cooling and integration. This work extended to collaboration with the NREL's VSA activity in relation to integrated vehicle thermal management involving the power electronics and electric machines. A capacitor thermal model was also developed to help address the broader power electronic thermal management challenges and support other research and development activities within the APEEM activity.

VSA Collaboration for Integrated Thermal Management

To reduce the cost of APEEM systems there is a strong desire to integrate the APEEM thermal management system with other thermal management systems of the vehicle. A current focus is the integration of the APEEM and ICE thermal management systems [8]. The assumptions associated with coolant temperature have a dramatic impact on the research goals, technical targets, and the ultimate direction of technology development. For this reason, there is a need to take a higher level vehicle system view of how cooling systems are integrated into an overall vehicle thermal management strategy. The VSA activity under the Vehicle Technologies Program was funded in FY09 to investigate applications for vehicle waste heat utilization and integrated thermal management. Part of the work investigated the potential for integrating the PEEM thermal management system with the ICE coolant loop and other vehicle thermal management systems (Figure 9). The analysis utilized a set of existing vehicle configurations and in-use drive cycles previously used by the APEEM activity when looking at the potential impacts on the PEEM system when moving from HEV applications to PHEV applications [11]. Thermal and fluid system models were developed within Aspen Plus and MATLAB to evaluate alternative integrated thermal management arrangements and the heat exchanger sizing impacts. The work was submitted as a DOE milestone and is under review for publication.

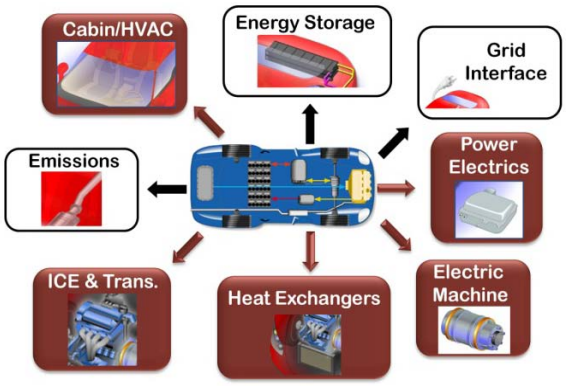

Figure 15: Integrated vehicle thermal management for ICE, PEEM, and heating ventilation and air conditioning systems (HVAC).

Of interest to the APEEM activity was work performed to evaluate the integration potential of the PEEM system with other vehicle systems as shown in Figure 9. The evaluation included both high and low temperature systems. The integration potential was based on coolant temperature requirement compatibility and misalignment in the peak heat loads over in-use drive cycles. The misalignment of the heat loads was determined by computing a running average of the merged or integrated heat load over expanding time windows. The resulting integrated heat load was compared against the simple addition of the individual component transient and continuous heat loads. In some applications the simple addition of the transient and continuous heat loads overestimates the heat loads on the thermal management system because of misalignment in the transient heating of the individual systems. The magnitude of the heat load reduction depends on the vehicle configuration, the drive profile, the selected systems for integration, and the operation strategy of the vehicle and systems.

Capacitor Thermal Model

The DC link capacitor module is approximately 20-31% of the inverter volume and weight in some current hybrid designs [6,12]. The thermal performance of capacitors and their thermal management system have a significant impact on size and weight both through ripple current ratings and packaging design. A capacitor thermal model was developed to begin addressing capacitor thermal design and capacitor system thermal management. To accurately approximate the thermal performance of capacitors, this model incorporates anisotropic material properties and non-uniform heat generation. The model is parametric for increased flexibility and to allow exploration of the design space. The model will be applied to perform design trade-off studies of various form factors and their application in alternative packaging designs.

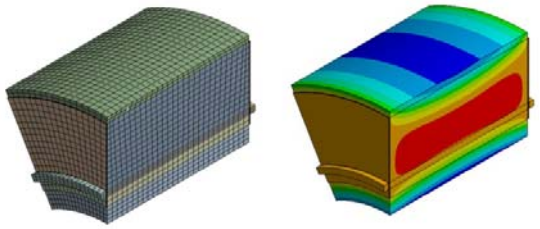

Figure 16: Parametric capacitor thermal model example results using anisotropic properties and non-uniform heat generation in the windings. Thirty degrees of a large annular capacitor form factor shown.

Conclusion

The objective of the thermal systems task is to facilitate the integration of advanced power electronic thermal management technologies into commercially viable advanced automotive systems. The design of a viable system requires understanding how the power electronics are used, how the environment in which they operate impacts thermal management, and how power semiconductor packaging and cooling impacts performance. In FY 2009 we worked to develop methodologies and capabilities to improve the selection of power electronics packages and associated thermal management technologies. The work primarily focused on the packaging of the power semiconductor devices, but efforts were also made to support other investigations related to capacitor thermal management and integrated vehicle thermal management incorporating power electronics and electric machines.

NREL researchers worked closely with engineers at Delphi Corporation to develop and apply a technique for characterizing power semiconductor thermal performance in terms of package configuration and heat exchanger performance. The collaboration assisted in down-selecting heat transfer techniques for the specific Delphi package as part of their DOE funded activity to develop a high temperature inverter.

A generalized version of the approach was demonstrated using an innovative commercially-available package to illustrate the process. Results were presented at the 2009 IEEE Vehicle Powertrain and Propulsion Conference. The combined analysis helps ensure that one area of the system is not overdesigned, leading to unnecessary cost, weight, and size. The techniques provide a consistent method for comparing the thermal performance of alternative package configurations and cooling technologies. The developed techniques will support new collaboration efforts between NREL, industry, and ORNL related to cooling alternatives for new power electronics packaging technologies.

Other major accomplishments for FY09 included the development of a parametric capacitor thermal model and collaboration with the VSA activity within the Vehicle Technologies Program. The collaboration work with the VSA activity highlighted potential concepts for integrating the PEEM cooling with other vehicle systems, which could be the subject of future work. The development of a parametric capacitor thermal model with anisotropic properties and non-uniform heat generation will enable design trade-off studies of various capacitor form factors and their application in alternative packaging designs.

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2.5 Research and Development of Air Cooling Technology for Power Electronics Thermal Control

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Objectives

- The overall objective of the thermal control activities is to develop advanced technologies and effective thermal control systems to meet DOE FreedomCAR program goals. These goals address key requirements for automotive power electronics. Those are target values for volumes, cost, and weight of various subcomponents. The objective of the present research activity is to assess the potential for reducing the cost and complexity of cooling systems for power electronics using air as the cooling medium. This study aims to quantify the relative merits of the use of air for cooling power electronic devices to achieve high-heat flux removal rates under steady-state and transient conditions, and assess the viability of air cooling from a thermal systems' perspective.

Approach

- Assess hardware options that may be available in the industry for varied air-cooling devices.
- Conduct system level analyses to identify areas of critical needs.
- Conduct computational analyses of fluid flow and heat transfer for promising devices and geometries.
- Fabricate and test prototype test articles and automotive-scale systems to validate design methods.
- Arrive at recommendations for future activities.

Major Accomplishments

- Characterized the potential for cooling with micro-channel geometries various fluids
- Developed simplified user-friendly software for quick assessment for various parameters
- Verified performance with computational fluid dynamic (CFD) analyses
- Identified air cooling heat exchanger geometries viable for use with automobiles
- Fabricated and tested two test articles with excellent agreement in performance between predictions and test results.
- Came up with an innovative heat sink design that doubles the heat-transfer area while cutting the pressure loss by one half, and generated an invention report which is currently in process at NREL legal offices.
- Fabricated a compact test article (air-cooled heat sink) capable of accommodating power devices and rejecting heat at a rate of 4.5 kW at a nominal heat sink plate temperate of 125^{o}C.

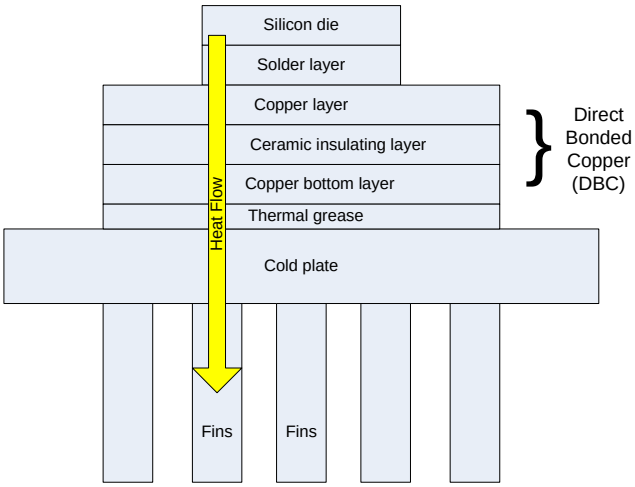
Future Direction

- Fabricate and test an automotive-scale air-cooled heat sink cooling an actual inverter (in collaboration with a supplier)

Technical Discussion

Current power-electronic modules are cooled with a dedicated water/glycol coolant loop operating at a nominal 70°C that eventually rejects heat to the ambient air (at 30°C) using a radiator. An alternative technical pathway involves eliminating the separate cooling loop and/or using coolants at a high temperature (105°C). Both these approaches require advanced cooling methods to achieve high heat fluxes (of the order of 200 W/cm^2) from the electronic chips.

Figure 1 shows a schematic cross-sectional view of an electronic die-mounted on a cold plate with the heat being removed by a coolant supplied to the bottom of the cold plate. Various layers that impede the heat flow from the die to the cooling fluid are indicated. A major contributor to the overall thermal resistance is the thermal grease. However, thermal grease is necessary to eliminate interlayer thermal stresses that can result from differential thermal expansion between the layers.



The next higher resistance usually comes from the heat sink rejecting heat to the cooling fluid. For cooling with air, ambient air is assumed to be available at a nominal 30°C (as for all the vehicle cooling strategies*). Use of ambient air increases the temperature-driving potential available to reject heat. Air, as the cooling medium, is benign, nontoxic, and readily available when compared to many other (heat-transfer) fluids. Airflow can be modulated in a transient manner to suit the needs the system continually.

Figure 1 Heat flux path and the various intervening layers

The use of air on both sides of the silicon switches remains an attractive option. Use of air for cooling has many advantages. Air remains the ultimate heat sink for all forms of heat rejection from an automobile. All the heat to be rejected, either directly or through the use of an intermediate coolant loop must end up in air. Direct use of air can eliminate many components of the cooling loop and the necessity for carrying a secondary coolant. Since the ambient air is at 30°C, air can be used to cool other components of the system, such as the capacitors. Capacitors with a central cavity are highly amenable to air cooling without exceeding limiting operating temperatures within their core.
*

Air cooling has many drawbacks as well. Air remains a poor heat transfer medium, with low thermal conductivity and low density. A fan or a blower must direct the air stream to the required hot spots, thus

* Use of under hood air or cabin air has been suggested for electronic cooling. Under hood air can reach temperatures of up to 140°C and thus is not suitable for cooling electronics at 125°C. Cabin air may be used in case the cabin needs heating. In case the cabin air needs to be cooled, the cooling load for the cabin will increase if it is used for cooling electronics. Ambient air makes the best medium for cooling power electronics.

requiring additional parasitic power loads. The coefficient of performance for such a system tends to be low.

Cooling with air may or may not meet requirements for current generation silicon-based devices that the temperatures at the chip be limited to 125^{o}C maximum. Trench devices offer a higher maximum of 150^{o}C. Future progress in solid-state switching devices, however, is expected to allow higher temperatures at the chip, with the trench IGBTs (Isolated Gated Bipolar Transistors) operating at 175°C, and Si-C devices operating at even higher temperatures. With these higher temperatures, air cooling is expected to become more practical.

To address many thermal control issues, NREL has undertaken a number of distinct areas of research and development. Multiple avenues of this research are expected to result in significant advancement in thermal control of power electronics with a high degree of flexibility in design to meet the targeted goals and objectives of the FreedomCAR initiative. Progress made toward evaluating air cooling as a viable option for power electronic components in FY2009 under the FreedomCAR Program follow.

Initial assessment for air cooling focuses on a simple heat transfer that occurs on a single chip. We assume a chip heat-rejection area of nominal 1 cm^2 with the chip generating a heat load of 200 W. This level of heat flux is an aggressive goal when compared today's devices operating at less than 100 W/cm^2. Air at ambient pressure and a temperature of 30^{o}C is used to remove the heat. The air approach temperature is fixed at 40^{o}C below that of the target hot surface (a value typical for airflow applications). The fan operates with an efficiency of 56 %, (a value perhaps high for today's available fans).

We find that the airflow requirement per chip is about 3.6 g/s (or 2 ACFM—actual cubic feet per minute). The required UA product (the product of the heat-transfer coefficient and the available area for heat transfer, normally termed the UA product) is 3.15 W/K. This translates to a thermal resistance of 0.32 K/W.

Typical industrial airflow applications nominally achieve a heat transfer coefficient of about 40 W/m^{2}K. If we use this value, the required area is about 800 square centimeters. That is, the heat generated in the chip area of nominal 1 cm^2 must be spread out over an area larger by a factor of 800. Normally this is accomplished through the use of fins or other means, at a certain loss of driving temperature potential. We find, however, that nominal air-side heat transfer coefficients fall well below the needs to accomplish the task at hand. To enhance the heat transfer coefficient and provide large area enhancements, we looked into micro-channel geometries.

Micro-channels have been shown to yield very high heat removal capability in many studies. Their attractiveness comes from being able to provide large surface areas in a relatively small volume. To maintain a low pressure drop through the micro-passages, fluid flow is limited to a laminar flow regime. Laminar flow heat transfer coefficients vary inversely with the passage hydraulic diameter. Maintaining low passage widths result in high heat transfer coefficients as well. Figure 2 shows a simplified two-node model for heat transfer in finned air-cooled heat sink. The sink is assumed to be 10 mm wide, 10 mm tall, and 10 mm in length. Two nodes are assumed to be in the center of the fin and in the center of the air passage. Air passage width is assumed to be the same as the fin thickness. Fins are assumed to be made of copper. Thermal resistances of the sink are plotted as functions of the fin thickness. For laminar flow, the Nusselt number remains constant. Therefore, the air-side heat transfer coefficient is only a function of the air passage width, and it increases monotonically with decreasing width. Heat transfer area also increases with decreasing fin spacing. At low fin spacing, air-side decreases dramatically. Increasing passage spacing increases air-side resistance. The fin resistance increases monotonically with decreasing fin thickness. The sum of the two resistances attains a minimum value of about 0.25 K/W at a fin thickness of

about 0.1 mm. This value, while derived from very simple approximation, represents a minimum thermal resistance we can expect from micro-finned air-cooled heat sink.

To achieve a heat flux of 200W from this heat sink, one would require a temperature drop of 50°C from the hot plate to the air stream. If the temperature of the heating surface is fixed at 150°C, the air temperature cannot exceed 100°C. Minimum air flow is dictated by this constraint.

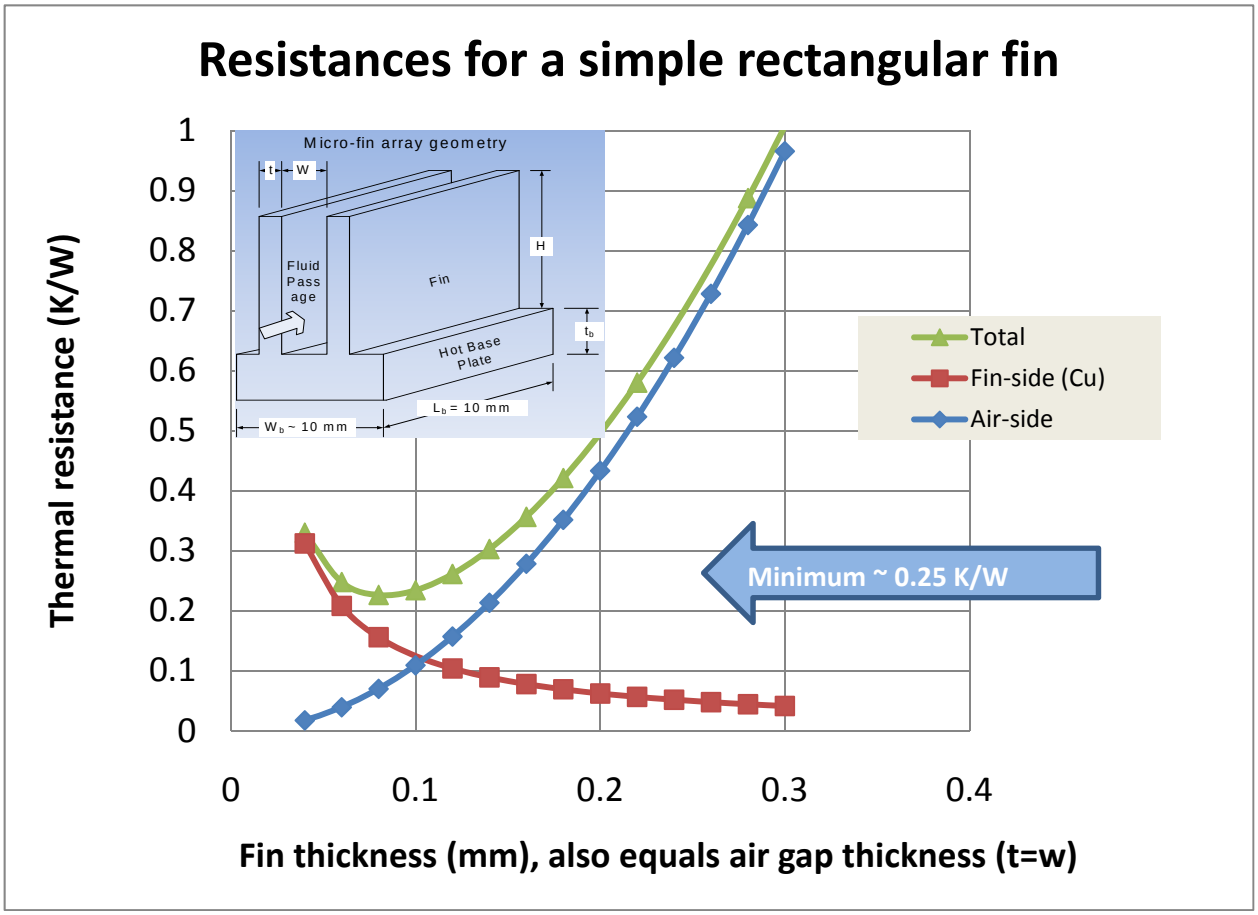


Figure 2 Simplified representation of the air-side and fin-side thermal resistances for a 1 cm cube copper heat sink.

We note air cooled heat sinks are viable for removing heat fluxes of up to 200 W/cm^2 as per the program goals. Since the pressure drop through the sink increases inversely proportional to the fin spacing, larger fin spacing is preferred if it can be accommodated.

Comparison of Air And Liquid Cooling

For automotive applications, we have compared air and liquid cooling approaches in our previous report. While such comparisons have been reported for other applications, the requirements for automotive applications are unique and differ considerably from other applications.

To carry out a direct comparison of the requirements of liquid vs. air cooling, we assumed an overall heat removal requirement of 3 kW from the power electronic components for an HEV. Additional assumptions are also made, as listed in Table 1. The approach temperatures, defined as the difference between the

coolant outlet temperature and the maximum surface temperature, are typical values for air and liquid cooling.

For this comparison, we used a liquid cooling temperature of 105°C to be consistent with the FreedomCAR goals. Air ducts were made of polyethylene. Liquid hoses were standard automotive grade components. In both cases we used micro-finned heat exchangers mounted on the base plate of the electronic devices. Pump and fan efficiencies were taken to be 0.7, a value high for today's fans. Detailed breakdowns of the components for each system allowed us to calculate various component masses, volumes, required parasitic power, and cost [Bharathan and Kelly, 2008]. Table 2 summarizes the results of this analysis.

Table 1 Assumption for Comparing Air and Liquid Cooling

Quantity	Air Cooling	Liquid Cooling
Inlet temperature (°C)	30	105
Approach temperature (°C)	40	5
Mass flow rate (g/s)	54	50
Volume flow rate	94 (SCFM)	0.8 (gpm)
Configuration	Open loop	Closed loop

Mass of the system is a key variable for automotive application. We find that the air-cooling system compares very favorably with the liquid-cooling system. Air-cooling system mass turned out to be one-half of that for the liquid cooling system. However, the air system is bulkier, occupying twice as much volume. Majority of the volume is related to the ducting necessary for handling air. Excess volumes are difficult to accommodate, especially in the cramped quarters under the hood of an automobile.

The parasitic power for the air-cooling system is close to three times that for the liquid-cooling system, reflecting its lower coefficient of performance (COP). Parasitic power is the power it takes to run the cooling system. It is an important parameter in that parasitic power adds load to the ICE and impacts overall fuel economy of the vehicle.

Costs were calculated based on the raw material cost for the components and multiplying that cost by two to account for fabrication in large quantities.

Table 2 A Quantitative and Qualitative Comparison of Air-Cooling versus Liquid-Cooling Options

Quantity	Air Cooling	Liquid Cooling
System mass (kg)	1.4	3.8
Volume (cc)	7000	3800
Parasitic power (W)	80	28
Relative component and system fabricated costs ($)	48	78

The impact of parasitic power or the excess mass on the vehicle's gasoline usage, in terms of miles per gallon (mpg), is very small for both systems. Our evaluation showed that air-cooling systems may have

additional benefits that are less tangible. These include a decreased number of components, increased reliability, ease of maintenance, and simplicity of design and installation. Based on these comparisons, we find that air cooling provides a viable option for heat removal from power electronic systems in automotive systems.

At present, cooling of the heat-generating chips from only one side is considered. With air cooling, the potential for cooling both sides of the chips will allow larger cooling loads and more compact and economic designs.

Experimental efforts

Efforts to fabricate and test prototype micro-fin air-cooled heat exchangers at NREL have been completed. Figure 3 shows a photograph of a test article fabricated at NREL for the tests. Thermal and flow performance data were obtained over a range of air flow rates in the laboratory. This test article was designed to cool a single chip of nominal 1-square centimeter area, generating fluxes up to 200 W/cm^2.

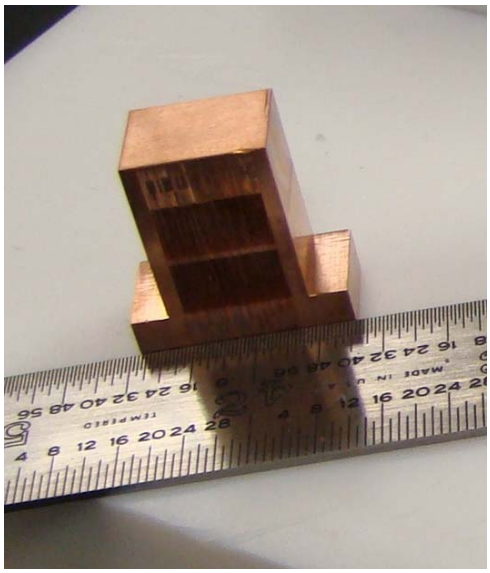


Figure 3 Photograph of the air-cooled heat sink

Overall dimensions are indicated with a ruler placed adjacent to the air cooler in this picture. Experimental data on the obtained heat fluxes are shown in Figure 4. In this figure, the test article base temperature (in degrees Celsius) is plotted as a function of the heat flux imposed at the base of the heat sink. We covered a range of fluxes up to 180 W/cm^2. Data for three different air flow rates are shown. At each airflow, the base temperature increases linearly with increasing imposed heat flux, as expected. Higher air flow rates yield lower base plate temperature. On account of the different layers on the chip, the chip temperature would be slightly higher than the base temperature indicated in this figure.

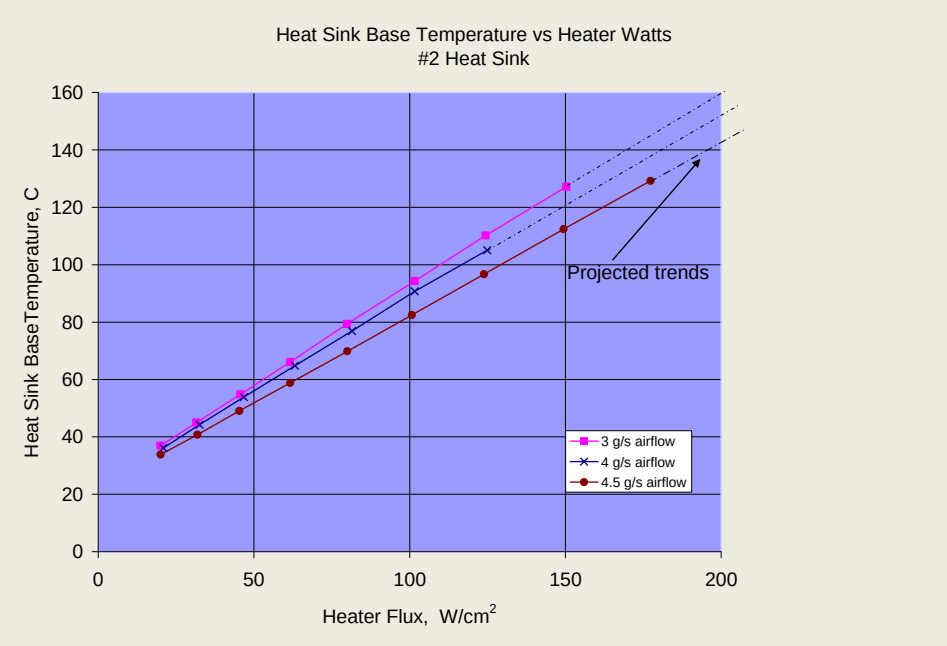


Figure 4 Variation of base plate temperature as a function of heat flux at varied air flow rates

A second heat sink fabricated at the Illinois Institute of Technology is shown in Figure 5. Copper plates were etched to form the fins and spacers as shown in the photograph. Thermal tests revealed that this test article also behaved as predicted. Pressure loss data are discussed next.

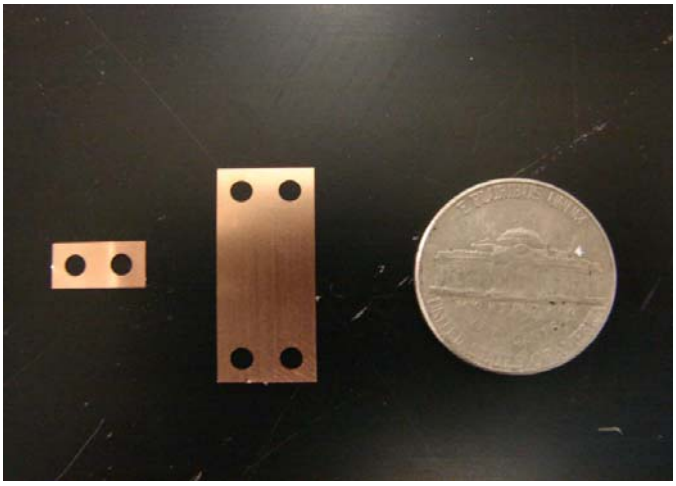


Figure 5 Photograph of the spacer and fin for the test article fabricated at Illinois Institute of Technology

Pressure loss measurements for both these heat sinks were found to agree with model predictions quite well, as shown in Figure 6.

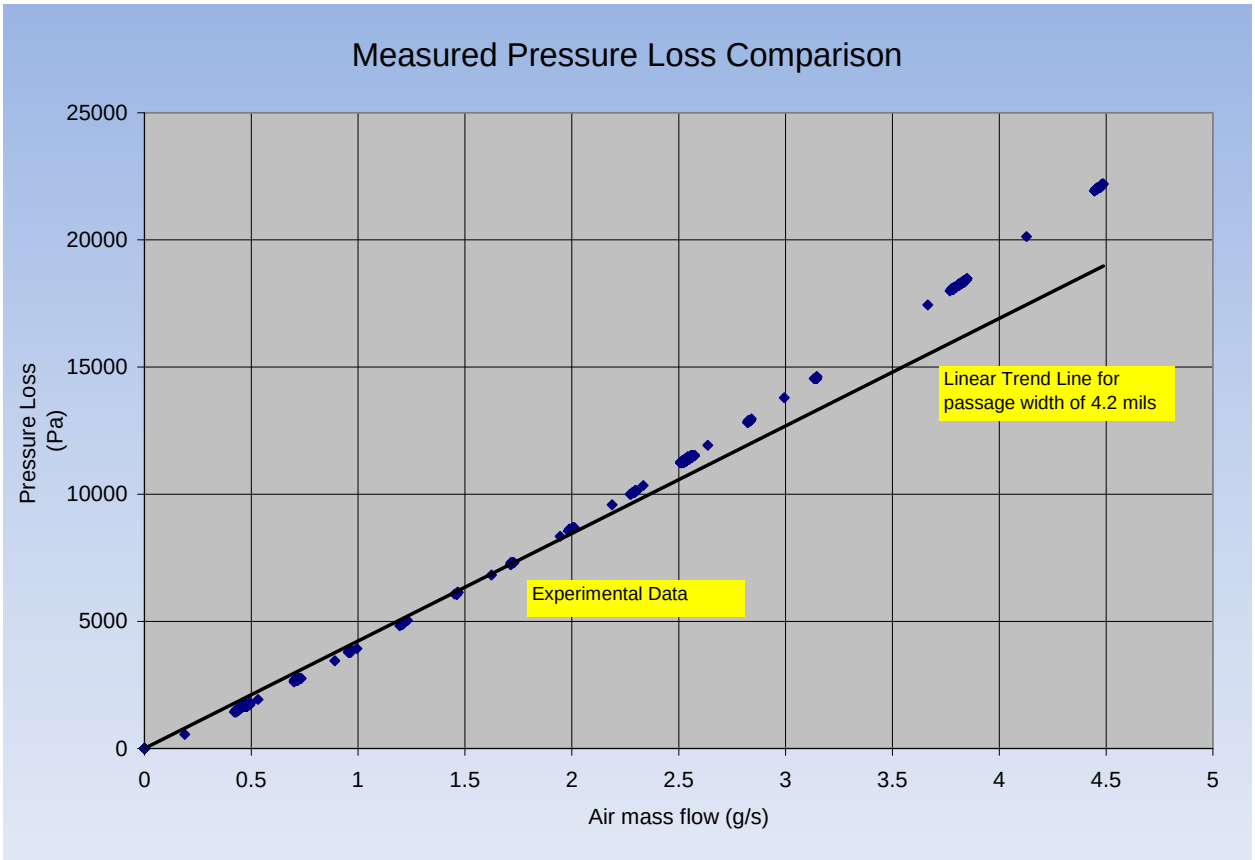


Figure 6 Measured pressure loss for the heat sink versus air mass flow rate; comparison to predicted values are also shown.

Our experimental data validated that we can confidently design air-cooled heat sinks with a good certainty of performance for cooling power electronics.

NREL researchers arrived at an innovative method for arranging the fins for any fluid-cooled heat sink early in the year 2009. The unique feature of this invention is it uses fins to address or service every portion of the heat source area. It improves the heat flux that can be removed from the sink by a factor of two while reducing the pressure loss by half in comparison to conventional fin arrangement (such as shown in Figure 2). NREL researchers have submitted an invention report to the NREL legal office for potential pursuit of a patent. On account of this, while we may not discuss the geometric arrangements for the fins and the sink, we discuss the projected performance of the sink in the next section.

Computational fluid dynamics modeling results

For conventional heat sink, we projected the variations of heat flux (in W/cm^2) plotted as a function of the heat source plate temperature at constant COPs, in Figure 7. The COP (coefficient of performance) is the ratio of heat removed to the amount of parasitic power used to maintain the air flow at the assumed fan efficieny. Predicted data points are shown together with least-square fit straight lines to the data in this figure. Two values for COP are used, namely 25 and 50. The hottest temperature for the sink is varied from 125^oC (corresponding to today's silicon chips) to 200^oC (for a potential future chip material and fabrication technology). We find that the allowable heat flux increases linearly with increasing hottest temperature. The allowable heat flux is lower for the higher COP values, because we are removing heat

less aggressively. At the higher COP of 50, heat flux ranges from 100 to 240 W/cm^2. For the lower COP of 25, the flux range is from 140 to 270 W/cm^2.

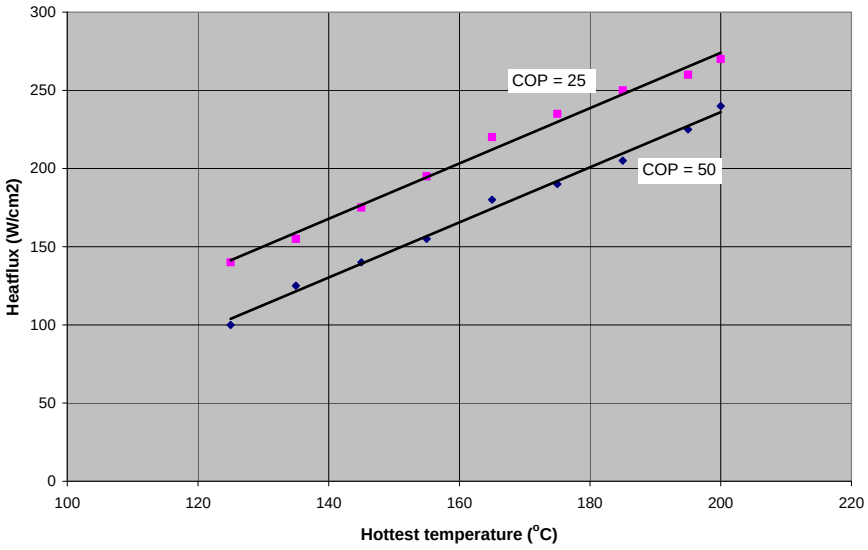


Figure 7 Projected heat flux as functions of chip high temperature and overall COP

With proper arrangement of the fins, we found that parasitic power can be reduced significantly without losing heat flux removal capacity at the same air mass flow. Doubling the mass flow still yields a higher COP and a higher heat flux. Simple modifications can boost the performance of the micro-channel considerably. Depending on the specific applications, key modifications to the geometry to maintain highly aerodynamic passages will result in further improvements in the overall performance of the micro-channel geometry.

Projected performance of a new test article designed at NREL is presented in Figure 8. Heat removed and parasitic power are plotted as functions of air mass flow (in g/s), for a conventional heat sink design and for a heat sink designed by NREL researchers. We note that both the heat removed and parasitic power increases with increasing air flow. At a nominal design point corresponding to an air flow of 8 g/s, the heat removed shows an improvement of about 15%. For NREL design it is about 570 W, compared to 510 W for the conventional design. Parasitic power reduction is substantial for the NREL design, of the order 50%. NREL design requires a power of only 10 W compared to 20 W needed for the conventional design. Another NREL design for a different configuration has been fabricated and is currently undergoing tests.

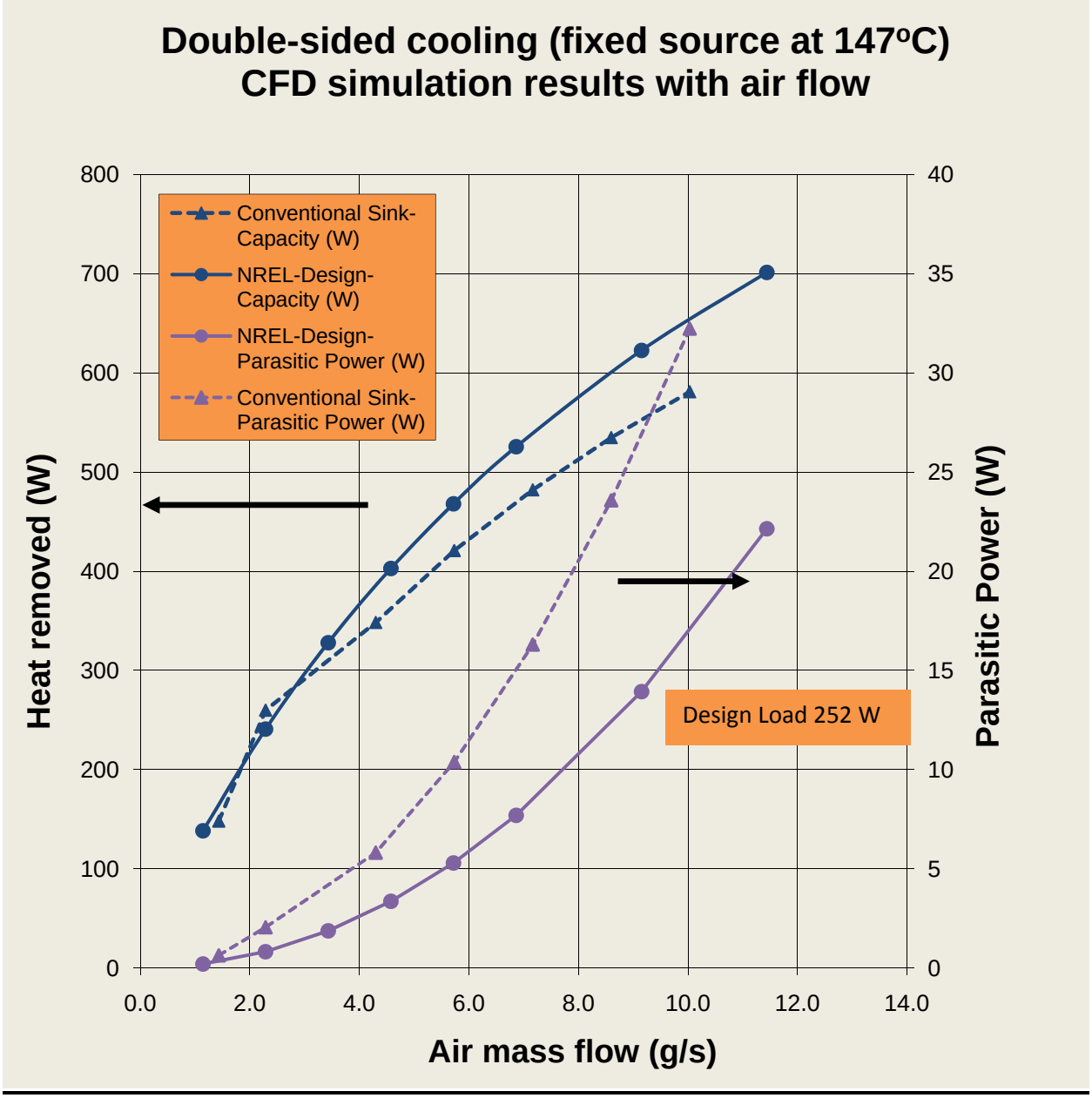


Figure 8. Comparison of performance for conventional and NREL design heat sink.

Measured pressure losses for the fabricated heat sink are shown in Figure 9. The data shows considerable scatter. However, the pressure loss varies linearly with air flow rate. The measured values are about 28% greater than predicted. At present, we suspect that the thin copper sheets that were used fabricate this sink might have potentially burs at the cut sheet edges. Closer examination of the copper sheets will help us pin down the cause for the increased pressure drop for the test article. Testing of this sink with heat loads are in progress.

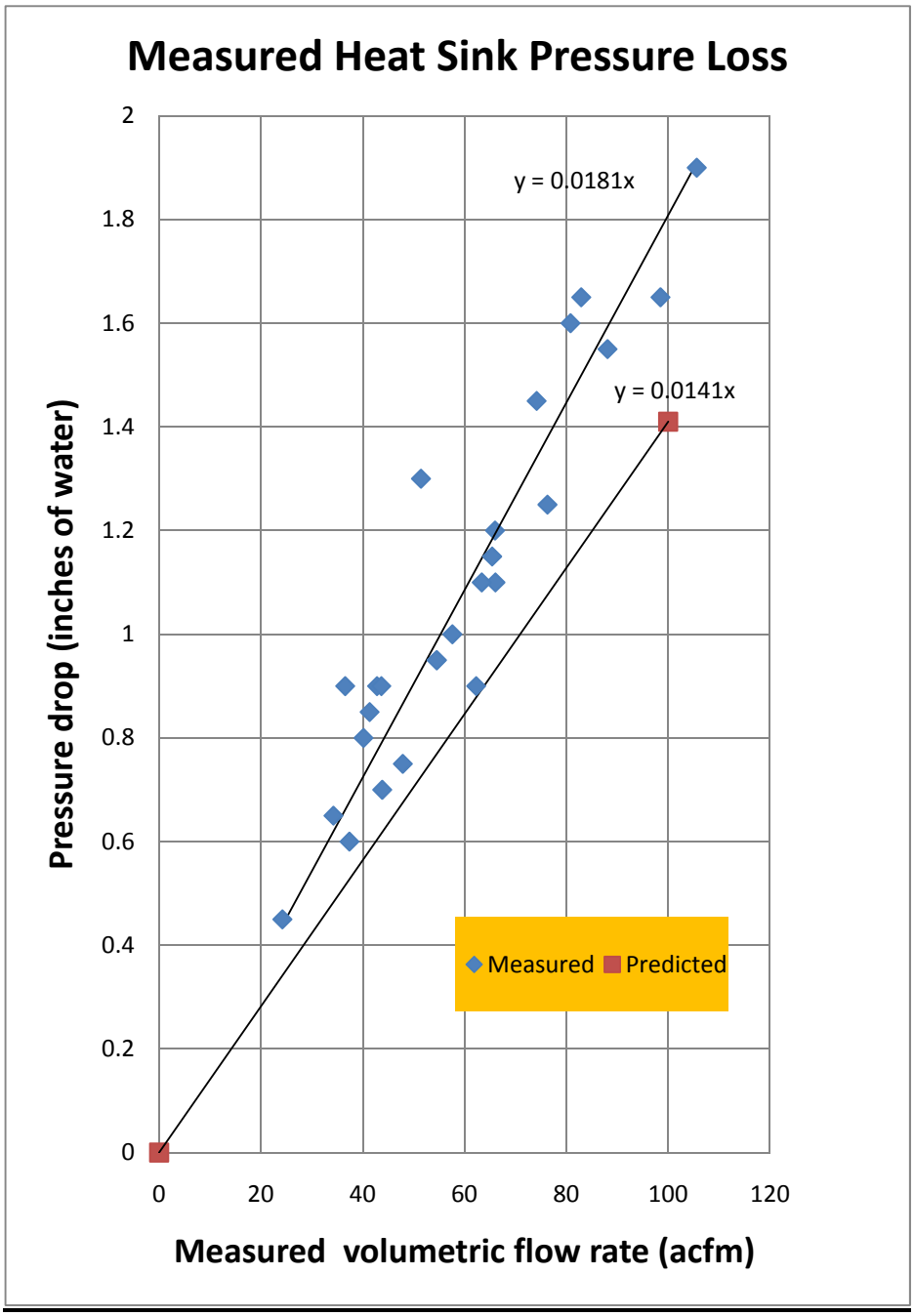


Figure 9 Projected performance of an innovative air-cooled heat sink

Other components of air-cooling approach

Key other parts for implementing air cooling include the prime mover, namely the fan, the air supply and removal ducts and an air filter to keep dust accumulating in the heat sink.

Fan: Fan, representing the prime mover, allows the air flow to be induced to flow through the heat sink. Fans remain one of the "neglected" components that require careful attention to improve the overall efficiency for the air cooled system. For a hybrid vehicle application with an electronic system capable of handling continuous power level of 30 kW, loss characteristics of the system suggest a steady-state heat removal need of nominally 3 kW. With ambient air available at 30oC, and an assumed air outlet temperature of 90oC, we need an air flow of about 50 g/s, or about 90 SCFM. Pressure loss characteristic for the system suggest a minimum pressure rise of about 2 inches of water (or 500 Pa). With these nominal specifications in mind, we selected a few commercially available fans to assess their performance. The following Table 3 compares the relative performance of these fans.

To compare, we introduce two commonly used fan (or single-stage compressor) parameters, namely, (following Balje, 1981):

The fan non-dimensional speed, n_s, as:

$$\underline{n_s = \frac{\omega\sqrt{V}}{(gH_{ad})^{\frac{3}{4}}}}$$

And the fan diameter, d_s, as:

$$\underline{d_s = D(gH_{ad})^{\frac{1}{4}}/\sqrt{V}}$$

In these equations, ω is the rotational speed (1/s), V is the volumetric flow (m^3/s), g is the gravitational acceleration (m^2/s), H_{ad} is the required head expressed in a height (m), and D is the mean fan diameter (m).

Based on the Table 3, we find the overall efficiencies for all fans lie below 40%, with some as low as 14%. Best efficiency is exhibited by fans by Xcelaero with an efficiency approaching 40%.

Based on their non-dimensional parameters, Balje provides a map of potential efficiencies that can be achieved for single-stage compressors. The fan characteristics are plotted on that map in Figure 10. The shown efficiency contours were developed for fans operating at a high Reynolds number of 1 million. At lower Re, the efficiencies will fall with decreasing Re. While a fan designed at the optimum conditions shown in this figure can achieve an efficiency of 0.85, realistic expectations for peak efficiency for such a fan operating at lower Re is perhaps 0.6. However, it is clear that when an application specific operating conditions are identified, custom designed fans should pursued to attain highest operational efficiencies.

Table 3 A comparison of operating characteristics for some commercially available fans

Manufacturer/Model		AMETEK Nautilair 8-inches*	ebmpabst 8200 JH3	Honda Insight Fan*	Mixtus 7.9 E-Series	Xcelaero Squall 50
Nominal Specification	Units	@80cfm and 3-in water	@80cfm and 3-in water	@100cfm and 1-in water	@100cfm and 2.2-in water	@100cfm and 2.2-in water
Air mass flow	(g/s)	46.28	43.39	57.85	57.85	57.85
Volumetric flow	(m^3/s)	0.0378	0.0354	0.0472	0.0472	0.0472
Required pressure drop	(Pa)	748	249	498	548	548
Mean fan diameter (d)	(m)	0.2032	0.08	0.08	0.2032	0.0762
Fan speed	(rad/s)	576	1466	377	471	1340
Adiabatic head (gH_{ad})	(m/s)^2	610	203	407	447	447
Spouting velocity (C-zero)	(m/s)	34.93	20.17	28.52	29.92	29.92
Tip speed (u)	(m/s)	58.52	58.64	15.08	47.88	51.07
Speed ratio (u/C-zero)	(---)	1.68	2.91	0.53	1.60	1.71
Non-dimensional speed, n-sub-s	(---)	0.91	5.12	0.90	1.05	2.99
Non-dimensional diameter, d-sub-s	(---)	5.20	1.61	1.65	4.30	1.61
q-adiabatic ($2gH/u^2$)	(---)	0.1782	0.0591	1.7890	0.1952	0.1716
Reynolds number (ρVd/μ)		409162	161433	41511	334769	133907
Fan Power	(W)	28.24	8.83	23.54	25.89	25.89
Actual Power	(W)	200	25	80	96	66
Efficiency Overall	**(---)**	**0.141**	**0.353**	**0.294**	**0.270**	**0.392**
***Measured values**						

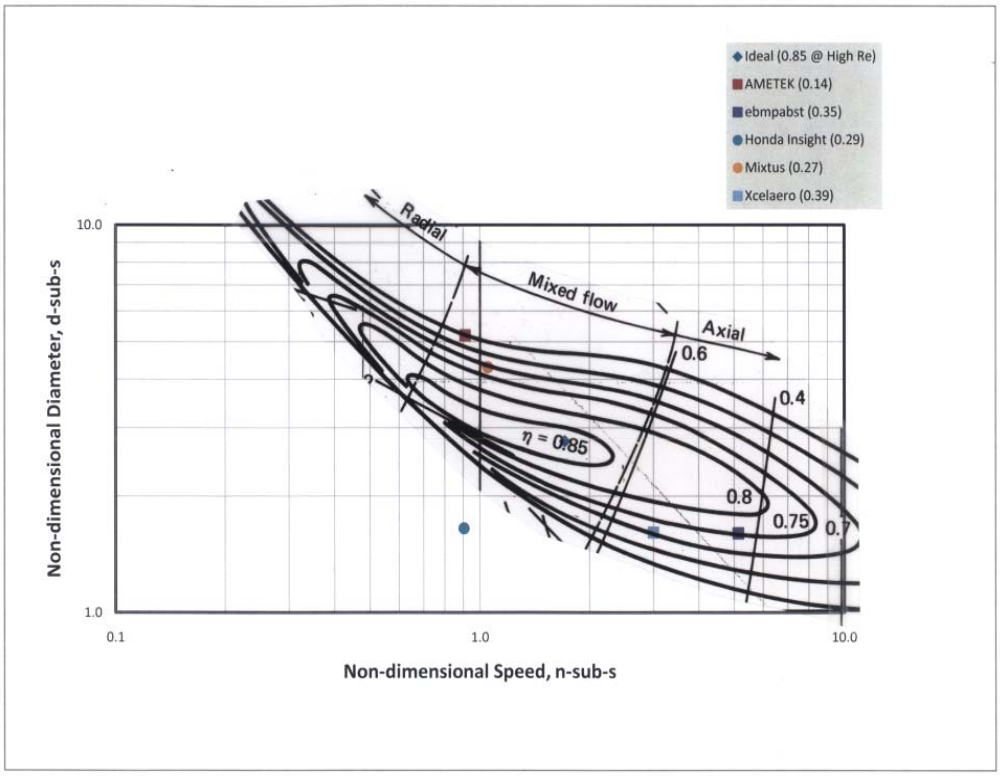


Figure 10 Fan design operating parameters are shown on a non-dimensional plot for expected single-stage compressors. An ideal fan for the given specifications falls at n_s of about 2 and d_s of about 3. Parameters for all commercially available fans (perhaps, designed for other applications) fall far from the optimum ideal fan parameters.

Ducting: Since we are seeking the coldest air available to cool the electronics, the ambient air must be brought in to vehicle and directed to the required areas. It makes no sense to use the "underhood air," which can turn out to be hotter the devices that we want to cool. To gather and direct air to the required areas, proper ducting should be designed. Proper care should be exercised in the design of the ducting so as not to cause excessive pressure losses in the system. All turns should be accomplished with elbows containing guiding vanes. Abrupt turns must be avoided. Basic aerodynamic principles for maintaining streamlined flow must be adopted. These guidelines will help minimize the power draw from the motive system for the vehicle.

Filter: Filtering requirements for the air flow for the micro-finned heat exchanger would require exclusion of air-borne particles of the order of 200 μm and above to be removed before they enter the ducts fan and the cooling system. The filter is likely to be located at the air intake near the front end of the vehicle perhaps adjacent to the radiator. The filter should be designed to take in air at a low-enough velocity so as not to cause pressure losses greater than 0.1 inch of water. We believe such filters should be readily available from existing line of products in the industry.

Conclusion

Aggressive designs for air cooling can meet the program goal for heat-flux removal rate as high as 200 W/cm^2 with relatively low cost and complexity. Air cooling allows ready access to cool other components of the system, such as the capacitors and other components.

While air cooling may not be appropriate for the current generation of silicon-based devices, it remains an attractive option for future devices that can operate at higher temperatures. Use of air helps avoid the need for a secondary cooling fluid in vehicles. Improving chip manufacturing technologies continue to push the envelope for the highest temperature environment that these chips may see during operation.

Air cooling remains a viable option for power electronics. Continued research in this area will result substantive progress in achieving the goals for this cooling technology. We recommend fabricating and testing working inverters that use advanced air cooling for heat removal devices.

Publications

Bharathan, D. and Kelly, K., "An assessment of air cooling for use with automotive power electronics," a paper presented at the 2008 ITHERM conference, April 2008.

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Patents

1. An invention report has been filed with NREL's legal office, pending processing.

2.6 Thermal Stress & Reliability for Advanced Power Electronics & Electric Machines

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Objectives

The objective of this research activity is to develop predictive modeling capabilities to assess the impacts of thermal stress on the life of advanced inverter package designs, and to demonstrate the modeling approach by evaluating dynamic thermal stresses of advanced APEEM designs.

Thermally induced stress is a major issue related to reliability, which is directly linked to heat dissipation and the electronics package configuration. Vehicle manufacturers and component suppliers must run extensive life and reliability testing on all new technologies and designs to understand the response to thermal cycling and environmental conditions. This research will work closely with industry to develop and validate advanced predictive modeling processes using techniques such as "physics of failure" to evaluate the impacts of new technologies on thermal stresses, life, and reliability. The ultimate goal is to reduce the amount of testing and the cost and time to market for new technologies. Predictive modeling tools, applied early in the development process can help guide research decisions, streamline development time, and identify potential barriers to meeting life and reliability goals. Physical modeling techniques will be used in conjunction with accelerated life testing to identify failure modes and relative impacts on reliability beyond what is currently available.

The specific goal of this fiscal year was to develop models to predict the life of bonded interfaces such as solder joints. We used a simple tin-lead solder for our initial analysis in order to gain confidence in our predictive techniques and compare the results to the extensive literature available on tin-lead solders.

Approach

- Subcontracted key personnel to assist in building the model
- Presented results to EE Tech Team and at Vehicle Power and Propulsion Systems conference
- Technical approach:
  - choose advanced power electronics package and thermal management technology to compare
  - created solid models in ANSYS finite element analysis (FEA) software
  - applied thermal boundary conditions and predicted the thermally induced stresses
  - used the Coffin-Manson model to predict the onset of failure in solder joints
  - compared results with those reported in literature

Major Accomplishments

- Developed a model to predict fatigue failure of solder joints in advanced power electronics packages

- Compared solder fatigue life characteristics for three combinations of package geometry and cooling mechanism
- Presented findings to EE Tech Team, authored two technical papers related to this work (one at the 2009 IEEE Vehicle Power and Propulsion Systems Conference; another at the ASME International Mechanical Engineering Conference), and will present at the 2009 IEEE Accelerated Stress Testing and Reliability Conference

Future Direction

- Explore the use of fast, high-level, models in conjunction with detailed FEA models in the assessment of power electronics designs for reliability
- Improve the bonded interface model to handle viscoplastic effects
- Enhance existing computer tools to handle:
  - Additional solder compositions for solder joint fatigue
  - Sintered joint failures
  - Capacitor failures
- Apply the toolset to technologies being considered under the APEEM program
- Add robust design (i.e., incorporation of variation and uncertainty) and optimization loops to enhance designs for higher reliability
- Work with reliability experts to review methodologies and develop new capabilities
- Validate the tools and predictions using test data

Technical Discussion

Power electronics are a key component of the electric traction drives being used and proposed for hybrid electric vehicles, plug-in hybrid electric vehicles, fuel cell electric vehicles, and pure electric vehicles. These vehicle technologies could play a key role in the reduction of vehicle emissions, reduction in the transportation sector's contribution to global warming, and enhancement of energy security due to reduced dependence on imported petroleum for transportation.

In order to increase the market share of advanced electric traction drive vehicles, component costs must come down while acceptable volume, weight, and life are maintained. The U.S. Department of Energy is collaborating with the U.S. automotive industry under the FreedomCAR and Fuel Partnership to develop component technologies that overcome the market barriers to advanced vehicle deployment. This report focuses on the power electronics (specifically, the power inverter) for advanced electric traction drive vehicles. Further details of the R&D program can be found in [1].

Thermal management and reliability at high temperature and under significant thermal cycling are may be required to enable lower cost system solutions. However, this is a difficult region for electronics to operate in reliably (see, for example, [2-4]). The electrical devices in the power inverter can experience immediate overstress failures at high temperatures. Furthermore, device reliability degrades as a result of fatigue mechanisms at higher temperatures and/or with higher magnitude or frequency of thermal cycling. Despite these challenges, the engineering community is pushing the limits of power electronics ever further. Improvements in thermal design have enabled further advances in power modules, allowing industry to meet increasingly stringent cost, weight, volume, and life targets (see, for example, [5]). This is not enough, however, as good thermal designs must also be reliable. Furthermore, it is increasingly important to evaluate reliability as we push the envelope into smaller, higher powered, and higher temperature systems.

This report presents a simulation study that begins to combine thermal performance with reliability prediction. In our study, the reliability of solder joints for three different cooling topologies is compared. The cooling topologies consist of two advanced options using jet impingement cooling and a baseline

option using pin-fin liquid cooling. Several major failure modes can be seen in automotive power modules. In this study, we will limit ourselves to predicting the number of temperature cycles until the onset of solder joint cracking. Delamination due to failure of the solder joint is one of the main failure modes for automotive power inverters (see, for example, [6]).

The paper begins with a literature review followed by an introduction to the model used and the simulation setup. Following that, thermal performance and reliability results are presented. Finally, concluding remarks and next steps are given.

Review of Prior Work

There are numerous studies on solder joint reliability in the context of electronics packaging (see, for example, [7-11]). Analytical models have been proposed to estimate the thermally induced (elastic) stresses due to differences in coefficients of thermal expansion between adjacent layers in multilayered bonded materials (see, for example, [12-13]). In these studies, both experimental and analytical evidence indicates that stresses in "soft" lead-based soldered joints are highest at the edges, and cracks will tend to propagate from the edge. This is not true for "hard" solders such as 80Au/20Sn or 95Sn/5Ag (see [11]). Furthermore, the literature indicates that the joint between the substrate and the heat sink is typically the weakest (see, in particular, [14]).

In [15-16], the authors discuss testing procedures called "power cycling" for both wire bond and solder joint fatigue. We use this solder joint power cycling procedure in our simulation as opposed to thermal shock procedures and/or temperature cycling procedures in which temperatures are induced via the ambient environment. Power cycling involves heating by means of the power semiconductors embedded in the inverter system under test.

Reference [4] presents a recent overview of the reliability challenges of advanced power modules for hybrid electric vehicles. The authors discuss the trend toward increased power density of next-generation power modules as well as industry's interest in operating power modules over a common coolant loop that includes the internal combustion engine (for hybrid electric vehicles). This would result in coolant temperatures up to 110^{o}C. This is similar to the coolant target of 105^{o}C used by the FreedomCAR and Fuel Partnership Electrical and Electronics Technical Team for the same reasons [1]. The relevant stressors on an automotive inverter are discussed, along with an overview of recent results of an analysis of wire bond cycles to failure and solder joint crack propagation due to stress/strain hysteresis. A reliability test with a temperature rise of 90^{o}C using a 95^{o}C coolant was briefly presented in which a mild-hybrid inverter (with output power of 8 kW) was shown to fail by wire-bond fatigue at 40,000 cycles.

In [17], the authors present three avenues for improving the power density of power inverters for automotive applications: better cooling, devices and packages that tolerate higher temperatures, and reduction of losses at the chip. Interconnection reliability in high-temperature-tolerant inverter packages is cited as a major requirement for the realization of inverters that tolerate higher temperatures. The failure mechanisms behind solder cracking and wire-bond lift-off are reviewed, as well as which accelerated tests correspond to which mechanisms: thermal shock tests and temperature cycling tests are commonly used for solder joint reliability, while power cycling is commonly used to determine wire-bond fatigue failure. Data for percentage delamination by number of temperature cycles are presented; unfortunately, the testing conditions are not stated.

Simulation Setup

In this study, three topologies for a hybrid inverter are compared with each other on the basis of their heat transfer performance and the reliability of their soldered interconnects. The three topologies include a baseline system that uses a liquid-cooled pin-fin heat sink and two advanced concepts that use jet

impingement cooling. The two jet impingement concepts are of interest because they have similar thermal performance but potentially very different reliability implications that reflect their different designs. In the following sections, the geometry, material properties, boundary conditions, and loading of the models will be discussed.

We used SolidWorks™ and Pro/ENGINEER™ to build the geometries and ANSYS™ version 11 to predict steady-state temperature, thermally induced stress, and solder fatigue failure results. The fatigue analysis required the ANSYS™ Fatigue Module.

Geometry and Material Properties

The models used in this analysis represent a small section of a larger inverter. Specifically, we modeled a single insulated gate bipolar transistor (IGBT) and diode pair. Our model is loosely based on the power semiconductor layout and sizes of the model year 2004 Toyota Prius, as shown in Figure 1. In the photo, the gate drivers and housing have been removed to show the power semiconductors. The Prius inverter drives two electric machines: a traction motor and a generator. The yellow dashed line in Figure 1 encircles the part of the inverter that drives the traction motor, and it is the focus of this study. More details on the Prius inverter and motor technology can be obtained from [18]. The IGBT and diode pair in our models loosely correspond to the inset of Figure 1. Note that we are not modeling wire bonds for this study.

Three geometries are being used in our study. The first, topology 1, a baseline system, is shown in Figure 2. The left side of the figure shows a top view, and the right side depicts the package topology from the bottom and highlights the pin-fin array design. The pin-fins have an elliptical shape. From top to bottom, the layers of this geometry are power semiconductors (one IGBT and one diode—the IGBT is the larger device) modeled with the temperature-dependent material properties of silicon, 63Sn-37Pb solder, an aluminum nitride (AlN) substrate metallized on the top and bottom with copper (this layer is called the DBC or direct bond copper layer), 63Sn-37Pb solder, an aluminum baseplate, a layer of thermal grease, and the aluminum pin-fin heat sink.

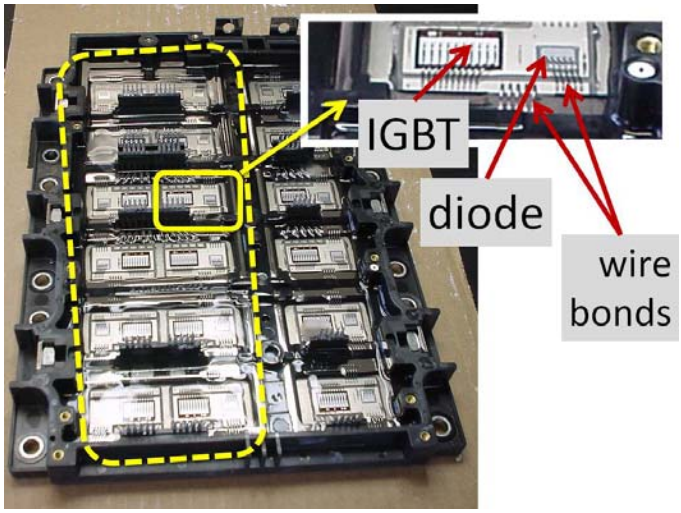

Figure 1: Example HEV Inverter (MY2004 Prius)

The layer thicknesses are depicted in Figure 3. Note that pin-fins are not depicted in this figure. Figure 2 and 3 share the same top section as topology 1 from the power semiconductors to the substrate. In topology 2, instead of having a thermal interface material and pin-fin heat exchanger, a coolant jet

impinges upon the baseplate. This is depicted in Figure 4. The dashed line in the figure indicates two jets—each jet is located directly below a power semiconductor.

Topology 3 goes one step further by removing the base plate and directly impinging upon the metalized bottom of the DBC substrate. Topology 3 is depicted graphically in Figure 5.

The dimensions of the power semiconductors and DBC are given in Figure 6. Further exploration of the heat transfer for these package geometries is given in [19]. The temperature-dependent properties of the materials used in this study were obtained from [20]. Temperature-dependent properties were used because of the large change in some properties across the temperature range of thermal cycling. For example, the thermal conductivity of silicon varies from over 170 W/m-K at -40°C to under 100 W/m-K at 150°C; this temperature range is commonly considered in the testing of components for automotive applications. Fatigue properties of the solder (presented later) were estimated using [21].

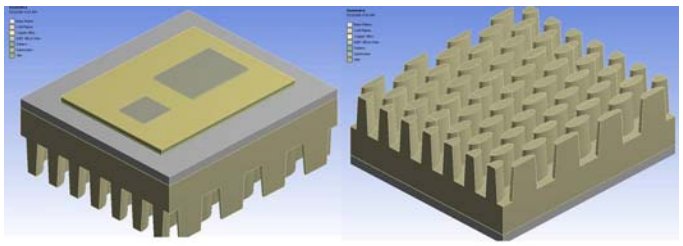

Figure 2: Topology 1: Baseline Package with Pin-Fin Cooling

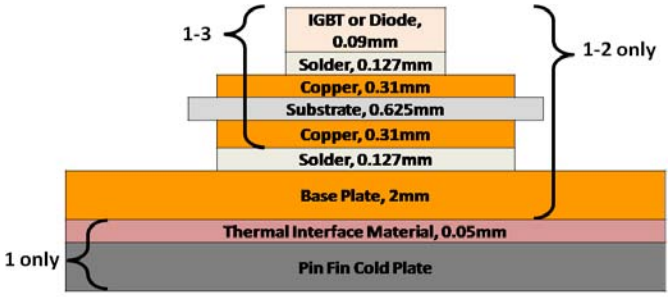

Figure 3: Layer Thicknesses and Materials in Package Topologies Modeled

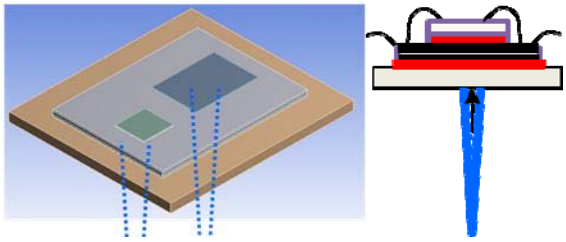

Figure 4: Topology 2: Indirect Jet Impingement on Base-Plate

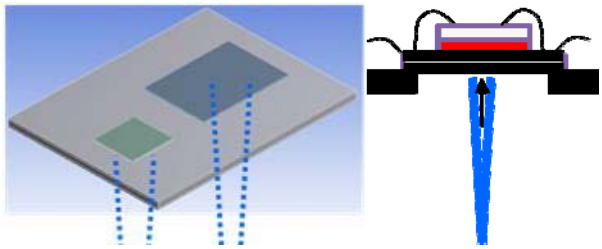

Figure 5: Topology 3: Indirect Jet Impingement on DBC Substrate

Heat Transfer Boundary Conditions

It is important to correctly predict the temperature distribution since the thermally induced stresses and fatigue analyses require it. Two heat transfer boundary conditions are relevant to the topologies examined in this study: pin-fin convective cooling and jet impingement cooling. Both boundary conditions are discussed below. The coolant used in this study is 50/50 by mass of water and ethylene glycol, and the fluid properties are obtained from [22]. The coolant inlet temperature is assumed to be 105°C during periods of maximum heat generation.

The pin-fin heat exchanger used in topology 1 contains pins spaced 5.08 mm apart in the transverse direction (perpendicular to the flow) and 10.16 mm apart streamwise. The pins are 7.62 mm tall and taper from top to bottom; they are 2.8 mm x 6 mm at the top and 2 mm x 5.2 mm at the bottom, and the dimensions are ellipse minor and major diameters, respectively. A total of 5 liters per minute of coolant flows through the section of the array pictured in Figure 2 (a parallel section carries an additional 5 liters per minute for a total flow of 10 liters per minute through the inverter). Note that the actual Prius inverter uses straight fins instead of pin-fins. However, pin-fin heat exchangers have appeared in other automotive inverters. The portion of the heat sink above the pins is 6.35 mm thick.

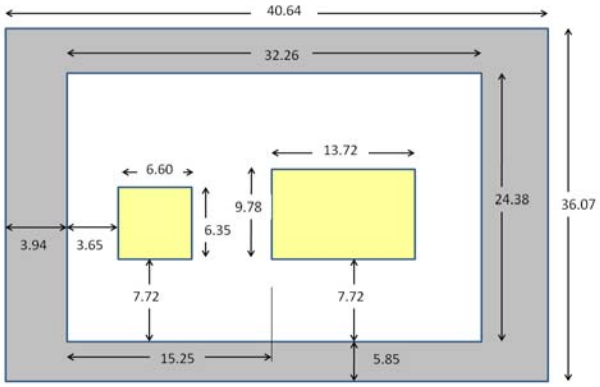

Figure 6: Dimensions of Package Topologies (mm)

Empirical relations for pin-fins from [23] were used in conjunction with CFD analysis to predict the area-averaged local heat transfer coefficient across the pin-fin surface. Fin efficiency is taken into account directly by explicitly modeling the pin-fins.

For jet impingement, the relation from [24] was used. This relation breaks the jet heat transfer coefficient into an impingement zone and a wall-jet region. For this analysis, we assume that there is no interference between adjacent jets. The heat transfer coefficients applied to the various model boundaries are

summarized in Table 1. We applied an area-averaged heat transfer coefficient directly below each power semiconductor on the baseplate; this heat transfer coefficient consists of an area average of impingement zone and wall jet zone directly under each chip. The remainder of the DBC is assumed to be in the wall jet region.

The jet nozzle diameter is assumed to be approximately 1.4 mm based on a simple calculation of 1 jet per 1 power semiconductor and a total of 24 power semiconductors (i.e., a total of 12 IGBTs and 12 diodes) at a total flow rate of 10 liters per minute and target nozzle velocity of 4.5 m/s per jet.

Table 1. Heat Transfer Coefficients Used In Simulation

Location	Heat Transfer Coefficient (W/m2.K)
Pin surface	10,437
Surface between pins	1,191
Jet impingement diode	31,534[b]
Jet impingement igbt	20,426[b]
Wall jet zone (under DBC[a])	15,382
Outside the wall jet zone	1,191

a. Direct bond copper layer. b. Note that the effective diode heat transfer coefficient is higher than for the IGBT due to the jet effect being area-averaged over a smaller area

Loading Conditions

A simple relationship was used to estimate the heat generation due to losses in the IGBT and diode pair. This estimate corresponds to an electric traction drive system of 55 kW, per the FreedomCar and Fuel Partnership targets [1]. A peak efficiency of ~98% was assumed for the inverter and 94% for the motor drive. Using the Prius geometry, 12 pairs of devices were assumed (i.e., 12 IGBTs and 12 diodes for a total of 24 devices or 12 pairs of devices). This results in a heat loss per IGBT and diode pair of approximately 120 W. Approximately 70% of the heat was apportioned to the IGBT and 30% to the diode, based on a rough estimate of the heat breakdown between components. This results in a heat loss per diode of 35 W and heat loss per IGBT of 85 W.

Structural Support

Structurally, the three topologies are assumed to be floating in space with “weak springs” as structural boundary conditions. This technique was chosen to avoid mounting-specific complexity.

Failure Models and Physics

Although there are several failure modes of concern for power inverters in automotive applications (see, for example, [6]), this study is focused only on solder joint fatigue due to temperature cycling. Solder joint delamination is one of the main failure modes in power inverters (see, for example, [25]). As reported in the literature, temperature cycling and thermal shock tests tend to directly stress solder joints and elicit failures. These tests are conducted in environmental chambers where the system under test is subjected to extreme changes in external temperature from ambient or even -40^{o}C to 140^{o}C or greater (see, for example, [26]).

Based on the discussion in [15], we are simulating a power cycling test in which the devices in the inverter create the heat necessary to raise the inverter temperatures, after which the entire inverter is allowed to cool back to ambient conditions (assumed to be 22^{o}C). The end effect is similar to those of the temperature cycling tests discussed above, but more realistic since the temperature distribution

corresponds to that of an active inverter. Note that this is different from power cycling tests conducted to elicit wire-bond fatigue failures.

In power cycling for wire-bonds, the package is never allowed to cool back to ambient conditions, and the power semiconductors are cycled on and off at a higher frequency. In contrast, the power cycling method to elicit solder joint fatigue has much higher temperature rises, which bring the inverter to a high temperature and then back to ambient, but at a much lower frequency than power cycling for wire-bond fatigue. We currently do not take viscoplastic or other dynamic effects such as creep into account with our model. Instead, our model calculates the effect of going from a stress-free state to the thermally induced stress state associated with the steady-state temperature field obtained by applying the heat loading condition. One power cycle is depicted in Figure 7.

The solder joints can experience both elastic and plastic deformation during high temperature excursions. The model we use to account for the elastic and plastic strain conditions is called the strain-life relationship:

$$\frac{\Delta\epsilon}{2} = \frac{\sigma_f'}{E} \cdot \left(2 \cdot N_f\right)^b + \epsilon_f' \cdot \left(2 \cdot N_f\right)^c \qquad \text{Equation (1)}$$

In (1), $\Delta\epsilon$ is the change in strain due to the application of our loading condition. The factor of 2 occurs because (1) is derived under the assumption of completely reversed loading—i.e., a load is fully applied in one direction and then applied at the same magnitude in the opposite direction. Thus, the total change in strain for the application of a load in one direction is half the total. N_f is the number of cycles to failure (the parameter of interest). E is the modulus of elasticity.

The remaining four terms are fatigue strength coefficient, σ_f', fatigue strength exponent, b, fatigue ductility coefficient, ϵ_f', and fatigue ductility exponent, c. The first term of (1) accounts for cycles to failure under elastic deformation, while the second term accounts for cycles to failure under plastic deformations. An in-depth derivation and discussion of this relationship and the parameters that are used can be found in [27] and Chapter 2 of [21]. A discussion of the engineering behind the ANSYS fatigue module that implements the strain-life model can be found in [28].

The fatigue properties of the solder corresponding to the strain-life model from (1) are given in **Error! Reference source not found.**. These properties were estimated using material properties from [20] and guidelines from [21]. Four empirical properties are needed to use (1): σ_f', b, ϵ_f', and c. Two additional properties, called cyclic strength coefficient, K', and cyclic strain hardening coefficient, n', are reported as well. These can be derived by curve fitting experimental data (see [21]) and relate to the other parameters as follows [21]:

$$K' = \frac{\sigma_f'}{\left(\epsilon_f'\right)^{n'}} \qquad (2)$$

$$n' = \frac{b}{c} \qquad (3)$$

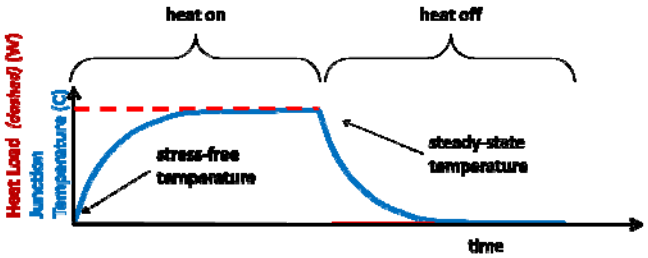

Figure 7. Equivalent Power Cycle Test

Table 2. **Fatigue Properties Estimated for 63Sn-37Pb Solder**

Fatigue Property	Value
Fatigue strength coefficient (MPa),	93.3
Fatigue strength exponent,	-0.085
Fatigue ductility coefficient (MPa),	1.0×10^{-6}
Fatigue ductility exponent,	-0.6
Cyclic strength coefficient (MPa),	93.3
Cyclic strain hardening exponent,	0.15

Results and Discussion

The results section is broken into two parts: thermal performance and solder joint fatigue failure prediction. The motivation behind topologies 2 and 3 is based on their thermal performance, but thermal performance alone is not sufficient. As new designs push the limits of materials and devices, the reliability must be considered as well. The section on fatigue prediction begins to address greater questions of concept feasibility in terms of meeting life requirements.

Thermal Results

The steady-state peak temperatures at the power semiconductors under the analysis conditions presented in the simulation setup section are given in Table 3. Figure 8 depicts the temperature profile of topology 1 and shows the location of the maximum temperature to be on the IGBT. There is nearly a 25% drop in thermal resistance from junction to fluid between topology 1 and 2. Thermally, topology 2 and 3 are similar.

The three topologies are interesting from a thermal perspective as there is a complex relationship between heat transfer coefficient, package thermal resistance, and heat spreading. Jet impingement provides an increased heat transfer coefficient but lower surface area. The pin-fins of topology 1 have a large area for heat transfer, but must contend with fin efficiencies and a lower heat transfer coefficient at the pins. This results in a few interesting "cross-over" points, as shown in Figure 9. The same results corrected for heat transfer coefficient multiplied by the area are shown in Figure 10. These phenomena have been reported elsewhere (see [19, 29]).

Table 3. Steady-State Peak Temperature Results

Topology	Max Temperature at IGBT (°C)	Max Temperature at Diode (°C)	Package Thermal Resistance (°C/kW)
Topology 1	136.1	133.3	279
Topology 2	130.3	126.7	211
Topology 3	129.8	117.7	206

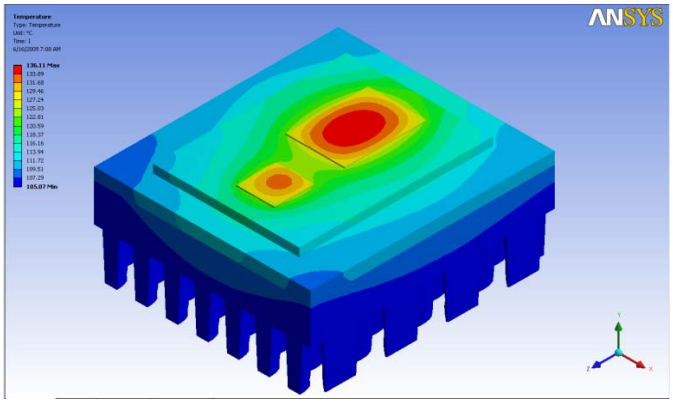

Figure 8. Temperature Distribution in Topology 1

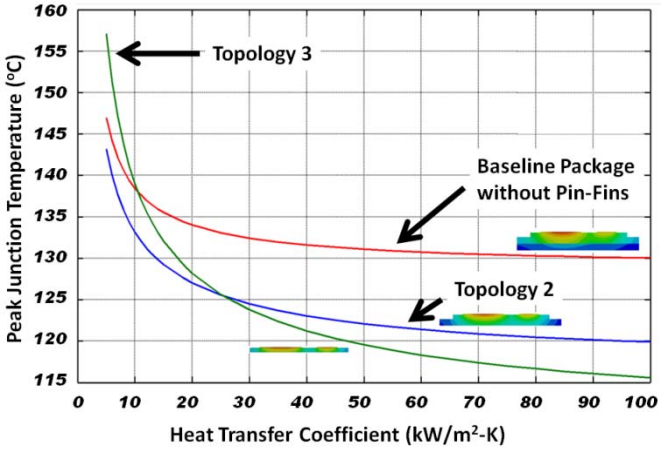

Figure 9. Thermal Performance by Heat Transfer Coefficient

Solder Joint Fatigue Results

Each topology is expected to dissipate the same amount of heat. However, the temperature rise for each topology is different on account of their different thermal performances (see Table 3). This is an important caveat since one may wish to use the enhanced thermal performance of topology 2 and 3 to dissipate more heat. One must use caution with this approach, since both topology 2 and 3 have less thermal mass than topology 1. Thus, the junction temperature of topology 2 and 3 would rise faster than topology 1 under fault conditions such as a loss of flow and/or short circuits. This matter requires further investigation.
As shown in Figure 11, the analysis predicts that fatigue failure initiates from the edges which is expected for lead based solders as discussed in the literature review.

The fatigue cycles to failure presented in Table 4 show a dramatic difference in fatigue life between the DBC solder joint and the other die attach joints. From the literature review, we expected the DBC solder joint to be the most susceptible to fatigue failure. This joint attaches the DBC to the base plate in topologies 1 and 2. Thus, we expected the model to predict the lowest number of cycles to failure for this joint based on test data from the literature (see, for example, [10]).

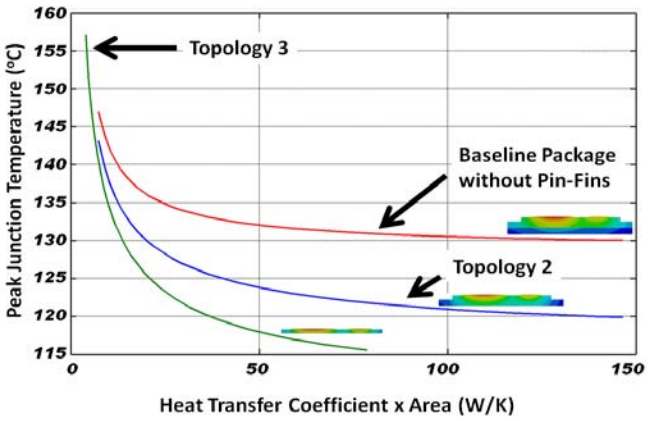

Figure 10. Thermal Performance by Heat Transfer Coefficient Times Area

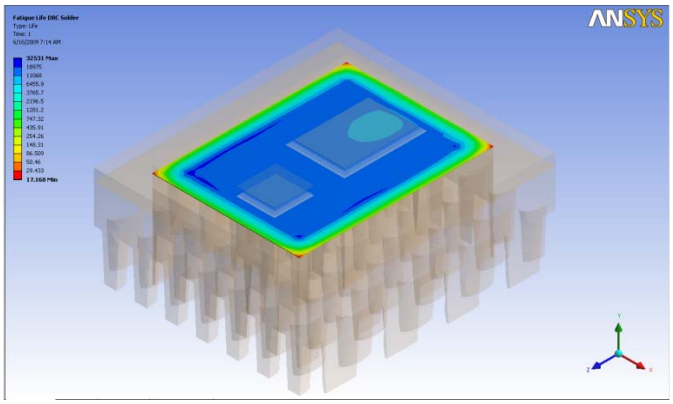

Figure 11. IGBT Solder Fatigue Life for Topology 1

Table 4. Cycles to Failure Under Simulated Conditions

Topology	Cycles to Failure for DBC Solder	Cycles to Failure for IGBT Solder	Cycles to Failure for Diode Solder
Topology 1	**17**	26,261	31,032
Topology 2	**163**	18,031	23,558
Topology 3	NA	**36,465**	42,245

Based on the literature, the predicted number of cycles seems reasonable. Basaran and Chandaroy [30] state that "a few hundred cycles of -40°C to +130°C is typically enough to cause cracks and electrical failures." We interpret the fatigue failure predicted by our analysis as the onset of a growing crack that will eventually lead to unacceptable delamination. As the solder delaminates, the thermal contact between the joined layers degrades, causing an increase in temperature. The device will eventually fail as a result of this excessive temperature and/or a loss of connection to the lower layer.

Reference [14] presents test results for solder joints subjected to thermal shock. Figure 6 of [14] indicates the onset of a crack occurs in less than 50 cycles for a temperature delta of 180°C for experiments with lead and lead-free solders (the exact composition was not disclosed in the paper as it was considered

proprietary). Since for this study we define failure as the onset of cracking, the number of "cycles to failure" would be lower than 50 under our definition. Similarly, Figure 9 of [17] depicts the onset of delamination on the order of hundreds of cycles. Unfortunately, the temperature range and solder type are not reported in this paper, so we cannot draw stronger conclusions. Based on the limited data available, the predicted low number of cycles for DBC solder joint fatigue seems reasonable.

In terms of the die attach solders (i.e., the IGBT and diode solder joints), [15] presents information on power cycling to predict solder joint lifetimes at the die attach. The authors report a lifetime of 1.7×10^4 cycles for a 100^oC temperature rise for the die attach solder. This is of similar magnitude to the predicted value of approximately 2 to 2.5×10^4 for the topology 1 and 2 packages from **Error! Reference source not found.**.

In Table 4, the minimum number of cycles to failure is highlighted. Based on the analysis results under the conditions and scope of consideration for this study, we see that topology 3 offers a significantly higher cycle life due to the elimination of the weakest joint. However, additional failure mechanisms may have been introduced into topology 3 (e.g., leakage of the coolant, failure of the sealing gasket, etc.). More work is necessary before final conclusions can be drawn.

Conclusion

This report presented preliminary work in the application of modern computer-aided engineering tools to assess the thermal performance and reliability of three different power inverter topologies. Although the models have not been directly validated against experimental data, there appears to be good qualitative agreement between the numbers we predict and information in the literature. Based on the data available so far, topology 3 shows promise both from a reliability standpoint (by removing the weakest solder joint from the system) and from a thermal performance standpoint. However, more work is required.

Future planned activities include model validation testing, prediction of solder crack propagation with cycling, wire-bond flexural fatigue prediction, expanding the solder models to include viscoplastic effects such as creep, incorporating substrate reliability (brittle fracture), bringing more rigor and analysis to the structural loading boundary conditions, adding transient heat transfer effects such as fault conditions due to short circuit or loss of coolant, adding vibration loading conditions, etc. In addition, we intend to enhance the thermal loading conditions similar to those in [31] and enhance the thermal-fluid models and associated predictions.

Publications

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2. Vlahinos, A. and O'Keefe, M. (Nov. 2009). *Sensitivity of Solder Joint Fatigue to Sources of Variation in Advanced Vehicular Power Electronics Cooling.* To be presented at the 2009 ASME International Mechanical Engineering Conference & Exposition. November 13-19, 2009 in Lake Buena Vista, Florida.

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3. Electric Machinery Research and Technology Development

3.1 A New Class of Switched Reluctance Motors

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Objectives

- Develop switched reluctance (SR) motor (SRM) technologies using a novel isolated multiple flux path (IMFP) approach.
- Verify feasibility through finite element analyses (FEAs) and fundamental assessments.
- Design a novel converter topology for the base SRM design, if applicable.

Approach

- Analyze various IMFP SRM designs.
  - — Perform crude flux flow, winding configuration, torque ripple, and reliability assessments.
  - — Verify overall feasibility of designs.
  - — Choose most favorable designs.
- Conduct FEAs.
  - — Perform analysis on conventional and IMFP SRM.
  - — Obtain three-dimensional flux paths, when necessary.
  - — Determine magnetic flux as a function of rotor angle between the unaligned and aligned positions as a function of current (needed for control development and dynamic simulation).
- Research novel inverter topologies.
  - — Explore use of unique IMFP SRM characteristics to improve conventional converter topologies.
  - — Study ways to reduce chip count and increase specific power and power density.

Major Accomplishments

- Assessed feasibility of various design techniques.
- Selected a preferred design technique.
- Made improvements on conventional SRM technology including the following:
  - — Developed hardware and software solutions for reducing torque ripple and acoustic noise.
  - — Demonstrated that for low and moderate torque levels, near zero torque ripple could be achieved.
  - — Increased power density via continuous conduction control.
- Maintained inherent advantages of conventional SRM, including
  - — simple, robust, and low cost rotor and stator and
  - — no permanent magnet (PM) material.
- Developed two universal dynamic simulators (crucial for structural and acoustic noise modeling).

  - — Parametric simulator: efficient means to optimize control and design parameters.
  - — FEA simulator: highly accurate, but more suited for known control and design conditions.

Future Direction

FY 2010

- Refine preferred design and approach.
  - — Further investigate aspects of novel design approach.
  - — Perform structural, thermal, and acoustic noise studies (aimed at minimizing torque ripple and acoustic noise). Conduct design parameter optimization studies.
- Optimize control system.
  - — Use continuous conduction when applicable.
  - — Incorporate torque ripple reduction into control software.
- Fully verify and simulate final design.
  - — Obtain maximum torque and power curves.
  - — Determine power density, specific power, and efficiency from simulation results.

FY 2011

- Build and test prototype.
  - — Assemble and integrate controller and converter.
  - — Build and test at least one design variation.

Technical Discussion

Due to the unpredictable cost and availability of PMs, which are used in most hybrid vehicle applications today, many automotive manufacturers have a common interest in the use of electric machines which do not use PM material. Although these PM motors are not easily surpassed in regards to efficiency and power density, other competitive motor technologies exist which can have lower cost per power rating ($/kW). Of the alternative motor technologies, the SRM offers the simplest rotor configuration, which is advantageous in terms of material cost, manufacturing cost, speed capability, and reliability. The highly nonlinear behavior and unusual control methods associated with the SRM require the use of sophisticated and computationally intensive software programs to fully optimize its design and operation. Therefore, the SRM is a relatively young motor technology in terms of research and development, as opposed to other technologies such as the induction motor. Two primary drawbacks of the SRM are the level of torque ripple and the acoustic noise inherently associated with the SRM's doubly salient stator and rotor geometry. The intent of this project is to apply novel design techniques that significantly reduce torque ripple and acoustic noise while maintaining the intrinsic benefits of the SRM.

Existing torque ripple and acoustic noise reduction techniques typically incur significant compromises of things such as peak torque, torque power density, material/manufacturing costs, and/or design complexity. A conventional SRM with eight stator teeth and six rotor teeth is shown in Fig. 1. If the rotor is assumed to be rotating clockwise, the two stator teeth without a superimposed yellow "X" are the only stator teeth that would have excited windings if a conventional control scheme were used. That is, only two (25%) of the eight stator teeth are active during this instant. As the rotor position continues to increase in the clockwise direction, coils of two additional stator teeth are excited, and thus 50% of the stator teeth are active at that instant. However, this condition is maintained only for a short duration, and thereafter only 25% of the stator teeth are active, giving a low average of active stator teeth.

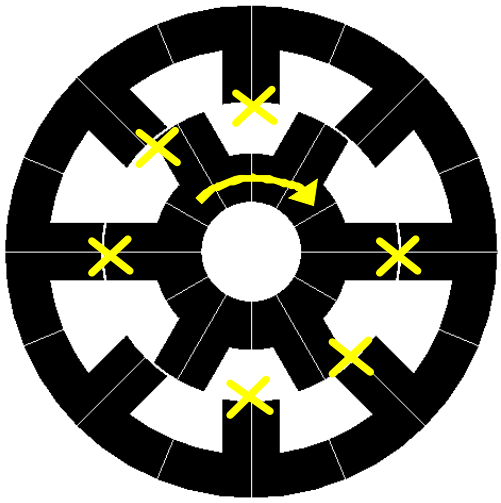

Fig. 1. Active stator teeth of a conventional 8-6 SRM (four-phase).

Because of the low amount of active air gap area within the conventional SRM, it was hypothesized that novel concepts could be used to increase the average amount of active stator teeth producing productive torque to more readily distribute the torque production and thereby reduce torque ripple. However, because the fundamental means by which torque is produced in an SRM rely on the magnetic saliency of the stator and rotor, it can be difficult to increase the amount of active stator teeth without compromising the reluctance ratio between aligned and unaligned rotor positions. This a result of introducing stator teeth within a closer proximity of each other, thereby promoting detrimental flux flow through undesired paths, which potentially decreases the overall torque capability of the machine. Therefore, the proposed general approach uses separate steel pieces and/or laminations to carry out the tasks mentioned above while seeking to minimize counterproductive flux flow by means of magnetic path isolation. Figure 2 shows two examples of the ways in which magnetic path isolation was approached, with interweaved laminations shown on the left and separate laminated pieces shown on the right. These concepts can be applied to the rotor and/or stator, depending on the configuration. Since the permeability of steel approaches that of air as magnetic saturation increases in the steel, it is not possible to have completely isolated magnetic paths in this type of application, particularly since the SRM often operates in the saturation region. Therefore, these types of hardware approaches must be incorporated carefully so that the natural operation and control of the motor inhibits the detrimental tendencies of leakage and undesired flux paths.

In addition to the hardware approach and control conditions discussed above, it was also desired that the SRM be operated with a continuous conduction control technique. Continuous conduction control can greatly increase the output power of an SRM at moderate and high rotor speeds as a higher amount of ampere-turns is applied during the torque production region (for the motoring operation mode). This is achieved by not requiring the ampere-turns in each stator tooth to reach zero during each electrical cycle. Since ampere-turns are still being applied when the rotor rotates beyond the alignment position, negative torque is applied to the shaft and thus this control mode does not operate with utmost efficiency, but it can greatly increase the power capability of the machine. This is particularly relevant to vehicle propulsion applications, wherein the average required power is relatively low for normal driving conditions and only short durations of high power demand are required for situations such as passing other vehicles or merging with high-speed traffic.

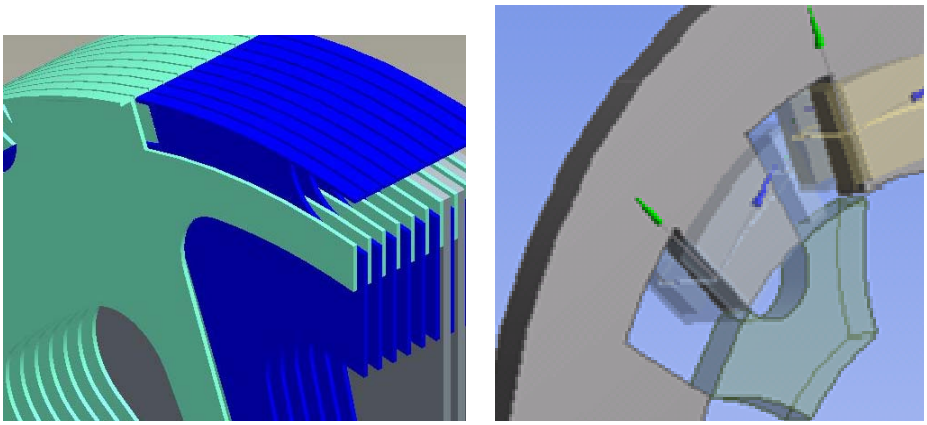

Fig. 2. Exemplar attempts toward magnetic path isolation.

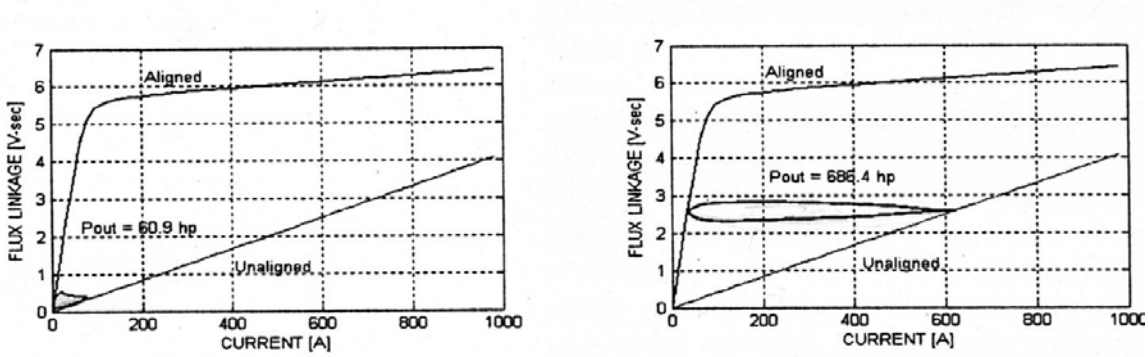

Fig. 3. Conventional control (left) and continuous conduction control (right).

Preliminary Studies—Interweaved Laminations

Preliminary studies were conducted using the conventional 12-8 SRM to investigate the feasibility of the interweaved lamination hardware configuration mentioned above. When applied to the rotor, the laminations are tapered in the radial direction so that a lamination is wide at the air gap but quickly tapers to make room for the adjacent lamination. Nonmagnetic spacers would serve as mechanical support and minimize flux flow between the laminations. Initially the impacts of channeling flux were studied through a series of basic FEA simulations. Figure 4 shows some of the shapes used to study the impact of various tapering geometries. Most of the shapes are not feasible in terms of overall design, performance, or fabrication, but rather illustrate the disadvantages of various tapering geometries. They offer crude, yet important data points and fundamental insight into design parameters on a generic level. Figure 5 is an example of how one of these shapes was applied to a conventional SRM rotor. Note that again, there would be no advantage to carrying through with this approach in a conventional SRM, but it can be used to study such geometries. A few flux density vector plots from static FEA simulations of various tapering lamination geometries are shown in Fig. 6. These results were surprising and encouraging in the sense that with the more feasible geometries (the two rightmost images), the rotor did not reach magnetic saturation before the stator reached magnetic saturation. Thus, the tapering of the laminations did not impose significant limitations on the natural magnetic circuit of the conventional SRM.

The next and most important aspect to be studied was the effect of leakage between adjacent laminations. Various geometries were used to investigate this phenomenon and one example is shown on the right in Fig. 5. The occurrence of this particular type of leakage greatly depends on the inherent characteristics and control of each design, and particularly when novel geometries are used, it is challenging to specify a configuration where such inherent characteristics are entirely known. A series of static FEA simulations

were conducted to determine the impacts of interlamination leakage. Simulation results indicate that there was only a 10% average decrease in torque in comparison with the conventional SRM. While this does not initially appear to be a positive finding, the interwoven lamination approach can be incorporated into novel geometries to gain an overall increase in average torque while obtaining improvements in torque ripple over the conventional SRM. However, when this concept is used in the design of a novel rotor, the result is typically structurally complex, and the design process becomes more significant. More important, the manufacture and reliability of complex rotor designs is also challenging. Therefore, while this approach is not necessarily infeasible, it is not well suited for broad-based analyses of a wide variety of novel concepts. Therefore, focus was placed on implementing an approach more suited to this project.

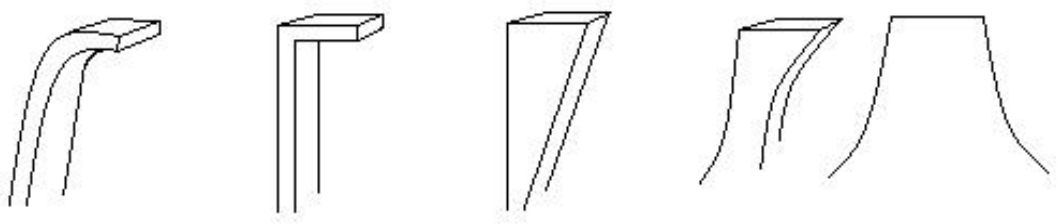

Fig. 4. Some of the various shapes used to study lamination tapering effects.

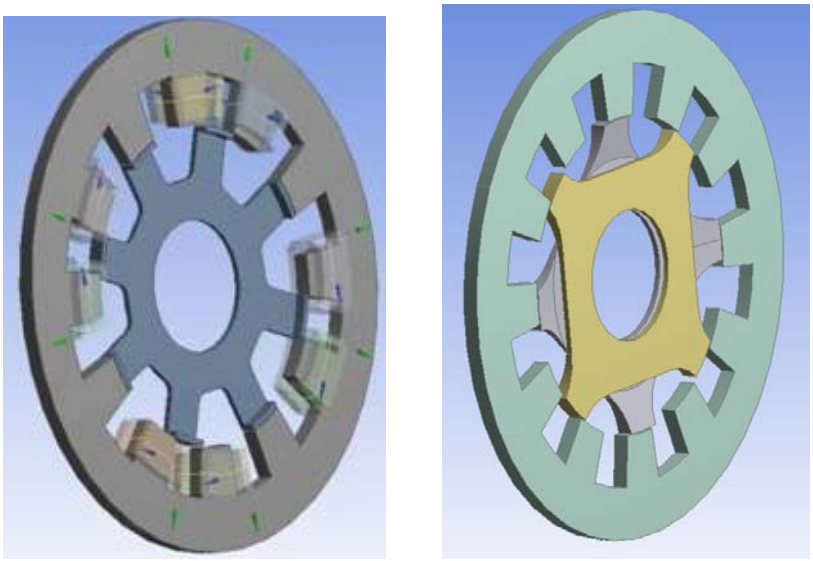

Fig. 5. Infeasible, yet informative applications of lamination taper.

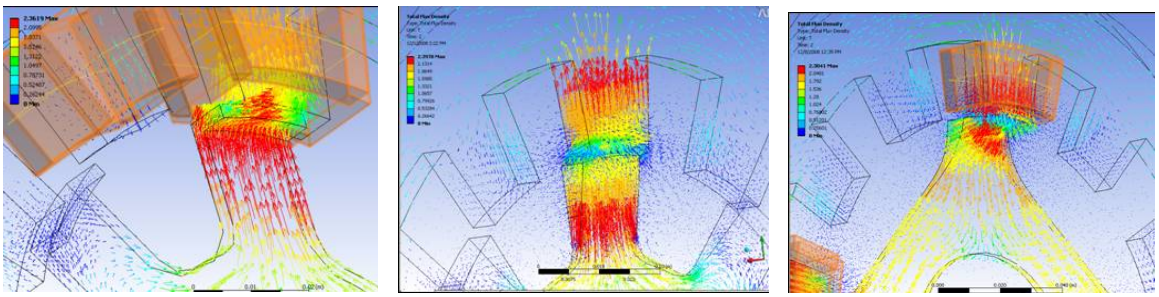

Fig. 6. FEA results from fundamental shape studies.

Separate Laminated Pieces

To reduce the complexity of the design in terms of the approach, simulation, and manufacturability, a wide-ranging evaluation technique was used to assess the various possibilities in which separate laminated pieces (example shown in Fig. 2) could be integrated into novel configurations. Initially, an assessment was made of the various possibilities for laminate piece use in the rotor, as shown in Fig. 7. The configuration shown in Fig. 7 is not entirely feasible but is merely an example of the initial approach. The lack of separation between the eight rotor pieces inherently leads to the presence of flux density in undesired paths, thereby reducing the saliency ratio and overall torque capability of the machine. A series of calculations was made to determine the separation between the pieces for various configurations, and the results are shown in Fig. 8. For the initial approach, the most clearly feasible configurations are a 15-9, 14-8, and 10-6, where the first number indicates the number of stator teeth and the second indicates the number of rotor pieces, where each rotor piece has two teeth. While these possibilities are feasible, there still exists some complexity in the rotor design in terms of manufacturability as well as complexity in the control and winding configuration.

A more appealing approach is obtained when the stator and rotor configurations that were just described are interchanged, as the configurations become an 18-15, 16-14, and 12-10, respectively. In these cases, the rotor is of the same design as a conventional SRM, thereby alleviating concerns for cost, manufacturability, and reliability. A sketch of the 18-15 is shown in Fig. 9, wherein 9 stator pieces have 18 poles and a conventional 15 pole rotor is visible. Figure 10 shows the static torque curves obtained from FEA simulations for half of an electrical cycle. The natural torque production of the machine involves a significant overlapping of torque contribution from each phase. For the configuration in Fig. 10, two phases produce torque for four mechanical degrees (60 electrical), then one phase produces torque for four degrees during its maximum torque zone, then two phases again produce torque for the remaining four degrees. During this half electrical cycle, one phase remains active for the entire region.

All of the machines of this type have torque characteristics similar to those of the 18-15. This approach inherently offers an opportunity to have greater control over torque ripple by means of current regulation. Based on the characteristics of the static torque curves of the initial design, it is apparent that if proper current regulation is applied during dynamic operation, torque ripple can be reduced to very low levels for low and moderate torque production. Although this technique will produce some benefit when applied to conventional SRMs, the inherent characteristics of the novel design approach more readily facilitate torque ripple levels below 5%. This is primarily because there are no zero or near-zero torque positions for the motor, as opposed to most conventional SRMs, which have sharp torque transients that approach zero. It is important to note that the static torque curves shown in Fig. 10 do not truly reflect the torque characteristics of the machine during dynamic operation, wherein inertia and inductance can introduce significant smoothing of the torque profile. More importantly, the design has significant room for optimization in terms of appropriately matching the torque, power, and speed requirements for each application. Additionally, detailed parametric studies will reveal more opportunities to manipulate the torque profile of the machine from a hardware design standpoint. Therefore a dynamic simulator is needed to fully realize all impacts of the design parameters.

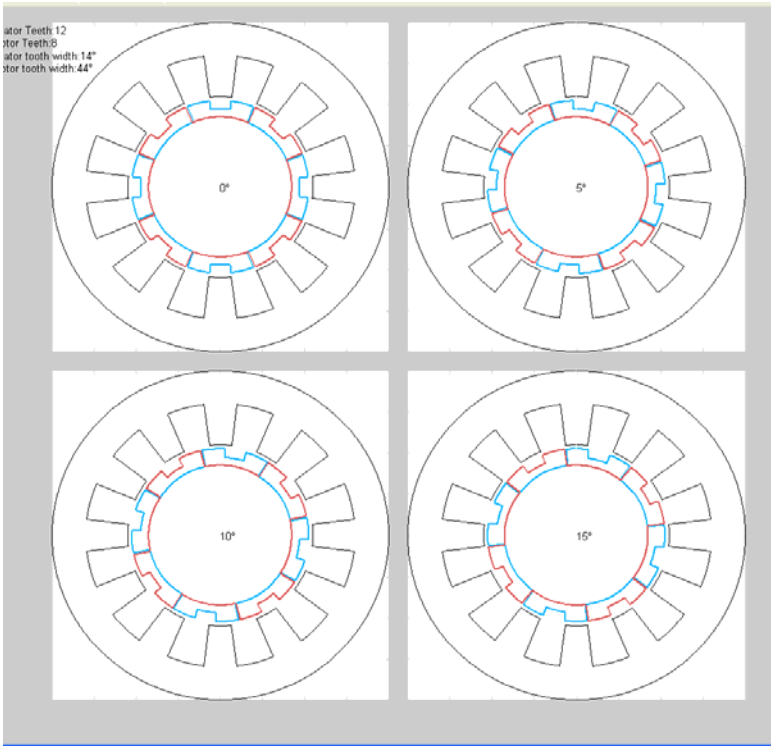

Fig. 7. Inefficient novel SRM with 12 stator teeth and 8 rotor pieces (16 rotor poles).

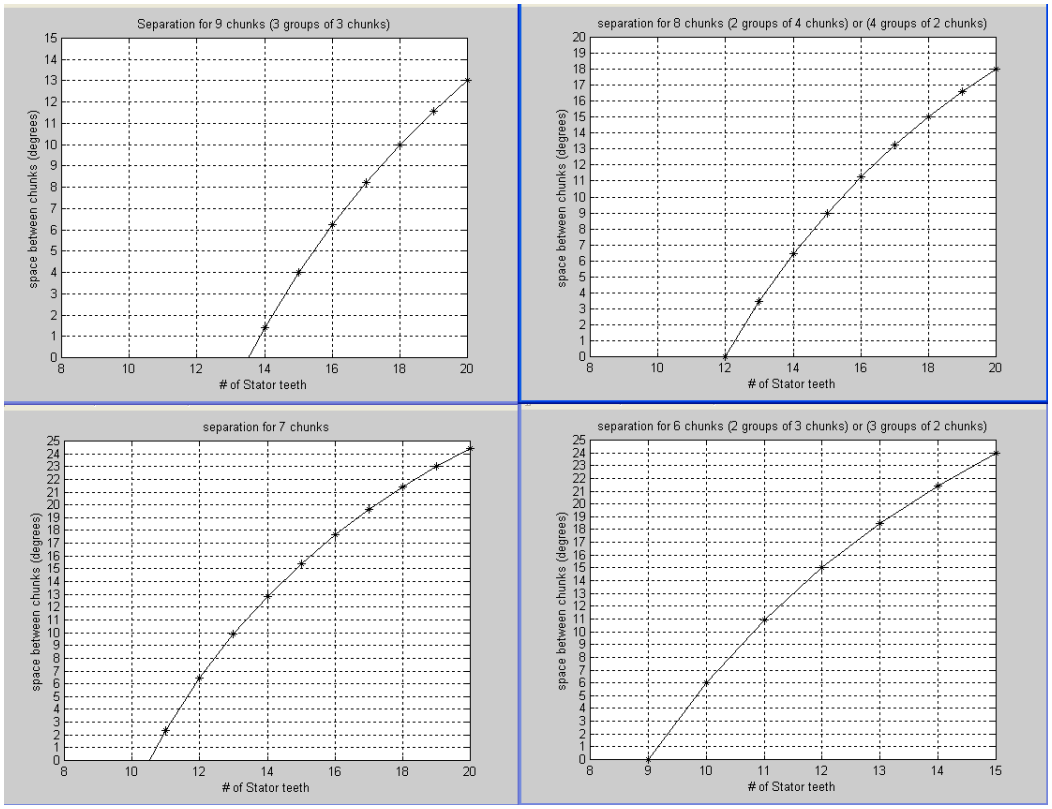

Fig. 8. Possible configurations for initial approach.

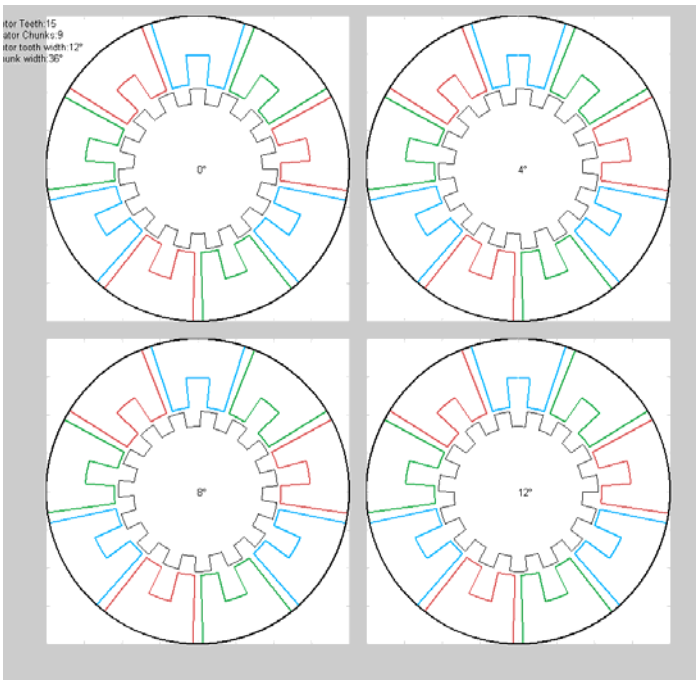

Fig. 9. Initial 18-15 configuration.

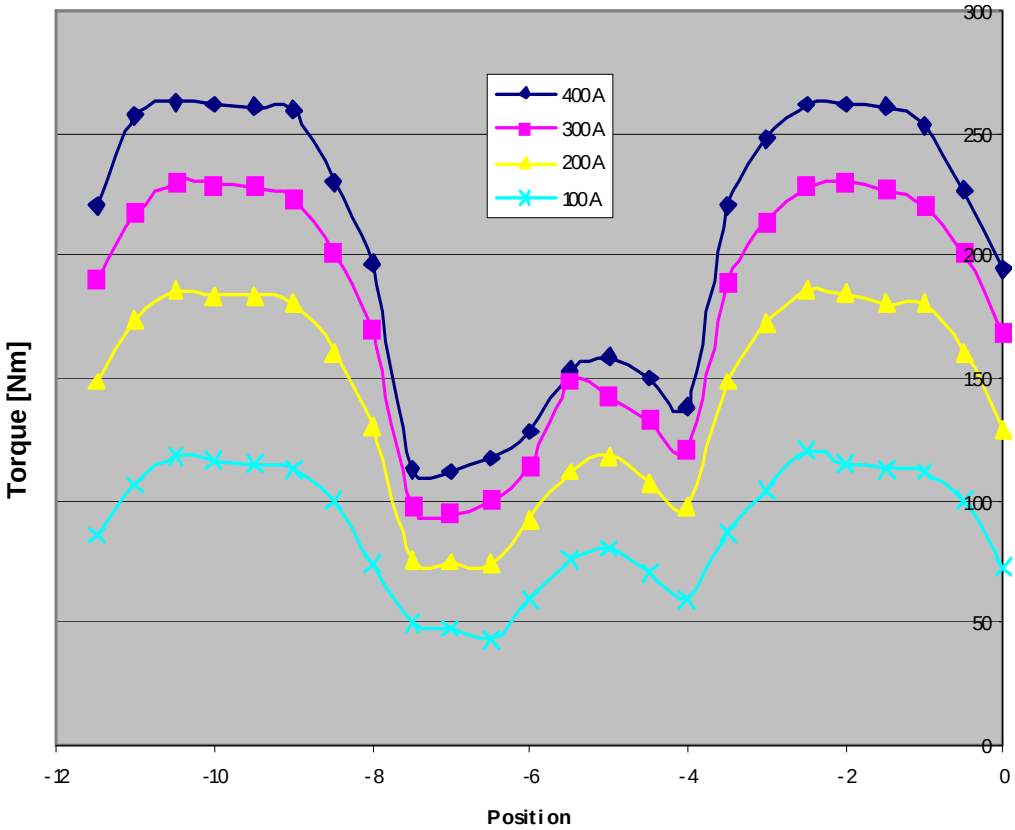

Fig. 10. Locked-rotor torque profile from the initial 18-15 configuration.

Development of Dynamic Simulators

To have the capability to fully assess the overall impact of the variation of a range of design parameters, two separate universal dynamic simulators were developed. The simulators are universal in the sense that they can simulate various motor designs, even other types of motors, with slight modification to the simulator. Having agreeable results from two separate types of simulators ensures that the simulation results are authentic. Otherwise, unacknowledged artifacts within the simulation environment setup could have profound impacts upon the results. One of the simulators carries out the dynamic simulation and corresponding computations within FEA software by accessing the FEA solution database for each iteration and applying the appropriate constraints, constants, and relationships for the transient solution. The other simulator is similar in nature but entails a more parametric oriented approach to the transient solution and relies on parametric data from static FEA solutions. This parametric simulator is particularly useful for optimizing control conditions such as maximum torque per amp, minimum torque ripple, or maximum efficiency. Extensive efforts were made to ensure that the impacts of saturation, mutual coupling, and other interactions between phases were fully realized. It is common for designers to neglect these phenomena, but the acknowledgement of these aspects is particularly important for this novel design approach. Both simulators have the capability to work in various modes such as current, torque, or speed regulated operation such that the simulation is conducted as if the design were in actual operation in a vehicle. Results from the parametric dynamic simulation of one of the preliminary designs are shown in Fig. 11. These curves represent the maximum torque and power achievable for each speed of this preliminary design and control technique, indicating that about 90 kW was obtained at 15,000 rpm. The size of the machine matches that of the Prius, with roughly a 10 in. stator outer diameter and a 3.3 in. stack length. This particular design is well suited for a situation similar to that in the primary motor of the Camry hybrid electric vehicle, wherein a gear reducer is used to increase the torque capability while the high-speed operation results in improved power density. Note that this design has by no means been optimized, nor has the control technique been fully optimized. Nonetheless, these results reveal that this design approach has great potential to offer competitive alternatives to PM machines.

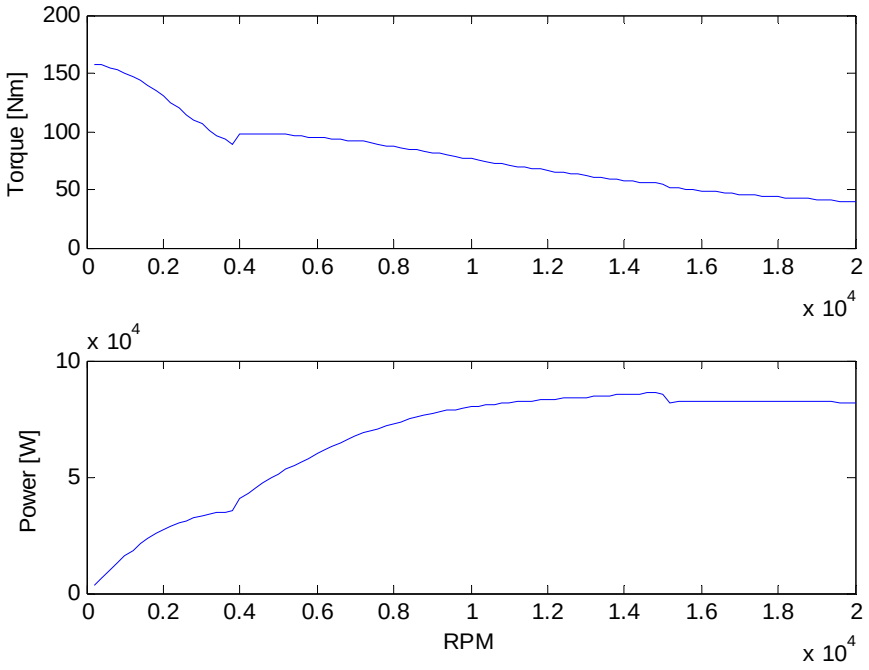

Fig. 11. Torque and power versus speed for preliminary design.

Conclusions

- Maintained low manufacturing and fabrication costs of conventional SRM.
- Maintained robustness of conventional SRM.
- Demonstrated through simulations a significant reduction of torque ripple versus conventional SRM.
- Matched or surpassed performance of conventional SRM.
- Design approach created the opportunity to greatly reduce acoustic noise and vibration from a structural and magnetic standpoint.
- Demonstrated continuous conduction operation.

Publications

None.

References

None.

Patents

None.

3.2 Novel Flux Coupling Machine without Permanent Magnets

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Objectives

- Research the feasibility of an electric motor, without permanent magnets (PMs), that has the potential to replace the internal PM (IPM) motor in hybrid electric vehicles and plug-in hybrid electric vehicles.
- Produce a motor that meets or exceeds DOE's 2020 motor targets for cost, weight, volume, and efficiency.

Approach

Identify the advantages and weaknesses of the most advanced IPM motors available in the market today and use this information to develop a motor which retains the advantages of IPM motors without the use of rare earth PMs.

Major Accomplishments

- Identified the advantages and disadvantages of IPM motors.

  — The following are among the advantages of IPM motors.
    1. They are compact, possessing high power density.
    2. They have good starting torque.

  — The following are among the weaknesses of IPM motors.
    1. Cost. The cost of IPM motors will likely go up due to supply and demand factors impacting the rare earth elements used in the PMs.
    2. Temperature limitations of PMs prevent higher operating temperatures.
    3. Speed limitations. Larger bridges are necessary to maintain mechanical integrity at high speeds. Larger bridges provide a pathway for flux leakage, resulting in poor performance.
    4. Low power factor (pF). This is due to the fixed strength of PMs when operating in a broad speed and load region. This lower pF reduces the power output of the motor at given current and voltage limits. It also increases the load on the power electronic switching devices.
    5. Saturated and unsaturated inductance values of the direct and quadrature axes (Ld and Lq, respectively) change significantly at different loads; thus, fixed PMs are not always optimized for these variable inductance values.
    6. Power levels cannot be increased at higher speeds due to the limitation of PMs under given voltage and current values.

7. The flux field produced by PMs cannot be cut off
   - — To prevent core losses at higher speeds. This also occurs even when the motor is disconnected from the power supply.
   - — To prevent a defective motor's winding short-circuiting (again, this occurs even when the motor is disconnected from the power supply).

- Completed the development of analytical tools used for the design of the Novel Flux Coupling Machine without PMs.
- Completed electromagnetic simulations for motor performance and mechanical finite element analysis for rotational stress loading (80% complete).

Future Direction

- Enhance the design to reduce the size of the motor.
- Analyze the feasibility of incorporating low cost PMs such as Alnico or ferrite. Determine whether these low cost PMs will enhance the motor's capabilities.

Technical Discussion

The following technical discussion shows three dimensional (3D) finite element results and analytical plots obtained through the ANSYS, ANSOFT, ALGOR, COMSOL, and MATLAB software. The analytical equations were derived by ORNL.

Power Factor of Internal PM Motors

There is a common misconception that IPM motor pFs are always high because of the PMs. This misconception can be clarified with an example from classical V-curve theory. Figure 1 shows a set of typical pF curves for different loads of a synchronous motor at different field excitation selected from the horizontal field current axis and from various armature currents indicated by the vertical axis. When the motor has a given field excitation such as a fixed PM excitation selected from the equivalent field current axis, the corresponding pF obtained from the curves would change at different loads. A good 100% pF can be obtained at any load if the field can be adjusted over a sufficiently wide range. For an IPM motor there is always a set of V curves corresponding to each set of given speed and terminal voltages; an optimal pF can be obtained by adjusting the field excitation.

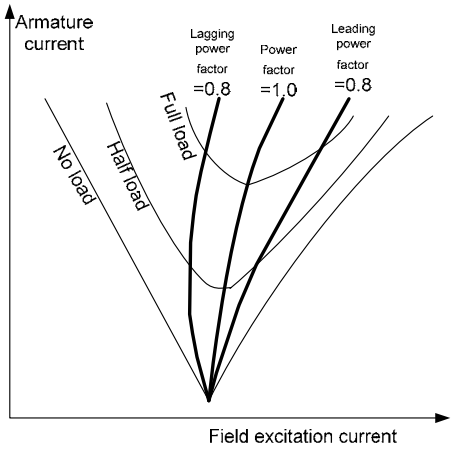


Fig. 1. Classical V curves.

The misconception of a high pF in IPMs can be further clarified through the analytical performance plots of a Camry IPM motor (Fig. 2).

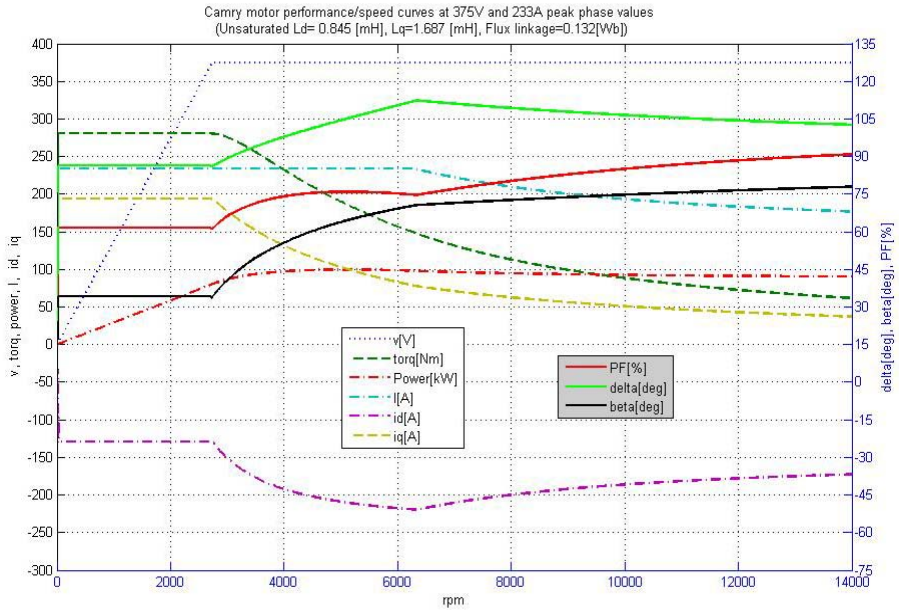


Fig. 2. Camry performance vs speed at 375 V, 233A peak phase values.

Figure 2 shows the Camry motor peak phase voltage (v), motor torque (torq), motor power (Power), peak current (I), direct-axis current (id), quadrature-axis current (iq), pF percentage (PF), load angle degree (delta), and current angle degree (beta) versus motor speed in revolutions per minute. The pF is low (about 62%) from zero to 2,800 rpm. It gradually goes up to about 90% at 14,000 rpm. The peak phase voltage goes up linearly from zero at 0 rpm to the permissible peak value of 375 V at 2,800 rpm and remains at 375 V all the way from 2,800 rpm to 14,000 rpm. The current is at 233 A from zero speed to 6,300 rpm,; after that the current gradually declines to 175 A at 14,000 rpm. The reduction of current at high speeds limits the motor torque and the output power, which cannot go higher than 90 kW at the top speed region. The following section will discuss how this power barrier can be removed.) Figure 2 also shows that the corner point for constant torque is around 2,800 rpm. The power at the corner point is about 70 kW, and the peak power of 100 kW can be obtained at 6,000 rpm.

Advantages of Adjustable Field

Note that the Camry motor performance versus speed curves of Fig. 2 are plotted for a fixed excitation flux linkage of 0.132 Wb, corresponding to the PMs of the motor. The question is, what improvements could be obtained from the motor if the excitation could be adjusted? As stated previously, the reduction of current at high speed shown in Fig. 2 limits the torque and the output power to 90 kW at the top speed region. This barrier could be overcome if the field could be adjusted to a higher value. Figure 3 shows an example of this. At 14,000 rpm, if we fictitiously assume that the field excitation represented by the characteristic current, Ich, can be changed, the best performance corresponds to Ich = 233 A, the corresponding pF reaches 100%, and the output power increases from 90 kW to 130 kW. The characteristic current Ich is defined as “excitation flux linkage”/Ld; therefore, when Ich = 233 A, the excitation flux linkage is 233 × Ld = 233 × 0.845/1000 = 0.197 Wb. This excitation flux is countered by the flux produced by the direct-axis current, id. The resultant flux of these two bucking fluxes prevents the saturation of the mutual magnetic circuit. However, this requires either a set of stronger PMs or a change to a set of stronger wound magnets.

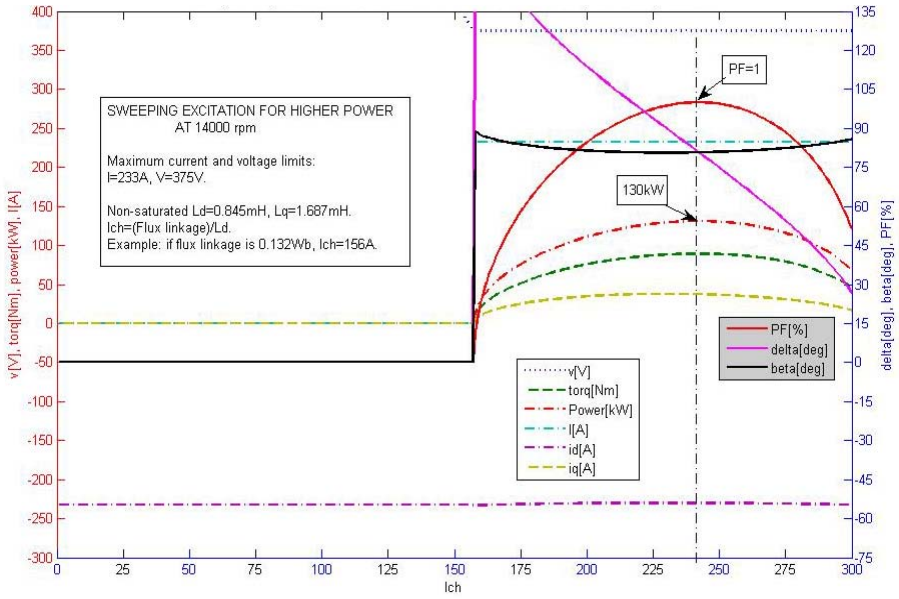


Fig. 3. Sweeping excitation of Camry motor for higher power within current and voltage limits at 14,000 rpm.

Conceptual Geometry of a Novel Flux Coupling Machine without PMs

Figure 4 shows a conceptualization of the Novel Flux Coupling Machine without PMs. It consists of a wound stator core; two stationary excitation toroidal coils; two stationary end brackets that house the bearings; the toroidal coils, which serve as flux paths for exciting the rotor; and a rotor. The rotor is made of lamination punchings, rotor hub, and end plates. There are no PMs in the rotor; the cavities vacated by the PMs are used for locating the mechanical enforcing components. The bridges are narrow for reducing the leakage fluxes. The radial air gap is 0.78 mm per side, and the axial air gap is 1.5 mm per side.

Figure 5 shows that the axial distance between end brackets of the Camry motor is 202 mm. Figure 6 shows the volume comparison between the Camry motor and the concept novel flux coupling motor by placing the latter in the space between the Camry end brackets. There are cross-sectional area deficits for the novel flux coupling motor, indicating the work needed to further reduce the motor's volume. The volume of the motor as currently envisioned is not excessively larger than the Camry motor; however, it would be expected that the motor would be heavier than the Camry motor due to the greater amount of iron in it.

The parts weight of the Novel Flux Coupling Machine is 115 lb. The motor would be heavier than the Camry motor due to the two 32 lb steel end brackets. Thus if the weight cannot be tolerated, the motor must be designed using a low iron approach (i.e., less flux and higher turns of stator winding) and be developed for a higher speed than the IPM motor. Alternatively, a low cost PM-assisted motor could be developed to reduce the weight of the steel end brackets.

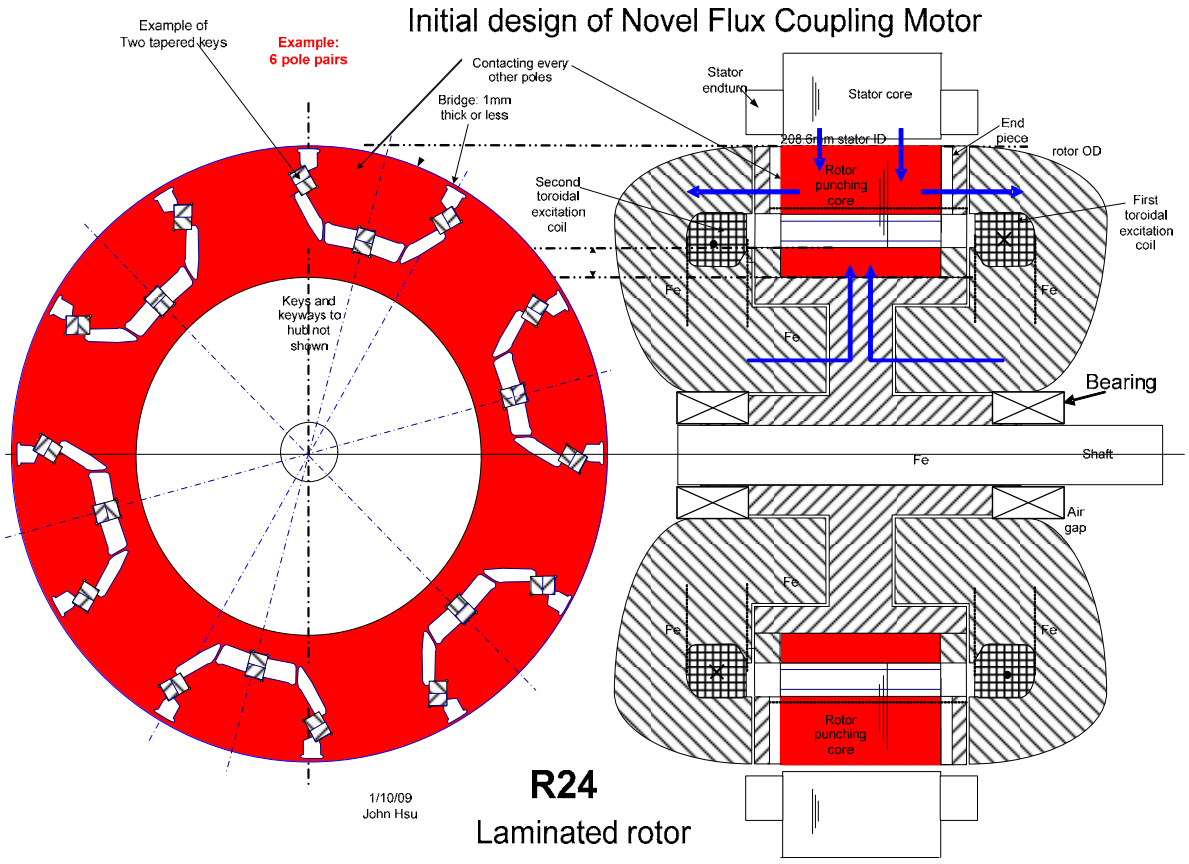


Fig. 4. Conceptual geometry of a Novel Flux Coupling Machine without PMs.

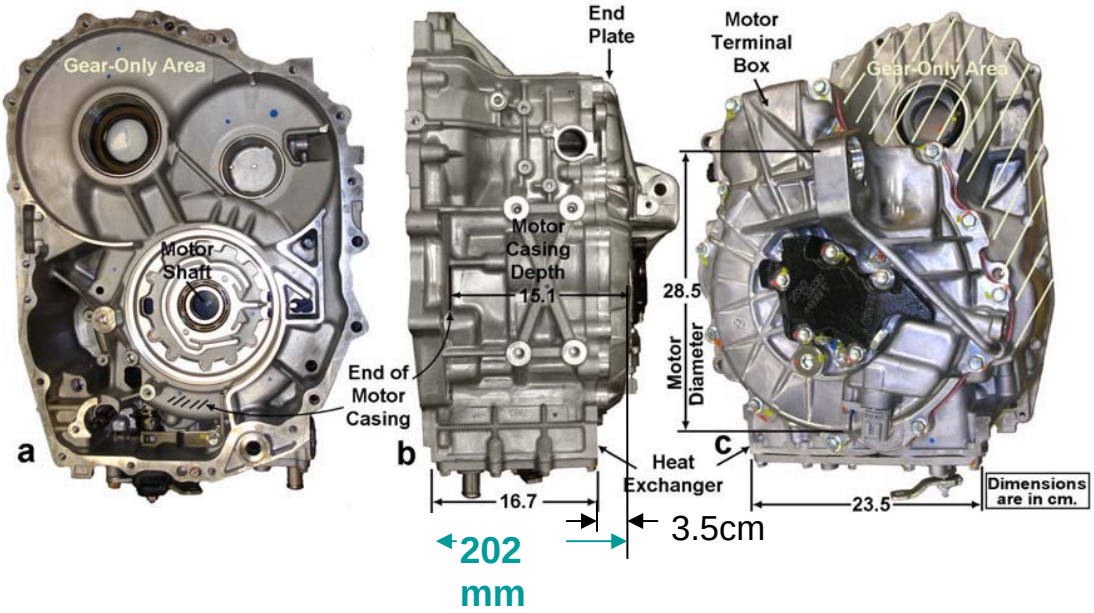


Fig. 5. Axial distance between end brackets of Camry motor.

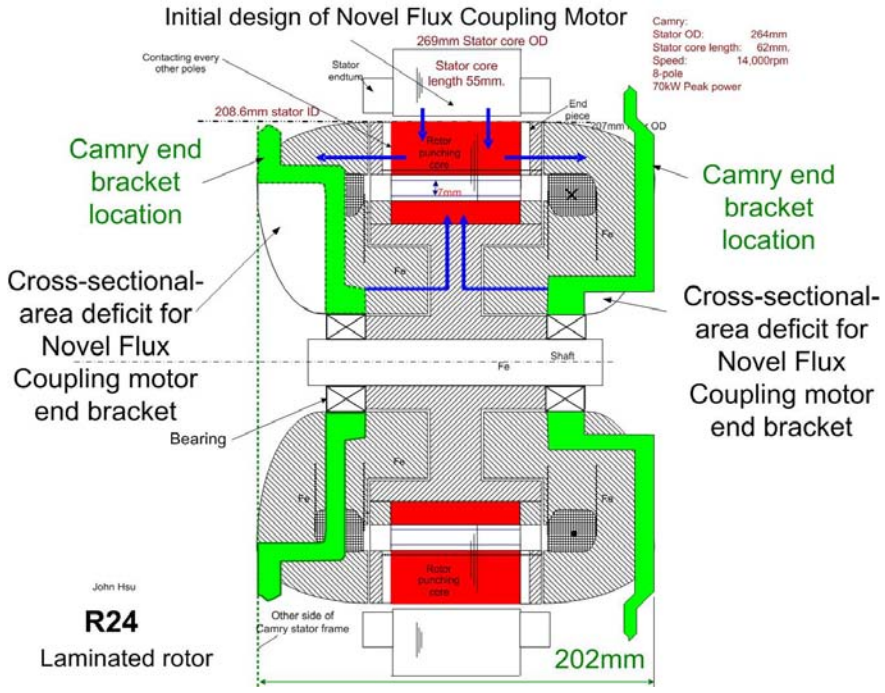
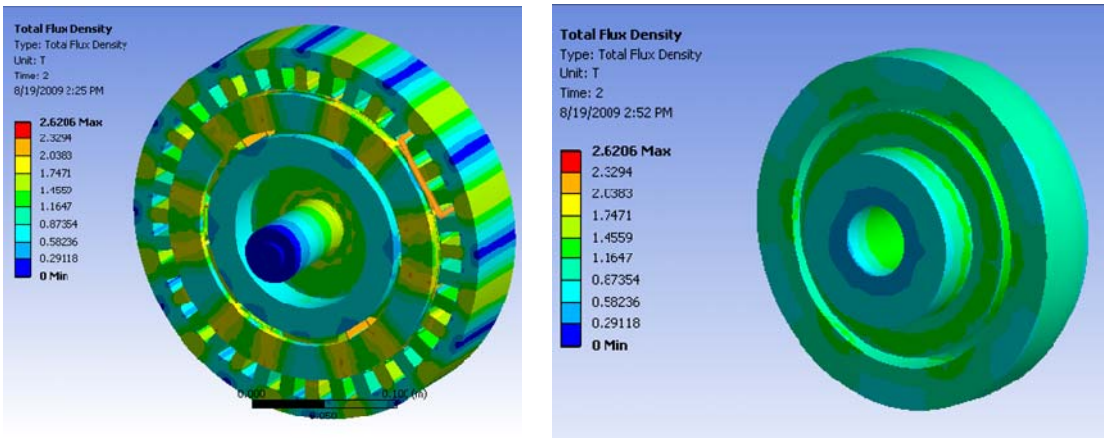


Fig. 6. Volume comparison between Camry motor and the concept novel flux coupling motor.

Electromagnetic Simulation of R24 Novel Flux Coupling Machine without PMs

The current conceptual design revision 24 (R24) Novel Flux Coupling Machine without PMs is a high flux design (or high iron design). As discussed previously, in the final prototype design, a low iron approach may reduce the weight of the iron components. The flux distribution in the rotor and stator computed at 3 A excitation and 50 A stator winding current is shown in Fig. 7.

Table 1 shows a comparison of corner point speeds and motor peak powers for the Camry and the R24 Novel Flux Coupling Machine without PMs. As shown in the table, the peak power of the R24 motor can exceed the peak power of the Camry motor, and it is expected that the specs for the final design will be even better than those shown in Table 1 (and Table 2).



(a) **(b)**

Fig. 7. Flux densities of R24 Novel Flux Coupling Machine at 3A excitation and 50A stator winding. (a) = stator and rotor lamination; (b) = end bracket.

Table 1. Comparison of corner-point speeds and motor peak powers

	Corner-point speed (rpm)	Peak power (Kw)
Camry	4,500 (claimed)	105 (claimed) (disputed to be 70kW)
R24 motor	3,987 Calculated @ 10A excitation	288 Nm*3,987 rpm*2*pi/60 = 120
	5,579 Calculated @ 60% excitation flux	182 Nm*5,579 rpm*2*pi/60 = 106

Excitation Power Required for R24 Novel Flux Coupling Machine without PMs

Table 2 shows the simulated torque of the R24 motor at different stator winding phase currents and excitation currents. During normal operation the excitation current would be around 3 A.

Table 2. Torque Versus Phase Current and Excitation Current

Phase current (Arm)	Excitation current (Adc)	Torque (Nm)
300	10	307
300	3	192
233	5	242
141	10	246
141	3	150

The required excitation power is inversely proportional to the available area of the excitation coil. Table 3 shows two available coil areas; one is a little less than 0.5 $in.^2$, and the second one is slightly less than 1 $in.^2$. The power consumed by the excitation coil at 3A and 200°C is 445 W and 159 W for the two available coil areas, respectively. The R24 motor's efficiency will be reduced by1% during normal operation. For a 100 kW motor, this would be 1 kW. The excitation loss can be significantly reduced if the available coil area can be increased from 0.5 $in.^2$.

Table 3. Excitation current, voltage, and power of R24 novel motor

Available coil area per side (mm)	Net copper area per side (mm^2) (0.8 fill factor)	Resistance[a] of 850-turn coil with 132 mm average diameter	Resistance[a] of coil at 200°C	Voltage at 10A and at 200°C (Vdc)	Voltage at 3A and at 200°C (Vdc)	Power at 3A and at 200°C per coil (W)
16 × 18 (288 mm^2)	230	22.4 (at 20°C)	38.2	382	115	445
25 × 25 (625 mm^2)	500	10.3 (at 20°C)	17.6	176	53	159

[a]Resistance in ohms.

Performance/Speed Curves of R24 Novel Flux Coupling Machine

The following two sets of performance versus speed curves show the differences corresponding to saturated inductances of Ld and Lq at the different flux linkage values that are produced by the adjustable field excitation. Ideally the inductances and the flux linkage values would be simulated for each point of the curves. Unfortunately, it takes more than 10 h to conduct one run for the 3D simulation, and this expenditure of time was not deemed to be justified at this conceptual design stage. To compensate, two excitation flux linkages, 0.132 and 0.09 Wb, were used to see their influences.

Figure 8 shows that when the inductances are saturated and the flux linkage is 0.132 Wb, the maximum power can reach 130 kW at about 5,000 rpm. The constant torque is about 290 Nm. However, the motor cannot operate after 8,000 rpm without exceeding the voltage and current limits of 375 V and 233 A.

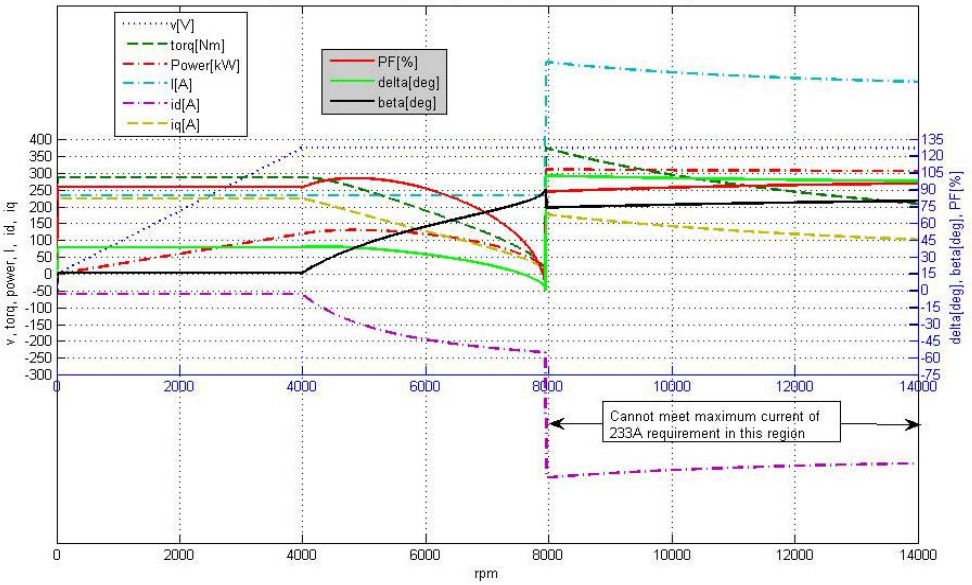


Fig. 8. R24 novel motor performance/speed curves at 375 V and 233 A with Ld = 0.244 mH, Lq = 0.413 mH, and flux linkage = 0.132 Wb.

Figure 9 shows the plots with saturated inductances and a lower excitation flux linkage of 0.09 Wb. The maximum power is about 130 kW at 8,500 rpm. The operation of the motor continues at high speed with higher than 100 kW output power. The constant torque (200 Nm) is significantly lower than the previous plots with higher excitation flux linkages. Comparing Figs. 8 and 9, by reducing the excitation from 0.132 to 0.09 Wb, the operation of the motor can continue at high speed; this illustrates the advantage of the adjustable field provided by the Novel Flux Coupling Machine without PMs.

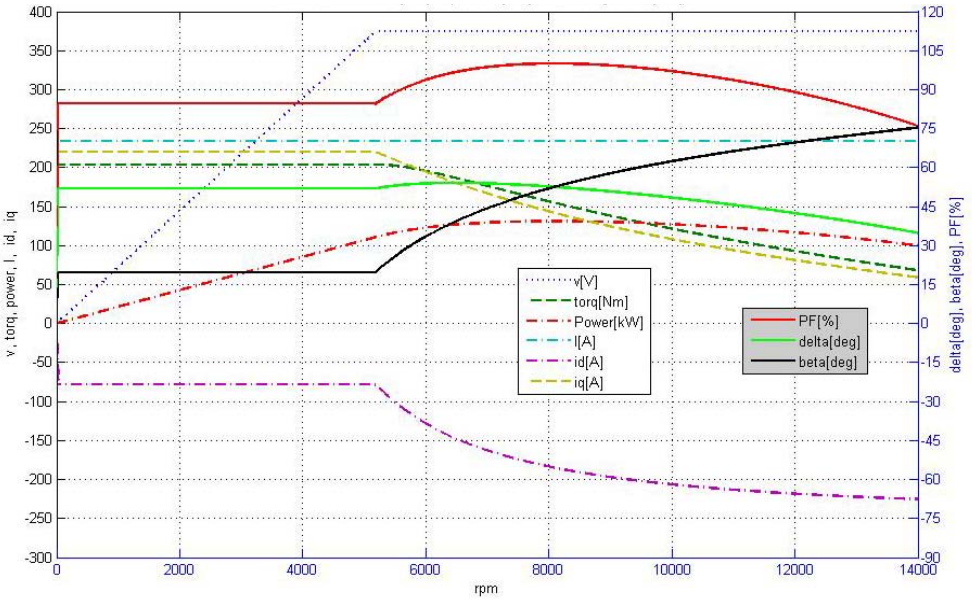
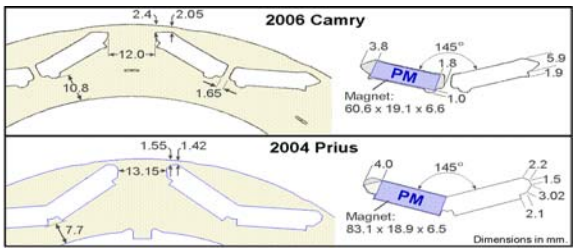


Fig. 9. R24 novel motor performance/speed curves at 375 V and 233 A with Ld = 0.244 mH, Lq = 0.413 mH, and flux linkage = 0.09 Wb.

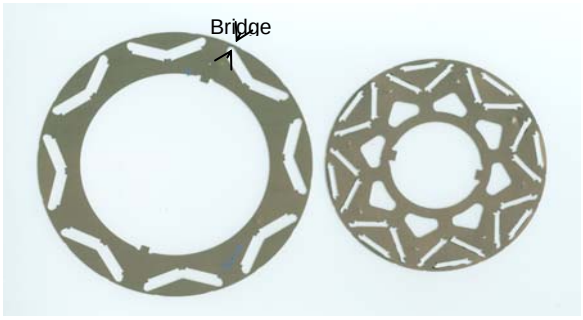
Mechanical Considerations of R24 Novel Flux Coupling Machine without PMs

Before considering the mechanical design of the R24 motor, let us first visit the drawbacks of current IPM motors. The bridge shown in the upper right side of Fig. 10 is used to hold the PMs. As shown in Fig. 10, the bridge thickness is 2.4 mm for the 14,000 rpm Camry, with three bridges per pole, and 1.55 mm for the 2004 Prius, with two bridges per pole. The higher the speed, the thicker the bridge must be for mechanical strength. Unfortunately for magnetic considerations, the thicker the bridge is, the greater the flux leakage between the PMs, thus lowering the performance of the motor. In the R24 machine design, thick bridges have been eliminated. The cavities vacated by the PMs can be used for mechanical reinforcement.

For a given diameter IPM rotor, when operating speed increases more and thicker bridges are required.



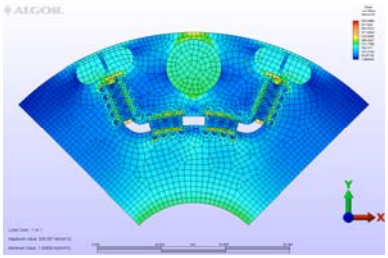
—Higher bridge leakage



Prius (2004)	Lexus (2008)
6,000 rpm	10,400 rpm
6.317 in. dia.	5.082 in. dia.
3.3 in. core length	5.349 in. core length
50 kW max.	110 kW max.

Fig. 10. Bridges of IPM motors.

There are many possible ways to use the cavities vacated by the PMs for mechanical reinforcement. Figure 11 shows one example: using "ziplocks" to link the rotor lamination pieces together. Other approaches such as dovetails, reversed T, keystone, and thread locks are under investigation. Providing satisfactory structural reinforcement while maintaining an easily manufacturable process is a significantly challenging task.



Stress at 20K RPM—530.6 N/mm^2 (77,015 PSI) Containing Ziplock Surface Contacts ONLY

Displacement at 20K RPM—0.07 mm (0.003 in.) Containing Ziplock Surface Contacts ONLY

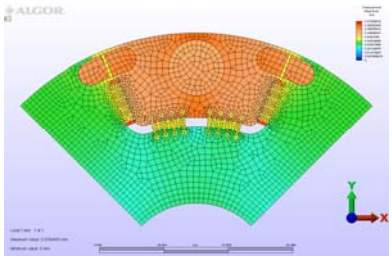


Fig. 11. Stress and displacement of ziplock at 20,000 rpm.

Target Review (Table 4)

Because the Camry IPM motor is close to meeting DOE's 2020 targets (except that the cost, $10.7/kW versus the $4.7/kW target, is high and the permissible temperature rating, 65°C coolant versus 105°C coolant target, is low), we have used the Camry motor as a point of reference for the R24 motor design. The R24 design features removing the rare earth PMs to lower the cost, increasing the motor permissible operating temperature, and increasing the permissible speed for size and weight reduction. With the R24 machine design, the power output of the motor can be higher than that of the Camry motor. Additionally, the permissible temperature can be higher, and the volume is close to the volume between the Camry end brackets. The R24 motor is heavier than the Camry motor because the end brackets are made of iron instead of aluminum.

Table 4. DOE Targets

	Traction drive system					Power electronics				Motor			
	$/kW	kW/kg	kW/L	Efficiency	Coolant temp. (°C)	$/kW	kW/$	kW/kg	kW/L	$/kW	kW/$	kW/kg	kW/L
Camry	36.6	1.2	3.2		65	25.9		4.3	7.1	10.7		1.7	4.73
Camry (est.)	73.1	0.6	1.6	89	105	51.7	0.019	2.2	3.5	21.4	0.047	0.9	2.9
Targets													
2010	19	1.06	2.6	90	90	7.9		10.8	8.7	11.1	0.09	1.2	3.7
2015	12	1.2	3.5	93	105	5	0.20	12	12	7	0.143	1.3	5
2020	8	1.4	4	94	105	3.3	0.30	14.1	13.4	4.7	0.213	1.6	5.7

Summary of FY 2009 Novel Flux Coupling Machine Work

- Computations show the R24 Novel Flux Coupling Machine without PMs has good potential for meeting the DOE 2020 targets.
- Further work remains to reduce the R24 machine size and weight.

Comparative assessment of the R24 Novel Flux Coupling Machine without PMs shows the following.

- Permissible rotor speed can increase without thick bridges for PM retention.
- Permissible temperature can be higher without the limitations of PMs.
- pF and performance can increase with adjustable field control.
- Load can affect Ld and Lq values of IPMs as well as the R24 motor due to magnetic saturation; the adjustable field can help achieve the best performance.
- Motor size is comparable to the Camry motor.
- Mild steel (or equivalent) motor brackets are required, which adds weight to the motor.

3.3 Development of Improved Powder for Bonded Permanent Magnets

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Objectives

- Increase the maximum operating temperature from about 125˚C to 180-200˚C and improve the environmental stability of permanent magnet (PM) materials to enable high volume manufacturing of advanced electric drive motors with improved operating characteristics and lifetime.
- Reduce the overall manufacturing cost of traction motors and enable a new generation of machine designs by developing magnets that can be formed efficiently into net-shapes or molded in-place as motor component assemblies with high magnetic energy density to conserve valuable materials.

Approach

- Develop enhanced control of nucleation and growth of nano-crystalline structure in rapidly solidified magnet alloy powders to reduce processing cost and to minimize annealing requirements.
- Attempt development of anisotropic (aligned cellular or single crystal) magnetic microstructures in particulate of mixed Rare Earth (MRE)-Fe-B alloys to make large gains in bonded magnet properties.
- Explore prospects for anisotropic sintered permanent magnets from the MRE-Fe-B alloys using transient liquid phase sintering or extrinsic additives for consolidation of aligned high strength (fully dense) magnets for high temperatures.
- Implement recommendations from analysis of total manufacturing cost for advanced electric drive motors that called for increased effort on anisotropic particulate for bonded MRE permanent magnets and other RE magnet types, e.g., sintered, which utilized improved tolerance to high operating temperatures.
- Formulate new research thrust on non-RE permanent magnets of sufficient magnetic strength and resistance to demagnetization for vehicle traction motor applications that include high operating temperatures.

Major Accomplishments

- Reviewed recommendations and initiated research emphasis on anisotropic sintered and bonded RE permanent magnets, consistent with the independent analysis that was received of the total manufacturing cost for advanced electric drive motors in appropriately designed interior PM rotor electric machines.
- Developed a milling process for chill cast ingots of MRE magnet alloys that involves hydrogen charging/decrepitation (HD), inert atmosphere (glove box) handling, and conventional ball milling to produce desirable powders for sintering with an average particle size of ~3μm and a reduced oxygen content, allowing excess rare earth in the alloy to be significantly reduced for enhancing the energy product.

- Coupled a new high temperature sintering and annealing process with a previous MRE magnet alloy that was developed for melt spun isotropic magnets, employing chill casting and HD milling, to produce magnets with a density of 7.35 g/cm^3 and an energy product of 25.4 MGOe, demonstrating the importance of achieving LPS conditions, albeit at a high temperature, to achieve enhanced densification and improved magnetic properties.
- Discovered a segregated type of "core-shell" 2-14-1 phase structure upon microstructural examination of the 2-14-1 grains of intrinsic (unmodified) sintered MRE magnet samples (with Y-enrichment as a shell or rim on each grain) that appears to increase the negative temperature coefficient of the magnetic properties of MRE sintered anisotropic magnets, which is a critical problem to solve to make this type of magnet useful.
- Initial results of studies with extrinsic sintering additions showed that Al appears to be the most promising additive when used for controlled solid-state transformation (forming Al-Fe intermetallic phase) bonding at a low temperature (<600˚C) that leaves residual Al phase in the interparticle region, but more work with Al coated magnet particulate or thin Al flake is needed to investigate this concept.
- Concluded from a review of literature that 3 approaches should be pursued for making anisotropic nano-crystalline particulate for high strength anisotropic bonded MRE magnets, including a modified melt spinning method with low heat extraction rate and reduced thickness, a devitrification method that imposes a large temperature gradient on the ribbon during crystallization, and a devitrification method with a uni-axial pressure gradient on ribbon samples during crystallization, with initial experiments in-progress on each.
- Completed plans and submitted invitations to University of Maryland, Brown University, University of Nebraska, and Oak Ridge National Laboratory to attend the first Ames Lab workshop entitled "Beyond Rare Earth Magnets" that will be held on November 5-6, 2009.

Future Directions

- Conduct a special invited workshop to identify productive directions for research in high performance non-rare earth permanent magnets with the planned research team that will lead to development of a detailed action plan for the project.
- Select viable processing approach for anisotropic sintered MRE permanent magnets from either intrinsic or extrinsic sintering methods and demonstrate potential for high-energy product and reduced temperature coefficients for operation up to 200C.
- Compare promising approaches for generating anisotropic nano-crystalline particulate that can be used in anisotropic MRE bonded magnets to decide on top two methods for further investigation and to obtain an estimate of the potential for increased magnetic strength over isotropic bonded magnets.

Technical Discussion

Executive Summary

The efficient use of energy for personal transportation is of prime concern for the Department of Energy. In addition, the Clean Air Act requires the implementation of the best available technology to reduce automotive emissions while promoting efficient use of non-renewable liquid transportation fuels. The work outlined here is aimed at the rapid growth of internal combustion/electric hybrids, plug-in hybrids, and full electric vehicles, powered by batteries or fuel cells, through improvements in the efficiency and durability of electric drive systems, consistent with APEEM program goals. By this means, the use of non-renewable liquid transportation fuels will be greatly diminished or, eventually, completely eliminated.

For FY2009, this project was expected to develop the materials and processes needed to fabricate high performance, RE permanent magnets that can be used for traction motors with an internal PM rotor design. While the APEEM program provided the largest portion of the total funding for this work in

FY2009, the Propulsion Materials program also provided significant support, consistent with the dual research emphasis and potential benefits of the work. To meet performance and cost goals for advanced electric drive motors, it is essential to improve the alloy design and processing of PM powders and the process for producing finished RE magnets, incorporating either direct in-rotor magnet molding or net shape magnet fabrication and insertion of the magnets in each rotor. The fully developed RE PM material must be suitable for elevated temperature (180-200˚C) operation to minimize motor cooling needs, where increased high temperature magnetic performance is a critical advantage over current commercial RE magnet material.

Ames Lab has developed a MRE magnet alloy design for high temperature operation that may be implemented at a first level of advantage with nano-crystalline isotropic flake particulate using conventional isotropic bonded magnet processing methods and a high temperature polymer. A second level of advantage may be realized if this high temperature MRE magnet alloy flake particulate is protected with an oxidation resistant surface coating by a batch process that was developed in this project. A third level of advantage may be realized for isotropic bonded magnets, if the high temperature magnet alloy can be translated successfully to a fine spherical isotropic powder production process based on inert gas atomization with and in situ protective powder coating. This third level of manufacturing advantage is derived from reduced molding pressures and enhanced performance and reliability for isotropic bonded MRE magnets, through increased magnetic powder loading and reduced irreversible magnetic losses from oxidation and corrosion.

According to the recommendations of an industry expert report that was commissioned by this project, anisotropic magnet development of the MRE alloys could provide further advantages over any of the isotropic MRE magnet developments that were cited above. First, if anisotropic nano-crystalline fine particulate can be produced so that polymer bonded MRE magnets can be in-rotor molded and magnetized in-place to the desired field pattern, it should be possible to achieve 4X multiplication of the magnetic torque, compared to similar isotropic bonded MRE magnets. As one of the targets of our current MRE magnet study, these high-energy bonded magnets may be strong enough to meet the 2015 APEEM goals for traction motor volume and weight, along with a significant manufacturing cost reduction and high temperature advantage. Second, if anisotropic sintered magnets can be fully consolidated from aligned micron-sized single crystal particles of the MRE magnet alloy by liquid phase sintering with an intrinsic or extrinsic phase, it should be possible to achieve the same maximum magnetic torque of today's RE sintered magnets, but with a higher operating temperature. As the other target of our current MRE magnet study, these anisotropic sintered magnets with maximum energy product certainly will support the 2015 APEEM goals for traction motor volume and weight, with the added advantage of high temperature operation.

In the final quarter of FY2009, the project was requested to expand beyond the study of RE permanent magnets to take up the search for non-RE permanent magnets that would have sufficient magnetic strength to power advanced traction drive motors for vehicle applications with volume and weight requirements consistent with APEEM goals. The key driver for this new research thrust is the ability to regain free market conditions for magnet component supplies, in contrast to the apparent monopolistic situation for RE supplies. The growing problem with RE availability at an acceptable price is compounded by the many new applications for RE materials, including high demand for RE magnets for electrical generators in wind turbines. Thus, planning was begun for a non-RE permanent magnet research thrust.

Introduction

Rare Earth permanent magnets based on $RE_2Fe_{14}B$ intermetallic compounds, with $Nd_2Fe_{14}B$ as a prototype, have had a large technological impact because of their unsurpassed (demonstrated) magnetic

energy density. Over the past 30 years, extensive research has been performed to develop and improve the magnetic properties and technological benefits of these RE magnetic compounds. Commercially, two classes, anisotropic sintered (microcrystalline) and isotropic polymer bonded (nano-crystalline) $Nd_2Fe_{14}B$ magnets have been successfully developed. It should be noted that anisotropic sintered $Nd_2Fe_{14}B$ magnets are used in current hybrid vehicle systems with interior PM motor designs that require high magnetic torque, but that this magnet class and magnetic torque-dominated motor design have been judged (by at least one of the OEM partners) to be impractical for very large scale mass production at reduced cost. Also, a higher operating temperature was requested for future traction motors (and magnets) to tolerate a planned increase in cooling loop temperature. Thus, the opportunity was recognized to use new motor designs that utilize an enhanced reluctance torque, and, as such, are well suited to the reduced (but still sufficient, potentially) magnetic flux available from anisotropic bonded magnets or sintered magnets, especially if the high temperature tolerance of the MRE magnet alloy could be retained. Because there was uncertainty about the technical feasibility and the total manufacturing cost advantage for the new type of drive motor system from this revolutionary shift in magnet type and motor design, a cost analysis of this situation was commissioned from an industry expert (Dr. Peter Campbell) and the report was obtained at the end of FY2008.

Thus, the Campbell report "System Cost Analysis for an Interior Permanent Magnet Motor" was analyzed and its recommendations were implemented in earnest during FY2009. The report evaluated the range of viable Rare Earth (RE) permanent magnet materials for an IPM motor. The report considered existing RE permanent magnet materials and the effects of possible future developments in this area. Motor costs were estimated for an annual production run of 200,000 units. The analysis considered key processing steps and evaluated alternative magnet shapes. Costs associated with RE permanent magnet raw materials, processing, and motor assembly and manufacturing methods were estimated. Mechanical stresses and thermal requirements were considered in the evaluation. The report found that there are two viable alternatives for IPM motors, which meet the FreedomCar goals. Both of these involve anisotropic magnets and emphasize the significance of the development of magnet compositions with mixed RE (MRE) alloys to give tolerance for high magnet operating temperatures. The first type that was recommended for development is based on conventional anisotropic sintered magnets, but based on our MRE alloy design, while the second type is based on anisotropic bonded MRE magnets. The full report is available from the US Office of Scientific and Technical Information (OSTI) (http://www.osti.gov/bridge/product.biblio.jsp?query_id=0&page=0&osti_id=940187).

Approach

As a result of the Campbell report, research efforts were directed toward anisotropic magnets with efforts focusing on both sintered and bonded magnets. Since the most conventional approach to anisotropic magnets is through the crushing and sintering route, the majority of our initial effort focused on this route. It should be mentioned that sintered magnets should have the highest energy density and that commercial $Nd_2Fe_{14}B$ (2-14-1) magnets in sintered form are used widely in hybrid automobiles, today. The report states that the advantage of sintered magnets made from the new MRE alloys for motor performance could be significant at increased operating temperature. However, the report notes that the current manufacturing processes used for making the sintered magnets and for assembling the motors have room for improvement in terms of efficiency and cost. For Nd-based 2-14-1 sintered magnets, it is necessary to produce single grain particles in the range of 1-3μm, to align and compact them in a magnetic field, locking in the alignment, to densify the compact by liquid phase sintering (LPS), and to anneal the magnet microstructure, maximizing coercivity. Unlike traditional $Nd_2Fe_{14}B$ magnets where a low melting ternary eutectic reaction that involves $Nd_2Fe_{14}B$ and $Nd_{1+\mu}Fe_4B_4$ phases forms a low melting Nd-rich liquid for LPS and provides a non-magnetic grain boundary phase after sintering, there is no low melting reaction in the $MRE_2Fe_{14}B$ system that involves the 2-14-1 phase and is near the stoichiometric composition. Therefore, in order to make LPS for $MRE_2Fe_{14}B$ practical, 1) the composition of

$MRE_2Fe_{14}B$ alloys must be adjusted to promote a sufficient melting reaction, or, 2) some suitable extrinsic sintering aids must added to obtain a liquid phase that permits LPS processing. Alternatively, the report states that anisotropic bonded magnets made from the high temperature compatible MRE alloys could offer a sufficient magnetic energy density and a significantly reduced manufacturing cost, especially if "molding in-place" can be used to form finished rotors. The energy product of an anisotropic bonded magnet can, in principal, be three to four times that of an isotropic bonded magnet. While the energy product of an anisotropic bonded magnet will never be more than 70% of that of an anisotropic sintered magnet, these magnets may offer the most significant advantages in terms of mechanical stability, corrosion resistance, and manufacturing simplicity, i.e., lower cost. In addition they allow much more flexibility in tailoring the direction of the magnetic flux, add to efficient use of the flux. Of course, to produce an anisotropic bonded magnet with greatly enhanced performance, anisotropic nano-crystalline powders of the MRE magnet alloys must be developed that can be used in the bonding process. Recognizing that the challenge of producing such powders has been investigated since the discovery of $Nd_2Fe_{14}B$ magnets, the phase relationships of the new MRE alloys (containing more "heavy" RE elements) may provide some advantage in terms of suppression of the free Fe phase over the previous Nd-based alloys. Thus, the development of anisotropic nano-crystalline MRE-Fe-B particulate also has been pursued during this period.

Results

Fine powder production for sintered MRE magnets

Based on our initial work on isotropic magnet alloys for bonded magnets, the alloy composition $[Nd_{0.45}(Y_6Dy_1)_{1/7*0.55}]_{16.6}Fe_{76.7}B_{6.7}$ (WT212) was selected because of its excellent high temperature properties. This WT212 magnet alloy also lacks Zr and C additions that previously were needed to stabilize a nano-crystalline structure, desirable for bonded isotropic magnets. As described above for Nd-based sintered magnets, the initial stage for production of sintered MRE magnets was the production of 1 to 3 μm powders of the 2-14-1 magnet alloy. The production of fine sized particulate was challenging due to the reactivity of the $MRE_2Fe_{14}B$ material. In contrast to the normal experimental situation, making large quantities of material is much easier than making small gram batches since in a large batch a small fraction of the sample may be sacrificed to clean up the atmosphere in the container. In addition, it was necessary to optimize many factors in the ball milling process to obtain fine particles. Initial experiments focused on conventional crushing and ball milling. Factors such as milling time, ball size and media to material ratio were studied.

The alloy ingots were first crushed into ~5mm chunks then further reduced to an average size of ~75μm using a mortar and pestle in a N_2 atmosphere glove box. The resulting powder was then placed in a ball mill jar in the glove box. This improved process greatly reduced the oxygen content during powder processing. The first ball milling studies were conducted using large balls and resulted in an average particle size for WT212 of 7.2 μm after 70 hr ball milling using large balls. The size was larger than the required size of 3μm single grains for 2-14-1. If the ball milling time was further increased, the distribution of size became narrower. However, the average size was not reduced significantly. Moreover, long term milling times resulted in more contamination. Therefore, studies for optimizing the grinding media size distribution and the ratio of powder to grinding media were conducted.

As the particle size was refined by adjusting the milling parameters, automated optical particle size analysis of milled powders was found to produce ambiguous results. As a consequence, direct observation of these powders by scanning electron microscopy (SEM) was employed to explain the results. These observations revealed that the automated particle analyzer greatly overestimated the actual particle size due to agglomeration of the fine particles into larger clusters. Therefore, only the SEM results are considered to be valid. From SEM micrographs of WT213 powders milled for 18h, the size for primary particles was less than 3μm, although there existed a small number of particles whose size was

larger than 3µm. On closer observation, most of those larger particles were agglomerates of many smaller particles. Therefore, the average size for the sample milled for 18h was ~ 3µm.

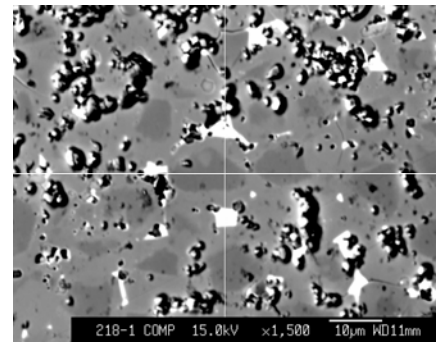
In addition to conventional ball milling, we also studied the use of a much higher energy ball milling process using a SPEX mill. Preliminary particle size analysis results indicated that the average size after milling for 3 and 5 hrs was 14.7 and 15.4 um, respectively. A longer milling time seemed to have resulted in a larger average size, indicating that powder particles are cold-welded together when powder reaches a critical size under the current milling conditions. Cold welded particles would not be single grained and so would not be suitable for our application. However, these SPEX milling results must be only considered as preliminary, since SEM measurements were not conducted to verify the automated particle size analysis results, as discussed above.

Although a grinding procedure using a conventional ball mill had been developed that produced the required size distribution, the oxygen contamination of the samples was higher than desired. In an effort to control oxygen content, the initial coarse grinding was replaced by hydrogen decrepitation (HD). In this process, the ingots were placed in a stainless steel container that was evacuated and filled with hydrogen at a pressure of 3bar. The samples remained under the 3 bar hydrogen pressure for 3-6h. After 4h of HD at 3 bar, SEM examination of the resulting powder showed that the average particle size was less than 20µm. This powder was then transferred to a roller ball mill jar and the jar was filled with cyclohexane or toluene and the grinding medium. This process was performed in a glove box so that the powder was not exposed to air. The post-HD powder was milled in the conventional ball mill for 16h. The average particle size was reduced to ~3µm, as desired. As a result of this process that suppressed RE oxidation and achieved the desired particle size, the amount of excess rare earth in the alloy could be significantly reduced; this in turn resulted in higher energy products due to an enhanced volume fraction of the 2-14-1 phase.

Sintering process development for MRE magnets

Intrinsic sintering: Unlike traditional $Nd_2Fe_{14}B$ magnets where a Nd-rich phase is in equilibrium with $Nd_2Fe_{14}B$ and $Nd_{1+\mu}Fe_4B_4$ phases forming a low melting (650-680˚C) ternary eutectic for LPS and providing a non magnetic grain boundary phase, there is no built in low melting reaction in the $MRE_2Fe_{14}B$ system, as mentioned above. Since the equilibrium phase diagram for the $MRE_2Fe_{14}B$ magnet alloy seems to be dominated by the majority Dy and Y components, the melting behavior of near-stoichiometric alloys, slightly RE-rich, follow the ternary diagram reported for Dy-Fe-B. Thus, DSC measurements, for example, of composition WT220 $[Nd_{0.45}(Y_3Dy_1)_{1/4*0.55}]_{2.8}Fe_{14}B_{1.1}$ revealed two melting reactions with onset temperatures of 725˚C and 1220°C. The 725°C corresponds to the lowest melting reaction in the MRE magnet alloys that involve the RE-rich phase and it apparently is not consistent with an equilibrium phase distribution, while the 1220°C event is the peritectic melting of the 2-14-1 phase. The sintering and annealing temperatures for materials without secondary grain boundary pinning additions, e.g., Zr and C, were determined from these two onset temperatures. In general, the higher the sintering temperature is for this type of near-stoichiometric 2-14-1 alloy, the higher will be the density of the sintered sample, which will have a higher saturation magnetization. However, a higher sintering temperature also may result in larger grains, resulting in a reduction of coercivity. Selection of an optimum annealing temperature (post-sintering) should result in an improved microstructure that further increases coercivity due to stress relief, re-distribution of liquid phase at grain boundaries, and other processes.

Samples for sintering experiments were prepared by aligning and securing this aligned state in the powders in a transverse magnetic field of 1.8 T. In the initial experiments the powders were manually pre-compacted under the field and then further compacted in a hydraulic press after removal from the magnetic field. In later experiments, an apparatus that allowed the hydraulic pressing to be performed in the magnetic field was used. Following alignment and compaction, the pellets were wrapped in tantalum foil and sintered in a high vacuum (10^{-6} torr) furnace that was fitted for sample quenching.



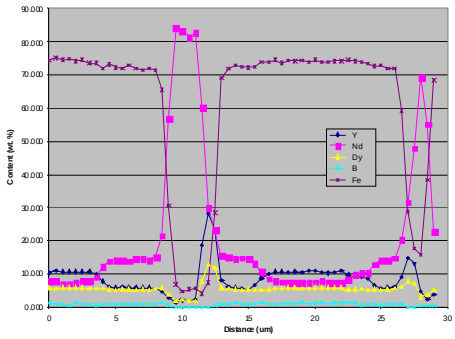


Figure 1. Backscattered SEM image (top) and WDS analysis (white horizontal line) of the sintered alloy WT218.

Initial results of the sintering experiments appeared to be closely linked to the improvements in the process for producing the required 3µm single grain particles, i.e., as oxidation of the powder was reduced the magnetic properties were improved. In experiments conducted after full development of the HD and milling process, two samples of composition WT220 were sintered at 1080°C for 2hrs and 1130°C for 1hr, respectively, and then both were annealed at 650°C for 2hrs. The densities of the two sintered samples were measured to be 7.10 and 7.35 g/cm^3, respectively, where 7.4 g/cm^3 is approximately full density. The higher sintering temperature, 1130°C, resulted in higher M_r (remanent magnetization) and H_c (coercivity), and thus higher $(BH)_{max}$ (energy product) than the sample sintered at 1080°C, i.e., 25.4 MGOe, and 21.9 MGOe, respectively. This suggests that full densification is critical to obtaining the best magnetic properties. Unfortunately, the results for high temperature magnetic properties showed that the sintered samples had higher negative temperature coefficients of remanence and coercivity compared to those of samples of similar composition made by melt spinning. It was also noticed that the sample sintered at 1130°C had greater negative temperature dependence than the sample sintered at 1080°C, indicating that increased density of samples may improve room temperature magnetic properties, but degrade high temperature magnetic properties.

Microstructural examination of the sintered samples (Fig. 1) showed that the 2-14-1 grains have formed a type of "core-shell" phase structure after sintering at 1100-1150°C. In the two types of regions in this structure, Nd-rich 2-14-1 was located at the center as a core, while Y-rich 2-14-1 was located outside as a shell, with the Dy level was constant throughout each grain. Therefore, it appeared that when a uniform compact of $MRE_2Fe_{14}B$ phase grains is sintered at high temperature, segregation of the rare earth elements within each 2-14-1 grain occurs. It was not clear why and how the segregation of the 2-14-1 phase occurred and if it can be suppressed, and this is still under investigation. However, it appeared obvious that increased segregation contributed to a strong negative temperature dependence of the sintered magnets, because Y-rich 2-14-1 located on the outside layer of the 2-14-1 grains would have a lower anisotropic field and result in a lower magnetic field reversal, i.e., coercivity. Consequently, in order to develop sintered MRE magnets with high performance, it is critical to solve this segregation problem.

In order to identify the sources of the segregation, microstructures of compositions over a wide range of MRE-rich alloys; WT218 $[Nd_{0.45}(Y_3Dy_1)_{1/4*0.55}]_{3.5}Fe_{14}B_{1.1}$, WT220 $[Nd_{0.45}(Y_3Dy_1)_{1/4*0.55}]_{2.8}Fe_{14}B_{1.1}$, and WT216 $[Nd_{0.45}(Y_3Dy_1)_{1/4*0.55}]_{2.5}Fe_{14}B_{1.1}$, have been studied. All of the samples exhibited rare earth segregation in the 2-14-1 phase, indicating that the segregation is independent of the RE enrichment. In an additional study, sintered magnets were prepared using a dual alloy approach, where a 2-14-1 alloy with a

ternary combination of rare earths, Nd-Y-Dy, was mixed with a 2-14-1 alloy with a binary combination of rare earths, Nd-Y or Y-Dy. Initial composition profile results within grains and near grain boundaries for sintered magnets made from a dual mixture of ternary Nd-Y-Dy and binary Y-Dy were determined by wavelength dispersive spectroscopy (WDS) and significant segregation was observed in these samples. Further studies are underway to clarify the origin of the segregation and to determine if it can be suppressed.

While studies of the origin of the segregation continue, an alternative approach to the magnet preparation is being investigated in hopes of avoiding the segregation. In this approach, the final composition is obtained by the blending and co-sintering of two types of alloy particles whose average composition is the desired MRE magnet alloy. One of the alloys, $[Y_{0.5}Dy_{0.5}]_{2.5}Fe_{14}B$ (WT231), does not contain a low melting eutectic while the other Nd-rich alloy, $Nd_{10}Fe_{14}B$ (WT232) does. The hypothesis involved in this approach is that the liquid from melting of the Nd rich phase particles will uniformly wet the prior particle boundaries at the temperature of the Nd-Fe-B ternary eutectic. This should provide densification at a significantly lower temperature than our current process. Following densification that was expected to be rapid, diffusion should slowly eliminate the compositional gradients.

Powders of the two alloys were prepared separately using the same casting and HD process described above. The powders were then blended together. Two blended compositions were prepared, one with 10wt% of the Nd-rich alloy and the other with 20wt% of the Nd-rich alloy. The samples were aligned, compacted, and then sintered. The samples were sintered at temperatures of 1100 and 1150°C for 1 hour. Preliminary evaluation of these samples has been completed. Unfortunately, the data indicates that the anticipated densification at lower temperature did not occur and that a sintering temperature of 1150 °C is still required to approach full density. However, the sample sintered at a higher temperature obtains not only a higher density, but also a higher coercivity and lower negative temperature coefficient of coercivity. Further, the sample that contains the 10wt%Nd-rich alloy exhibited a lower H_c but higher B_r and $(BH)_{max}$ than the 20wt% of Nd-rich alloy sample. However, the coefficient of B_r for that sample is also higher, while the coefficient of H_c is slightly lower. The explanation of these results will require further microstructural studies to see if it is useful.

Extrinsic sintering additions: An alternative approach to the intrinsic sintering approach is the addition of an extrinsic sintering aid. Three techniques of increasing complexity are being used to study potential extrinsic liquid phase sintering aids. They are

1. *Liquid phase diffusion couple – Single Interface*
   This technique gave a rapid evaluation of the compatibility of the candidate sintering aid with the magnet alloy, in this case WT-201, $[Nd_{0.45}(Y_2Dy_1)_{1/3*0.55}]_2Fe_{14}B$. A piece of melt-spun ribbon of the proposed sintering aid was placed on top of a polished disk of magnet alloy, sealed in a Ta can and annealed slightly above the melting temperature of the ribbon. The resulting piece was then cross-sectioned and viewed under the SEM with compositional analysis using EDS.

2. *Liquid phase diffusion couple – Double Interface*
   This technique was designed to determine how well the candidate sintering aid wets the magnet alloy. Wetting is required to provide the capillary action that causes densification in LPS. In this case a ribbon of the sintering aid was held between two disks of magnet alloy in a boron nitride clamp. Annealing and analysis was the same as above.

3. *Sintered Compact*
   This is a critical test of sintering. Magnet particulate of less than 45μm in size was mixed with roughly 10-50% by volume of equal sized sintering aid material in a Turbula blending system and

pressed into a pellet. After annealing, the density, magnetic properties, and microstructure of the resulting pellet were determined.

Two types of extrinsic sintering aid candidates were considered with technique 1. The first contained only elements that are present in the parent magnet alloy. Adding these alloys can result in a tailored distribution of phases while reducing the chance of unwanted reactions. We have studied the iron-neodymium eutectic using the single interface method. The eutectic composition was chosen in order to achieve a low melting point. The sample was cross-sectioned and imaged. The compositions of the phases at the interface were studied both in the SEM and with our electron microprobe using WDS analysis that is more sensitive than energy dispersive spectroscopy (EDS). Two primary regions were seen in the region that was molten during annealing. One phase appeared to be an iron-neodymium mixture with a stoichiometry close to Fe_3Nd. Fe_3Nd is not stable in the iron-neodymium phase diagram. However, 3-1 phase is present in the dysprosium-iron system. It is possible that the dysprosium present in the substrate alloy is allowing a 3-1 phase to form. The other phase appeared to be a highly porous Nd eutectic phase mixture, as expected, that was oxidized during polishing. While this alloy appeared promising, it had one significant drawback in the easy oxidation of the Nd part of the eutectic. As in normal Nd-Fe-B, this will result in corrosion problems.

The second type of candidate sintering aids for liquid phase sintering contained elements that are not in the magnet alloy. While this may allow tailoring of the interface, there is a large potential for unwanted reactions. An example of this type of aid is Cu-35.5Zr (wt.%). This alloy is a glass former. It was thought that the corrosion resistance of the glass would provide a good interconnect for the magnet particles. Additionally, Zr is used in magnet alloys in order to refine grain structure. At 885ºC, the melting temperature of this composition is slightly higher than the optimum temperature. Once more the single interface diffusion (method 1) was used. Analysis of the reaction layer (Fig. 2) showed a considerable amount of nearly pure iron surrounded by a neodymium copper mixture. Zirconium was only present in the surface layer (~25µm). Using WDS measurements the phases were more accurately described. Copper was seen nearly 80µm from the surface, indicating significant diffusion into the magnet material. While the copper did not appear to become a part of the matrix, the rare-earth/iron/boron ratios appeared to change in the region of Cu diffusion. This region changed from a $RE_2Fe_{14}B$ phase to a RE_2Fe_{17} phase. Near the interface, the presence of ZrB_2 explained this transformation. Due to these reactions, this alloy was not feasible to use as a sintering aid. However, similar alloys may still be used.

Figure 2. SEM Image of Cu- 35.5% Zr interface with $RE_2Fe_{14}B$ magnet alloy.

Another attractive extrinsic sintering aid prospect is aluminum, which is simple to incorporate as a particulate in a blended sample or allows the possibility of individually coating each magnetic powder particle using well-established industrial processes. Al also offers the prospect of either a transient liquid phase sintering process that stops when the Al is completely consumed by interparticle compound formation or an activated (exothermic) solid-state sintering process at lower temperatures that can leave residual Al as a ductile interparticle phase. In the initial investigation to determine the reaction temperatures of Al with our alloy, a sample was sintered in our differential scanning calorimeter (technique 3). A 50:50 (% by volume) mixture of MQP-11-HTP magnet alloy flake particulate and

aluminum powder was pressed and placed in the DSC. The sample was ramped to 700°C and cooled back to room temperature. Two exothermic reactions were observed. The first, milder, reaction started at 570°C and a second, more intense, reaction started at 638°C. Both reactions appeared to be irreversible. In a second experiment a sample was pressed and taken to 598°C. Both samples were crushed and x-ray diffraction patterns were obtained. In the sample ramped to 598°C, the phases $RE_2Fe_{14}B$ and α-Al can be seen. While in the sample taken to the higher temperature, $RE_2Fe_{14}B$ and $NdAl_8Fe_4$ are observed. It appears that the higher temperature reaction is a liquid state reaction that complete consumes the Al, while the lower temperature reaction is a solid-state reaction, as expected. SEM analysis using EDS confirmed the above results with the additional finding that the low temperature (solid-state) sintered sample also showed presence of the phase Al_3Fe.

A double interface diffusion couple (technique 2) between Al and WT201, a simple stoichiometric Nd-based 2-14-1 magnet alloy, was made to test the low temperature (diffusion rate) limit of the solid-state reaction to determine if it was suitable for interparticle bonding without complete Al consumption. The diffusion couple was prepared by placing a piece of Al foil between two polished wafers of a drop-cast and annealed ingot of the magnet alloy. The assembly was placed in a boron nitride clamp. The diffusion couple was heat treated in a vacuum furnace which was ramped to 572°C and then quenched. The diffusion couple was then sectioned and polished, then submitted for electron microprobe (WDS) analysis. Line scans across the interface are currently being analyzed.

In further studies of aluminum as a sintering aid, magnet powders of MRE-based compositions $[Nd_{0.45}(Y_2Dy_1)_{1/3*0.55}]_{2.5}Fe_{14}B$ and $[Nd_{0.45}(Y_2Dy_1)_{1/3*0.55}]_{2.8}Fe_{14}B$, with higher RE content, were prepared by hydrogen decrepitation of strip cast alloy, followed by ball milling in cyclohexane. The average particle size of the milled powder of both alloys was approximately 3μm. The particulate of composition $[Nd_{0.45}(Y_2Dy_1)_{1/3*0.55}]_{2.5}Fe_{14}B$ was dried in a low vacuum environment and mixed with 10 vol.% gas atomized (high purity) Al powder (dia.<10μm) in a Turbula powder mixing system. The resulting blended sample was aligned and pressed into a dense compact in a magnetic field of 1.5T. For comparison, a second sample of the RE-enriched, $[Nd_{0.45}(Y_2Dy_1)_{1/3*0.55}]_{2.8}Fe_{14}B$, particulate, without an Al addition, also was aligned and pressed into a dense compact in a magnetic field of 1.5T. The resulting pellet of composition $[Nd_{0.45}(Y_2Dy_1)_{1/3*0.55}]_{2.8}Fe_{14}B$ was sintered in a vacuum furnace at 1130°C for one hour then quickly removed from the heating zone. The pellet of blended composition $[Nd_{0.45}(Y_2Dy_1)_{1/3*0.55}]_{2.5}Fe_{14}B$ + Al was sintered with the extrinsic sintering aid in a vacuum furnace at 580°C for one hour and slowly cooled. The magnetic properties of the aligned and sintered magnets were measured parallel and perpendicular to the alignment direction. The intrinsically sintered sample showed good room temperature properties, typical of similar unannealed samples. However, the low temperature extrinsically sintered compact displayed soft magnetic properties.

One obvious reason for the apparent lack of retained anisotropy was the very limited distribution of the relatively large Al powders in the aligned and pressed sample and the planned avoidance of the Al melting excursion. The lack of Al melting probably limited the possible bonding (solid-state phase transformation) reaction to a very small fraction of the available 3μm magnetic particulate in the compact. Thus, when exposed to a reversed magnetic field in the SQUID magnetometer, the unbonded particles may have simply shifted position, losing the initial aligned orientation and exhibiting a soft magnetic behavior. While detailed studies of the extrinsically (Al aided) sintered sample is underway to verify this mechanism, further plans were set in motion to perform an improved test of the solid state sintering approach assisted by the Al (extrinsic) addition. It was decided to pursue physical vapor deposition (vacuum) coating of magnetic alloy particulate with Al to ensure availability of the Al phase on all surfaces during the solid-state reaction and to try the technique 3 test again, using a similar low sintering temperature. This improved initial condition should also permit the low temperature bonding procedure to be tested for its capability to produce smooth 2-14-1 phase grain boundaries for enhanced coercivity.

Particulate production for anisotropic MRE bonded magnets

In preparation for beginning efforts to produce anisotropic powders for bonded magnets an extensive review of the literature has been undertaken to identify what has been tried and what is known about the formation of anisotropic powders. Four different approaches have been tried previously to produce anisotropic powders. The only method currently employed to create anisotropic particulate on a commercial basis is known as the HDDR (hydrogenation, decomposition, desorption, recombination) process. It involves exposing a chill cast ingot of magnet material to an elevated pressure hydrogen atmosphere at high temperature, followed by evacuation and a diffusion anneal. While this produces anisotropic powders, they have extremely poor thermal stability and high (negative) temperature coefficients of coercivity and remanence. Other researchers have considered methods of improving this stability, but HDDR powders also exhibit poor environmental stability. Magnequench also produced commercial anisotropic magnet powders in the past by reprocessing scrap bulk isotropic (fully crystallized) magnets by a hot open die forging method. However, this process for making "MQ-III" particulate was only viable when their production process yielded large numbers of scrap magnets, a highly undesirable situation. The most desired powder for anisotropic bonded magnets would consist of polycrystalline particles of 30-50μm size that each contain crystallographically aligned 200nm grains. While it is possible to produced texture ribbons by controlling rapid solidification, the typical grain size is larger than acceptable for coercivity.

In 1987, Dadon et al. [1] determined that by melt spinning onto an uncooled copper wheel rotating at 19m/s, a large degree of anisotropy could be created. The wheel side of the ribbon exhibited significant texturing, with the c-axis of the 2-14-1 grains perpendicular to the surface. These grains were very small at the surface. Near the center of the ribbon, the grains grew and maintained anisotropy, but were greatly increased in size. Unfortunately, the solidification beyond the central zone, commonly called the "free" (unchilled) side resulted in equi-axed (unaligned) grains. The origin of the extended texture that grew beyond the chilled (wheel side) surface was later attributed by Kramer and McCallum [2] as a secondary nucleation effect induced by a fine distribution of α-Fe phase. Unfortunately these materials have very low coercivity that is attributed to the relatively poor alignment and large grain size of the overall (through-thickness) microstructure for this rapidly solidified ribbon material, producing strong coupling between grains. Since the grain size is significantly below that of sintered magnets, this suggests an approach aimed at modifying the grain boundary phases to stabilize extended growth of fine aligned grains may work, along with promoting thinner ribbons. From this motivation, a modification of the conventional melt spinning approach, away from extremely rapid solidification, was attempted, involving use of a modified quench wheel surface to reduce thermal conductivity, but to maintain high wheel speeds. Microstructural and magnetic analysis of the resulting ribbon particulate from the initial experiments is in progress to determine the prospects for this approach.

Various attempts at inducing texture during solid-state crystallization (devitrification) of ribbons in the amorphous state also have been tried. Basically, a unique crystallization direction must be defined during growth of the crystal embryos in an "over-quenched" ribbon, contrary to the typical isotropic crystallization annealing process. Two new approaches that may be investigated are crystallizing in a magnetic field or under an applied temperature gradient. At the beginning of this project, a collaboration with Argonne National Lab was formed and attempts were made to anneal amorphous ribbon samples in an applied field of 8T. Unfortunately, the crystallization temperature is well above the Curie temperature and so that the magnetic force available for grain alignment from the external applied field was very low and no significant texture was observed. This also was attributed to the existence of randomly oriented crystalline embryos in the as-quenched material, which appear to be very difficult to eliminate. The imposition of a large temperature gradient on the ribbon during crystallization may also lead to anisotropic material; however, a large temperature gradient is difficult to achieve across a thin ribbon, but

may be possible in the 2-14-1 phase due to its very poor thermal conductivity. Methods involving radiant heating and forced cooling are being considered.

At the current time, experiments also have begun where amorphous precursor ribbon samples are crystallized under uni-axial pressure. Based on the work of W. Barclay Kamb [3], the favored crystallization and growth directions should be the directions with the highest elastic constants. In the case of $Nd_2Fe_{14}B$, these directions are the 110-type directions. Starting amorphous ribbon material of $Nd_2Fe_{14}B$ + 3% TiC that was melt-spun at 25 m/s in 1/3 atm. of He was selected for the initial test of the pressure induced anisotropic growth concept in a magnet alloy that should suppress effectively the formation of random crystal embryos. Differential scanning calorimetry was performed on the resulting ribbon and a strong crystallization peak was observed. Based on the data gathered from the DSC, a small amount of the ribbon was annealed in a vacuum furnace at 625°C for 12 minutes under a 10^{-6} Torr atmosphere in order to crystallize the sample. X-ray diffraction was conducted on both the annealed and as-spun samples. The as-spun ribbon showed no significant crystallinity, while the annealed sample showed well-crystallized material. Studies of crystallization under uni-axial stress now will be undertaken on these samples.

Studies of the factors that control grain growth and grain morphology are continuing in order to gain an understanding of how to produce gain aligned nano-grained magnets. Annealing experiments with holding times from 0-11 min were chosen for an isothermal study to slow the diffusion kinetics and to probe the phase evolution to the thermodynamically stable phase field. The analysis of the atom probe tomography (APT) results on ribbon sample of WT147 melt-spun at 25m/s and then annealed at 638˚C for 8 min. using DSC gave clear information about the local microstructure and chemical information along grain boundaries, as reported previously. The nominal composition of the WT147 alloy is $[(Nd_{4.5}(Y_2Dy_1)_{1/3*0.55})_{(2.3-y)}Zr_{0.3}Co_1Fe_{13}B]_{1-2x}+Zr_xC_x$, x=0.01, y=Zr. We found that Zr, C, B and RE are enriched and that Fe and Co are depleted within a 10nm region at the grain boundary indicating the second phase on the boundary is already formed after the 8 minute anneal. In order to gain further understanding of the devitrification behavior of the elements at the initiation of the nucleation stage, samples annealed for 2 minutes were chosen for investigated using both TEM and APT (atom probe tomography, with a 3DAP, LEAP 3000Si) techniques. The annealing temperature was chosen based on DSC analysis (20 ˚C below the onset of the first crystallization event in the DSC). The annealing of these samples has been completed and the preparation of TEM and APT samples is underway.

Conclusions

An independent analysis was received of the total manufacturing cost for advanced electric drive motors. Based on the recommendations, the project research emphasis was focused on anisotropic sintered and anisotropic bonded MRE permanent magnets with capability for high temperature operation. To enable anisotropic sintered MRE magnet development, the processing steps needed to make particulate with an average particle size of ~3µm and a reduced oxygen content were developed, allowing excess rare earth in the MRE alloy to be significantly reduced to reduce alloy cost and to help enhance final energy product. In subsequent progress, a new high temperature sintering and annealing process was developed specifically for MRE magnet alloys that produced sintered anisotropic magnets with a density of 7.35 g/cm^3 and an energy product of 25.4 MGOe, about 5X stronger than isotropic bonded MRE magnets. Unfortunately, the high sintering temperatures developed for intrinsic consolidation/densification of the MRE magnet alloys also were discovered to produce a deleterious “core-shell” segregation pattern in the 2-14-1 phase grains in the finished magnets with Y-enrichment around the rim of each grain. This RE segregation tendency appears to increase the negative temperature coefficient of the magnetic properties of these MRE sintered anisotropic magnets, which is a critical problem to solve to make such magnets useful. Alternatively, preliminary results indicated that Al is a promising extrinsic sintering aid, especially if used for controlled solid-state transformation (forming Al-Fe intermetallic phase) bonding at

a low temperature (<600˚C) that leaves residual Al phase in the interparticle region. To enable anisotropic bonded MRE magnet development, a review of literature revealed that 3 approaches should be pursued for making anisotropic nano-crystalline particulate. These approaches include a modified melt spinning method and two devitrification methods that use either a large temperature gradient or a uni-axial pressure gradient on ribbon samples during crystallization. Preliminary experiments with these approaches were conducted and analysis is in-progress. In response to a request to initiate a new research thrust that goes beyond rare earth permanent magnets, prospective partners were selected and a workshop was organized at Ames Lab to be held on November 5-6, 2009.

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3. Y. Q. Wu, W. Tang, M. J. Kramer, K. W. Dennis, N. T. Oster, R. W. McCallum, I. E. Anderson, *Correlation of the energy product with evolution of the nanostructure in the Y,Dy,Nd-(Fe, Co)-B magnetic alloy*, Journal of Applied Physics (2009), 105(7, Pt. 2), 07A720/1-07A720/3.

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Patents

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3.4 Scalable, Low-Cost, High Performance IPM Motor for Hybrid Vehicles

GE - DOE Cooperative Research Agreement DE-FC28-07NT43122

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Objectives

Electric drive systems, which include electric machines and power electronics, are a key enabling technology for advanced vehicle propulsion systems that reduce the petroleum dependence of the transportation sector. To have significant effect, electric drive technologies must be economical in terms of cost, weight, and size while meeting performance and reliability expectations.

The objective of the GE Global Research "Scalable Low-Cost, High-Performance IPM Motor for Hybrid Vehicles" program is to develop a higher power density IPM motor at a lower cost. Successful completion of this program will accelerate the introduction of hybrid electric vehicles into the U.S. road vehicle fleet and bring the added benefits of reduced fuel consumption and environmental impacts.

(A) Motor Development

- Phase I: Develop advanced motor concepts including electromagnetic, mechanical, and thermal concepts.
- Phase I: Build proof-of-principle machines to verify the design process as well retire the key risks.
- Phase II: Design and build 55kW/30kW machines that meet the DoE specifications
- Phase II: Develop cost model to estimate the advanced IPM motor based on 100000 units/year
- Phase II: Investigate the scalability of the developed concepts by building and testing a 120kW/65kW machine

(B) Materials Development

- Phase I: Demonstrate high resistivity soft magnetic material with resistivity 3X silicon steel
- Phase I: Demonstrate high resistivity permanent magnet materials with resistivity 3X sintered NdFeB
- Phase II: Demonstrate scalable processing of high resistivity permanent magnet and determine cost advantage

Approach

(A) Motor Development

- Simplified stator windings will reduce end-turn length and losses, together with motor mass and volume and manufacturing cost.
- Advanced rotor concepts to achieve higher power density as well as meeting the high-speed requirement.
- Advanced scalable thermal management schemes for both the stator and the rotor to meet the required set of specifications.

(B) Materials Development

- Phase I: Warm extrusion of bulk metallic glass-based composites to form high resistivity composite microstructure
- Phase I: Co-sintering of permanent magnet and high-resistivity phase to achieve novel high effective resistivity microstructure
- Phase II: Co-sintering process improvements to enhance reproducibility and scalability of high effective resistivity microstructure

Major Accomplishments

(A) Motor Development

- 2 rotor & 2 stator electromagnetic (EM) concepts developed & analyzed in detail
- Scalable rotor and stator cooling concepts selected to meet performance, simplicity and scalability requirements
- Highest-performance EM concept selected for proof-of-principle motor build.
- Machine built and testing is almost finished
- Build of second machine (different rotor structure) is initiated and expected to be finished by end of 2009 or early 2010
- Development of cost model is initiated and expected to be finished by end of 2009 or early 2010

(B) Materials Development

- Phase I: Bulk metallic glass soft magnetic composite > 1 mm thick, 2X resistivity of Silicon steel, and saturation magnetization of 1.3 Tesla
- Phase I: Co-sintered permanent magnet with effective resistivity 3X sintered NdFeB with 5-10% reduction in energy product

Future Direction

(A) Motor Development

- Phase II: Concluding the testing of the second proof-of-principle machine
- Phase II: Testing the second proof-of-principle machine with a different rotor concept
- Phase II: Down selecting a rotor concept based on test results of both machines
- Phase II: Design and build the third 55kWpk/30 kW IPM machine that will be delivered to the DoE for verification.
- Phase II: Develop cost model based on 100000 units/year

(B) Materials Development

- Phase II: Improve co-sintering of high resistivity sintered magnets process to enhance reproducibility and improve scalability
- Phase II: Materials selection study of structural and magnetic components of rotor and shaft assembly

Technical Discussion

(A) Motor Development

After the concept for the proof-of-principle (PoP) machine was down-selected, the design of the PoP machine was finalized and the machine was built. The PoP machine has many novel features including novel simplified stator structure, novel rotor structure to be able to run the machine at 14000 rpm while achieving the required torque density, and novel thermal management scheme. Figure 1 shows the test setup of the PoP machine. The machine is heavily instrumented with thermocouples and RTDs for measuring stator temperatures and calirometric measurements as well as a pyrometer for measuring the rotor temperature. The setup is also equipped with a flowmeter 9to measure coolant flow rate), pressure transducers (to measure coolant pressure), accelerometers and proximity probes for measuring vibrations.

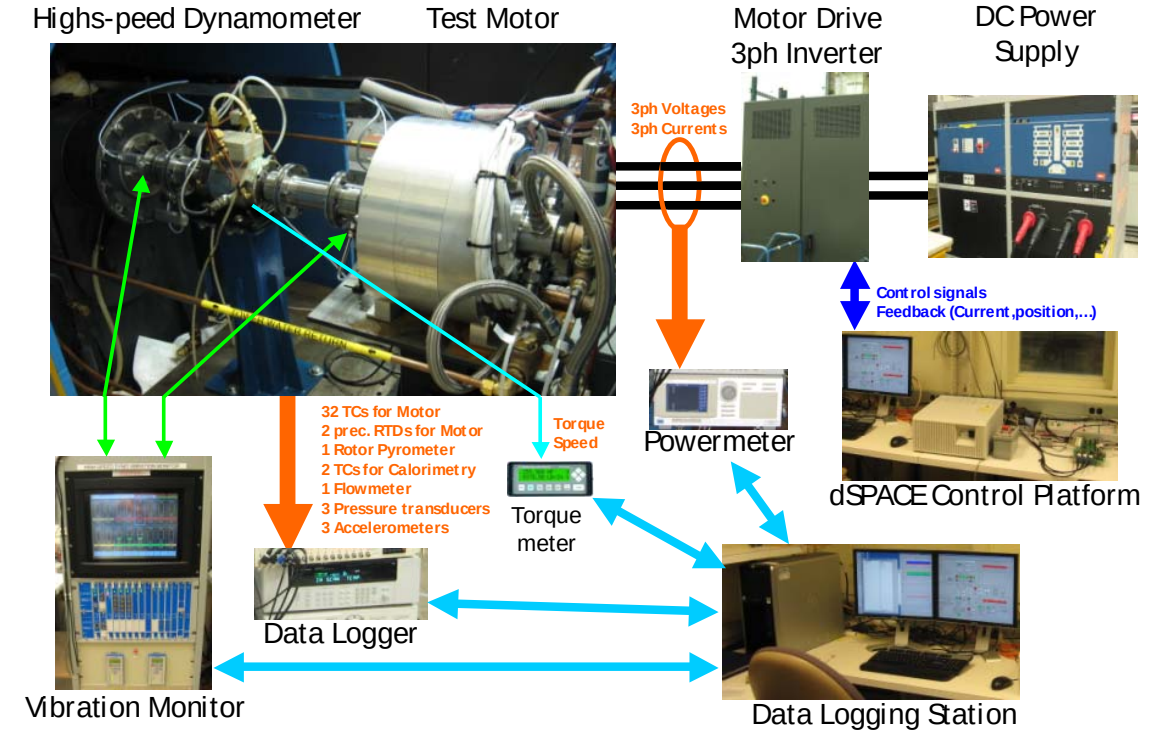


Figure 1. Test setup for the proof-of-principle machine.

Figure 2 shows the PoP machine on the dynamometer while figure 3 shows a comparison of the measured versus predicted back emf at 100 rpm. It can be seen that machine parameters closely match predictions. The machine has been tested at full load of 33 kW up to the max speed of 14000 rpm. This confirms the machine sizing. This also shows that the machine with its fundamentally novel rotor structure can run safely at 14000 rpm, which is one of the key risks. Also this shows that the machine is capable electrically of producing the rated power over the whole speed range.

Figure 4 shows the various measured machine performance parameters at rated power. These results show that the Machine meets and exceeds both peak and steady state power requirements. Efficiency targets (and 105 C coolant inlet temp.) are met at lower speeds but more work is needed to meet these challenging targets at speeds>7500 rpm

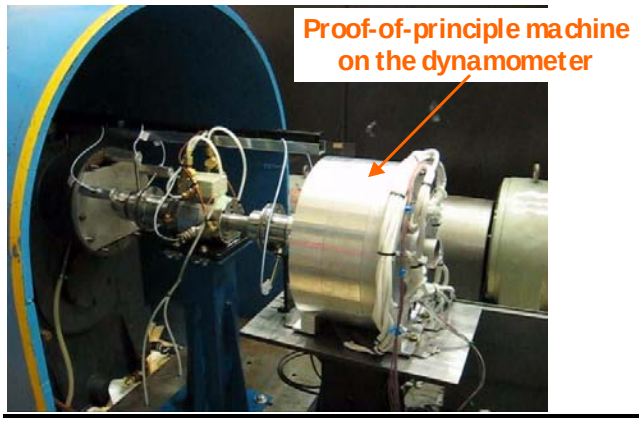


Figure 2. Proof-of-principle machine on the dynamometer.

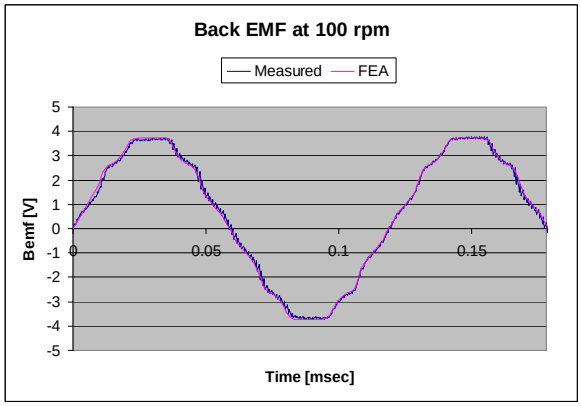


Figure 3. Predicted vs measured back emf of the proof-of-principle machine at 100 rpm.

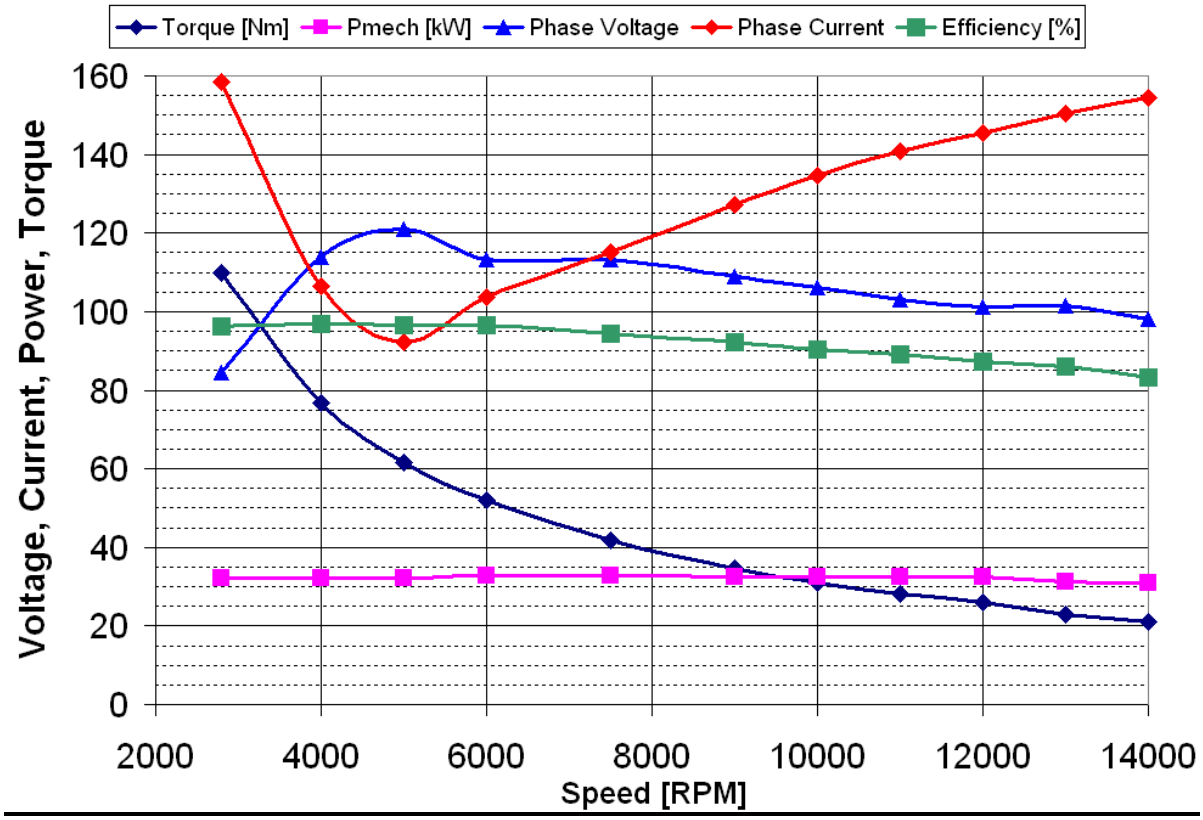


Figure 4. Proof-of-principle machine measured performance at rated power.

Figure 5 shows a comparison of the PoP measured versus predicted efficiency at rated power. Both short runs as well as heat runs are shown. It can be seen that Measured efficiency closely matches predictions up to ~ 7500 rpm. Measured efficiency progressively becomes lower than predictions at higher speeds. The source(s) of discrepancy is currently being investigated

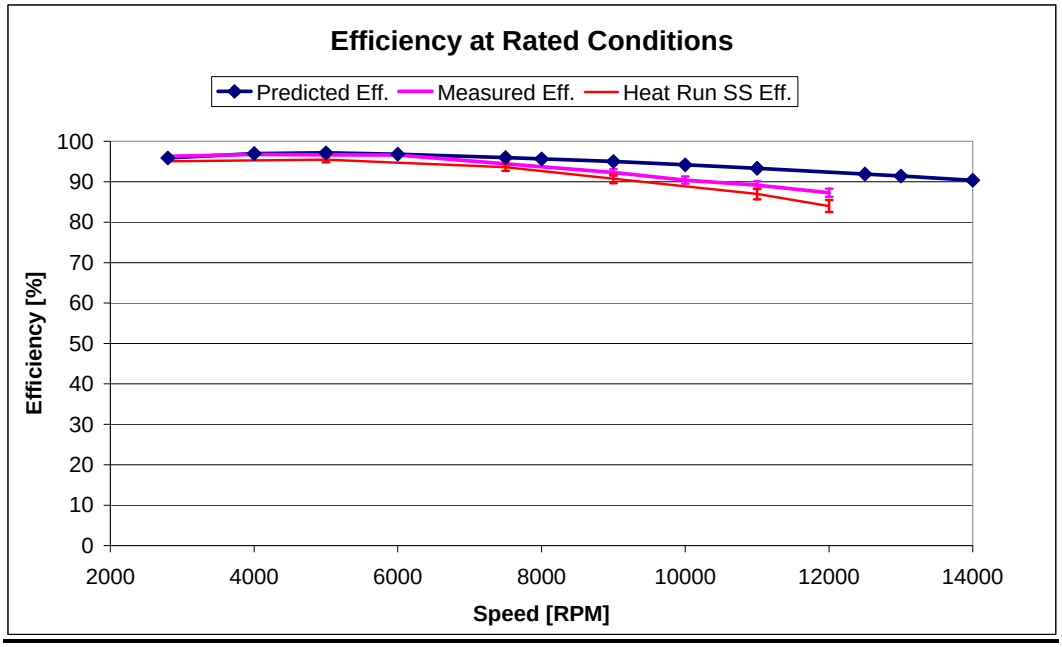


Figure 5. Proof-of-principle machine measured vs predicted efficiency at rated power.

Figure 6 shows a comparison of the PoP machine measured (electrical and calorimetric) vs predicted losses at rated power. Figure 7 shows the PoP machine heat runs temperature rises in the various machine components at various speeds. It can be seen that calorimetric based loss measurements (temperature and flow rate measurement) and electrical input/mechanical output based loss measurements have reasonable agreement. Both show losses higher than predicted. Temperature rise behavior in the various machine locations is reasonably as expected. There are two exceptions: the cooling jacket and yoke temperature rises show the thermal resistance between the cooling jacket and stator is higher than expected. The rotor temperature is also higher than expected. All these results are currently being closely examined and investigated.

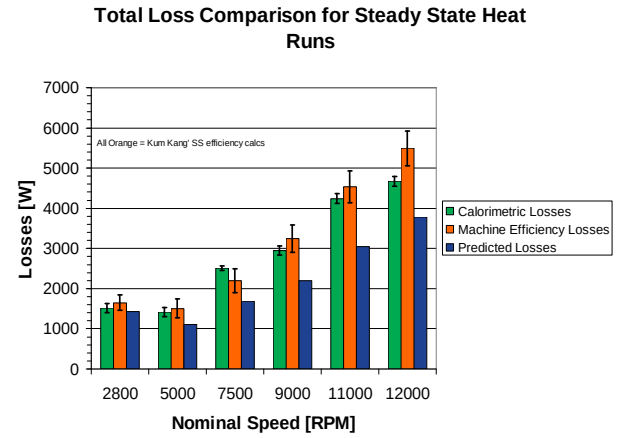


Figure 6. Proof-of-principle machine measured (electrical and calorimetric) vs predicted losses at rated power

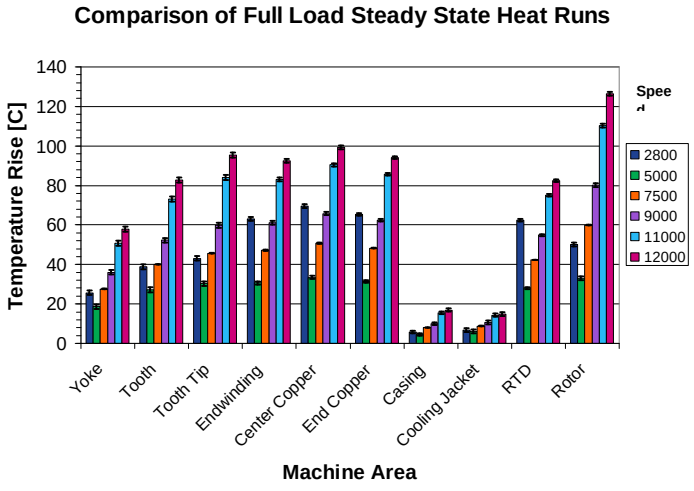


Figure 7. Proof-of-principle machine heat runs temperature rises in the various machine components at various speeds.

(B) Materials Development

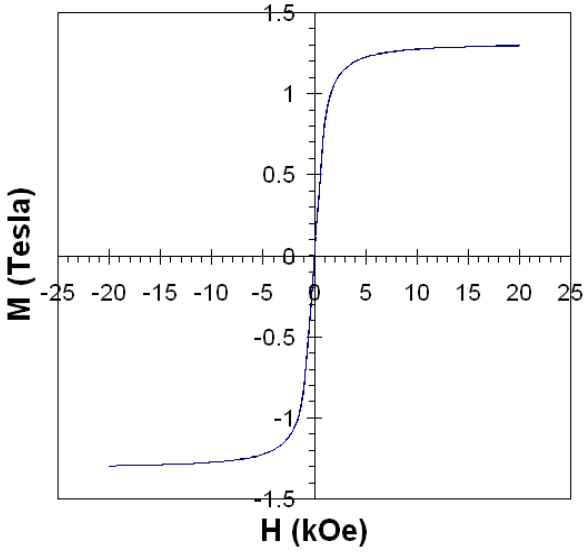
Phase I

High resistivity nanostructured soft magnetics.

Warm extrusion was used to produce bulk metallic glass-based composites with enhanced resistivity and saturation magnetization. The cross-sectional thickness of the composite material exceeded 1 mm. The composite material achieved a resistivity of 90 μΩ-cm with a saturation magnetization of 1.3 Tesla (Figure 8).

However, crystallization of the bulk metallic glass powder during the extrusion process could not be avoided. Analysis by X-ray diffraction indicated that several non-cubic crystalline product phases were produced. These crystalline phases resulted in high coercivities and low permeabilities of the extrudates, which would lead to high hysteretic power loss in components manufactured from the composites. Efforts to avoid crystallization included close monitoring of the thermal profile during the extrusion process. It is likely that adiabatic heating during extrusion was larger than estimated and caused the bulk metallic glass to exceed its crystallization temperature. It is likely that further process development could control the thermal environment during extrusion well enough to avoid crystallization.

However, as the motor design has matured, a clearer understanding of soft magnetic component geometries and material needs has been developed. This enabled a calculation of the impact of the measured soft magnetic material properties on the performance parameters of the motor design. Partial crystallization of the bulk metallic glass prevented core loss measurements at operational frequencies. Thus, the core loss behavior of MetGlas 2605SA1 (a conventional, non-bulk, magnetic metallic glass) was used to approximate the expected loss behavior of the bulk metallic glass composite. Simulations were performed for candidate prototype motor designs. Substitution of the bulk-metallic glass composite was shown to increase efficiency by up to 2% at peak-power (14400 rpm) operation. However, torque density at constant speed operation (2800 rpm) was seen to decrease by up to 1.38 Nm/kg. This decrease in overall power density resulted from the lower saturation magnetization of the bulk metallic glass composite relative to the conventional choice of Silicon steel. As it is not possble to engineer the saturation magnetization of the bulk metallic glass composite to reach the magnetization of Silicon steel, the decision was made not to continue bulk metallic glass research in Phase II.



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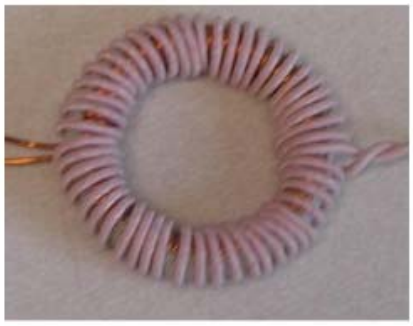

b)

Figure 8 a) DC Hysteresis loop of bulk metallic glass composite material with saturation magnetization of 1.3 T. b) Magnetic test sample of bulk metallic glass composite formed into 25.4 mm diameter toroid.

High resistivity nanostructured permanent magnets.
A composite sintered NdFeB-based microstructure was developed that allowed an enhanced effective resistivity in a permanent magnet, relative to conventionally sintered NdFeB. This would lead to a reduction in eddy current losses when used in high frequency operation such as the motor design developed in this program. A vendor was selected to explore the scalability of the process used to make the permanent magnet. The vendor delivered samples of sintered NdFeB magnets with the specified microstructure, as well as several baseline NdFeB magnets for comparison. The mass of the samples was approximately 10 grams, large enough to demonstrate feasbility. Figure 9 shows a comparison between a baseline magnet and a high effective resistivity composite magnet. The composite magnet is observed to have an energy product 7% less then the baseline magnet but the composite microstructure does enable an effective resistivity 3X that of NdFeB. Some variability in resistivity (2-4X the baseline resistivity) was noted in the samples received from the vendor. Addressing the root causes of the variability, as well as the stability of the novel microstructure in operating conditions, are important future steps to be addressed in scaling up the production process to meet motor system needs.

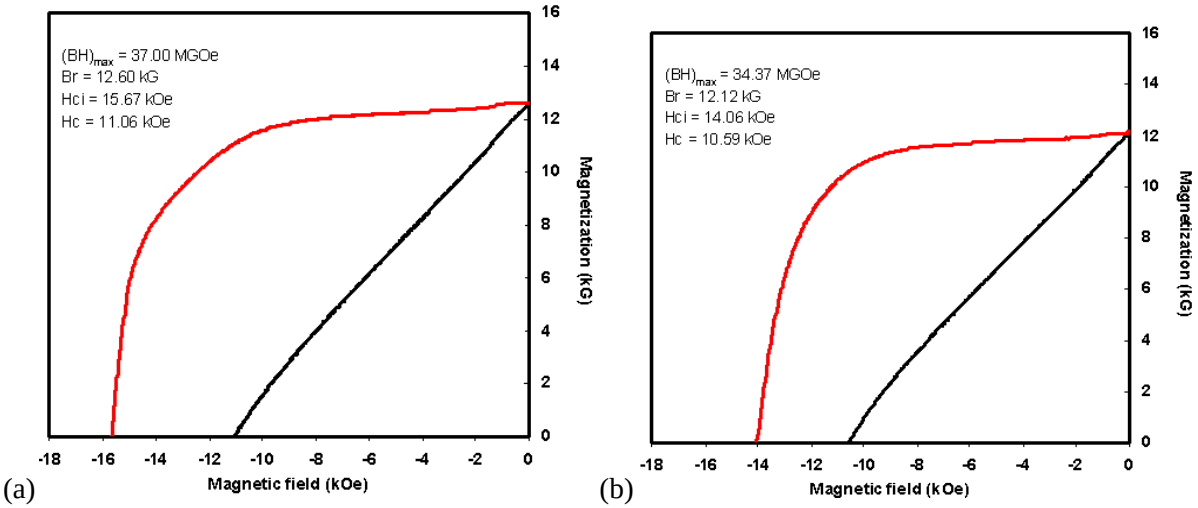

Figure 9. a) Demagnetization of conventional sintered NdFeB permanent magnet with resistivity of 140 μΩ-cm. b) Demagnetization of sintered composite NdFeB magnet with effective resistivity of 450 μΩ-cm. Energy product of composite magnet is 7% less than baseline magnet.

Phase II

High-resistivity permanent magnets
The focus of the Phase II effort high-resistivity sintered permanent magnets is to improve reproducibility and demonstrate scalable production. Phase I efforts demonstrated a novel microstructure and processing route that demonstrated an effective resistivity of 2-4X with a sample size of approximately 10 grams. Goals for Phase II include reducing the variability to achieve 3X effective resistivity and demonstrating scalability to the kilogram scale. The cost advantage of the scalable process will be compared to existing methods for achieving high effective resistivity, such as mechanical segmentation.

Improving control of the co-sintering process used to form the novel microstructure from permanent magnet and resistive phases is required to meet these goals. Alternate resistive phase compositions are being investigated to improve compatibility with the sintering behavior of the permanent magnet material. Alternate methods of ceramic green-body production, such as tape-casting, are being investigated as scalable, low-cost production methods. The densification behavior of the resistive phase during sintering,

and its degree of coefficient of thermal expansion mismatch with the permanent magnet, are being measured by high temperature dilatometry.

High temperature contact angle measurements are being investigated to determine the nature and extent of the interaction between the resistive phase and the permanent magnet material. It was learned in Phase I that some interaction and degradation of the permanent magnet is unavoidable during the co-sintering process. However, it was also demonstrated that the novel microstructure would localize the degree of interaction between the phases and minimize the impact on permanent magnet properties.

Soft magnetic material selection study
The focus of efforts in Phase II for soft magnetic material is to perform a systematic materials selection study of the major structural and magnetic components of the prototype motor's shaft and rotor assembly. The study will follow the material selection in mechanical design methodology developed by Prof. M.F. Ashby [1] of Cambridge University. This method identifies indices of materials properties based on performance metrics of mechanical systems, such as motors. The indices are used to rank known engineering materials. External constraints, such as cost per mass, or cost per unit performance, and property specification limits can be applied to narrow the selection criteria. The outcome is expected to be a set of material selection recommendations that can be used optimize system performance.

Conclusion

All the key deliverables have been met and the phase II tasks successfully initiated.

(A) Motor Development

Phase I
2 rotor & 2 stator electromagnetic (EM) concepts were developed & analyzed in detail. Scalable rotor and stator cooling concepts were selected to meet performance, simplicity and scalability requirements. The highest-performance EM concept selected for proof-of-principle motor build.

The proof-of-principle machine with a novel rotor structure and scalable thermal management schemes has been built and is almost fully tested. The machine was tested at the peak power of 55 kW at 2800 rpm for 18 seconds. The machine was also tested at the rated power of 30 kW over the speed range 2800-14000 rpm. This is a major accomplishment both electrically and mechanically. Both short runs as well as heat runs were performed. The testing of this machine retired many key risks including being able to operate the machine at the max speed of 14000 rpm with the novel rotor structure as well as being able to effectively control the machine to deliver the required power at such high speed. More work is underway to better understand the loss distribution and the effectiveness of the thermal management scheme. This effort will be concluded fairly soon.

Phase II
The tasks for efforts have been successfully initiated. The design of the second proof-of-principle machine has been finalize and build initiated. The build is expected to be finished by end of 2009 or early 2010. Based on the test results of both machines, a rotor concept will be down-selected for the next generation IPM machine that will be delivered to the DoE for verification. Development of cost model is initiated and expected to be finished by end of 2009 or early 2010

(B) Materials Development

Phase I
Novel bulk metallic glass composites have been developed with resistivities 2X conventional silicon steel and saturation magnetizations comparable to conventional magnetic metallic glasses. Simulations with the developed prototype design show that while efficiency is increased, the torque density is decreased. A

high effective resistivity co-sintered permanent magnet microstructure was demonstrated with an acceptable decrease in magnetic properties. Further work will be performed in phase II to increase reproducibility and scalability of the co-sintered composite permanent magnet

Phase II

Alternate resistive phase compositions and improvements of the co-sintering process have been identified. Densification behavior and wettability of the composite phases are being studied to improve compatibility of the phases during co-sintering. A material selection study is being performed to identify the optimal combination of materials in the rotor and shaft assembly of the prototype motor.

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3.5 Technology and Market Intelligence Regarding:

- Rare earth materials and rare earth magnets
- IGBTs (insulated gate bi-polar transistors)/high-power silicon switches
- US automotive DC and AC electric motor manufacturing capability

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Objectives

Synthesis Partners was tasked by the Department of Energy (DOE) Vehicle Technologies Program to collect, integrate and analyze open source technology and market research information to assess specific questions in three fields:

1) Rare earth (RE) materials and permanent magnets (PM)
2) Insulated gate bi-polar transistors (IGBTs)/ high power silicon switches
3) US automotive DC and AC electric motor manufacturing capability

Regarding rare earth materials and rare earth magnets and IGBTs/high-power silicon switches, Synthesis addressed:

- Current US mining or manufacturing capabilities and capacities
- Plans to expand the mining or manufacturing capabilities in the US in the near-term (over the next 10 years) and the availability of industry roadmaps
- Limitations or constraints on mining or manufacturing in the US
- Determine requirements for US industries to mine or manufacture devices, materials and magnets that would include a timeline for production ramp-up if the aforementioned requirements were met
- Potential for non-Chinese suppliers of rare earths and rare earth magnets.

Regarding the US automotive DC and AC electric motor manufacturing capability, Synthesis addressed:

- Current state of the US and global industry, to include motor types, location and current inventory
- Current state of the US industry
- Pricing structure for motors being manufactured outside the US, with direct comparison to that of the US to include a description of price drivers affecting US industry competitiveness

Approach

This rapid turnaround research effort covered a range of secondary and primary sources during the March to July 2009 timeframe. The effort led to the production of three published reports, each of which provides key findings, information on key sources identified and analyzed.

Deliverables (Major Accomplishments)

Synthesis delivered three concise written reports and several oral briefings on same under this Task. The reports are entitled:

- RE Materials and PM Report (August 2009)
- IGBT Report (August 2009)
- Electric Motor Report (August 2009)

Future Direction

Primary and secondary source collection is on-going based on the proprietary database of worldwide sources Synthesis has identified as critical to the evolution of one or more of the relevant market sectors. FY10 work includes continued market and technology assessments focused on the following areas and questions:

- Rare Earths
  - Market analyses and technology research and development updates
  - Rare Earth materials substitution including identification of new materials which could potentially be used, including new designs, re-designs, and re-engineering to reduce or eliminate rare earths, including game-changing technologies.

- Wide Band Gap Semiconductors
  - Review current technology R&D activities relevant to automotive power semiconductors
  - Focus on market and technology developments affecting devices with the following characteristics:
    - 600-1200 Volts
    - 5-20 Amps or higher if possible, up to ~70 Amps
    - 200-300°C operating environments

- Recycling of Automotive Motors, Power Electronics and Rare Earths
  - Characterize the nature of emerging programs, trends, and relevant technology developments
  - Identify approaches under consideration or being implemented
  - Ascertain emerging potentially successful economic and business models
  - Determine relevant lessons learned
  - Determine barriers to the implementation of current and emerging approaches and technologies in the US market, including economic, regulatory, and others

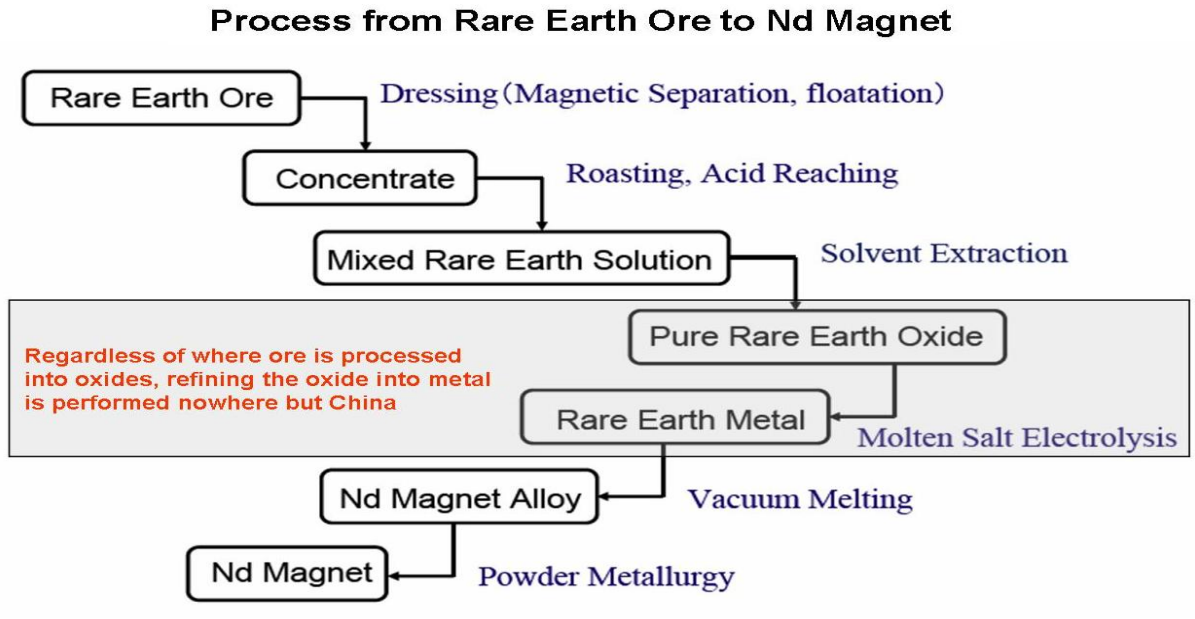
Technical Discussion

The published market research reports produced the following selected key findings. Please see the published market research reports for more detailed findings, information on sources and additional market projections.

RE Materials and PM Report (August 2009):

- Industry forecasts for the production of permanent magnet material has been revised significantly downward through 2020; the global recession will reduce sales by $7.2B (or ~40% of total sales in 2015) in the global magnetics industry
- Molycorp is the only company actively producing rare earths in US and is currently refining previously mined ore; new mining is expected in late 2010.
- Molycorp and Arnold Magnetics formed a joint venture in July 2009 to manufacture rare earth magnets in the US.

- A US infrastructure and commercial supply chain for NdFeB magnet production no longer appears to exist.
- All indications are that the Chinese plan to maintain their domination of the high-volume rare earth mining and expand into the magnet production industry.

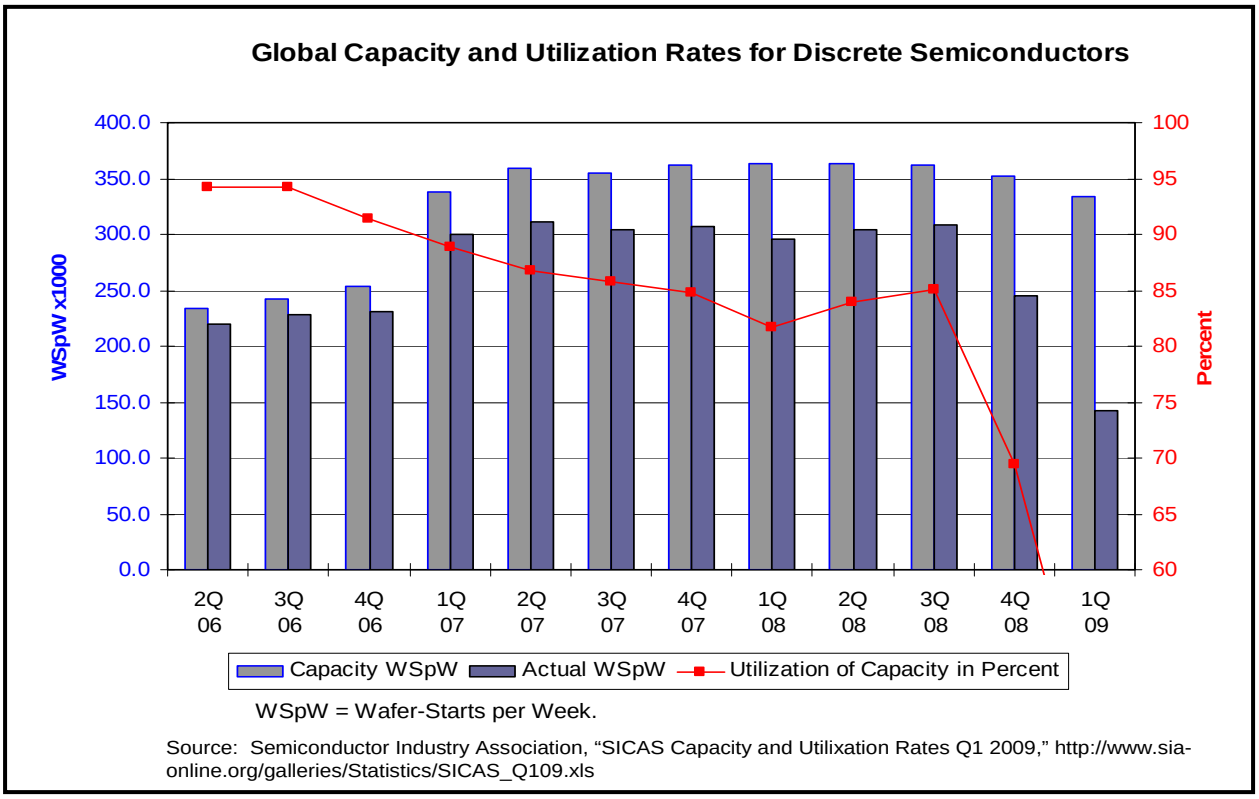


Source: Takehisa Minowa Takehi, "Rare Earth Resources for Nd Magnetics: Their Present and Future," Magnetics Conference 2009

- Global recession has driven almost all non-Chinese suppliers out of the market; all majors outside US and Canada are now owned (minority or majority share) by Chinese investors.
- US-based small mining companies face financial problems. Their best prospects in 2009 appear to be to sell their projects to the Chinese.
- Synthesis assesses a potential Rare Earth Gap in 2012-2014, as the Chinese economy is expected to consume all of its production of rare earths beginning in that timeframe, and there will be insufficient alternative supplies coming on-stream prior to that time period.
- There are potential supply-constraints affecting cobalt used in Li-Ion batteries and SmCo magnets. Therefore cobalt could become a material chokepoint similar to that of the rare earth metals.

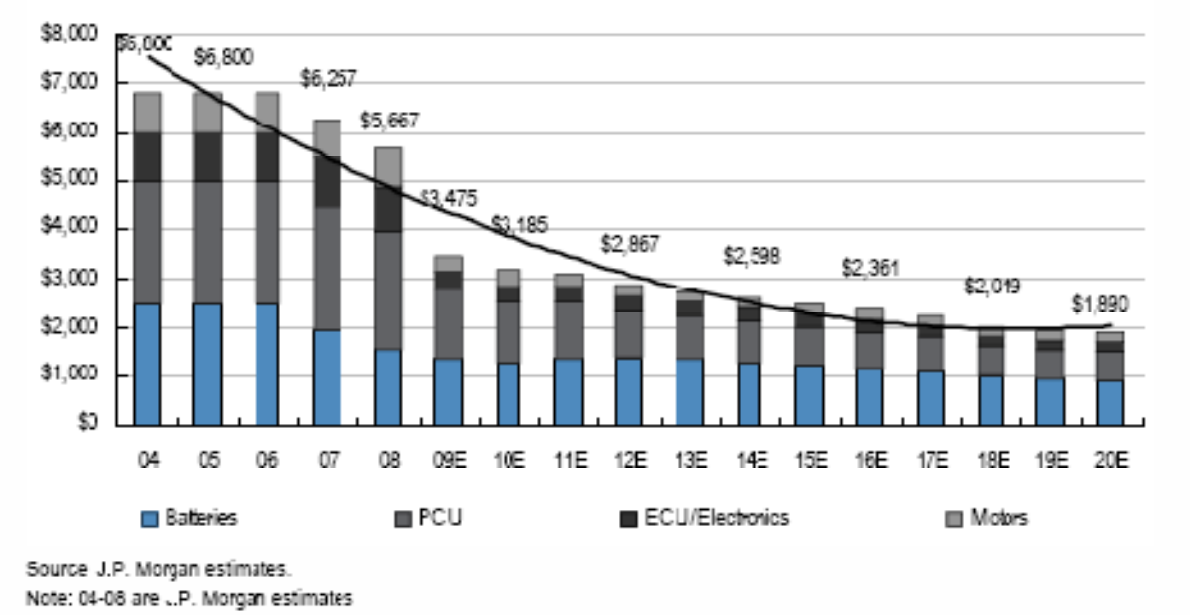
IGBT Report (August 2009):

- Recession exacerbated the downswing of a four-year business cycle
- IGBT global production capacity utilization rate is currently below 55.6 percent
- As depicted in the Figure below, global capacity utilization for production of wafers for discrete semiconductor devices – which includes IGBTs – fell precipitously beginning in the third quarter of 2008.
- Gartner Group's Dataquest Semiconductor Inventory Index (DASI) dropped from 1.54 in the fourth quarter of 2008 to 1.31 in the first quarter of 2009, indicating "severe excess inventory"
- Current excess capacity will sustain industry for foreseeable future (2-3 years)
- US manufacturing capability is being reduced
  - "Few American companies want to manufacture low-profit commodity semiconductors like IGBTs" – industry source
- No apparent near-term plans to expand US or global manufacturing capability



Electric Motor Report (August 2009):

- Demand for the motors used in hybrid electric vehicles (HEVs) is expected to grow by 480 percent by 2020, and demand for batteries and specialized power control units will grow at an even faster rate.
- Overall hybrid production costs are expected to drop by 66 percent from 2008 levels by 2020
- As noted in the Figure below, the production cost of the electric motor component is currently approximately 13.8 percent of the cost of the hybrid system; by 2020, the motor is forecast to account for only about 8.75 percent of the total system cost
- Sources indicate there is no current surplus capacity, due to the unique manufacturing requirements for these motors and the relatively low demand. However, strong growth is expected as the hybrid vehicle market grows.
- The only materials used in motor manufacturing currently facing supply constraints are the rare earth metals.
- Research indicated that six US companies manufacture motors used for electric or hybrid vehicle traction drives, or are in hybrid motor R&D.
- US manufacturing appears competitive at production rates of hundreds of motors per year (prototypes), but not at production rates of tens of thousands of motors per year (full-scale)
- One academic program on hybrid vehicle R&D was identified: the Hybrid and Plug-in Hybrid Electric Vehicle Research program in the Power Electronics and Motor Drives Laboratory at the Illinois Institute of Technology



Conclusions

Rare earth (RE) materials and permanent magnets (PM)

- The push for green technologies and industries is a driver of demand for rare earth materials. Increased demand for high power rare earth magnets, in particular for hybrid electric vehicles, electric vehicles, and wind turbines may well exacerbate emerging rare earth supply chokepoints over the next five years.

Insulated gate bi-polar transistors (IGBTs)/ high power silicon switches

- IGBT production in the US will likely not expand in the next five years. Excess inventory levels are expected to continue worldwide for the same timeframe.

US automotive DC and AC electric motor manufacturing capability

- There are relatively few companies which manufacture the motors used for electric or hybrid vehicle traction drives. US manufacturing capacity is likely to remain constrained vis-à-vis projected increasing demand. Motors are designed for specific cars and production capacity is scaled to projected vehicle sales. Research revealed six companies in the US that claim to be involved in producing motors for hybrid vehicles (including buses and large trucks) or in hybrid motor R&D.

Publications

Please see published reports.

References

Please see published reports.

Patents

None

4. Power Electronics Research and Technology Development

4.1 Wide Bandgap Materials

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Objectives

- To keep up-to-date with state-of-the-art wide bandgap (WBG) power devices and acquire, test, and characterize new WBG power devices.
- To study the feasibility of an air-cooled 55 kW inverter.

Approach

- Acquire, test, and characterize new WBG power devices. Analysis includes the following.
  - — Static characteristic tests.
  - — Dynamic characteristic tests.
  - — Behavioral modeling.
- Perform a feasibility study on an air-cooled inverter concept. The tasks include the following.
  - — Conduct research on new packaging techniques.
  - — Develop inverter designs and model them to evaluate the thermal performance through conduction analysis.
  - — Design air flow patterns and simulate the inverter design to assess the feasibility.

Major Accomplishments

- Acquired, tested, and characterized silicon carbide (SiC) junction field-effect transistors (JFETs), metal-oxide semiconductor field-effect transistors (MOSFETs), and diodes.
- Completed evaluation of a 10 kW SiC JFET-based inverter.
- Completed the feasibility study of an air-cooled 55 kW inverter design.

Future Direction

- State-of-the-art WBG power devices will be acquired, tested, and characterized.
- Test data will be used to develop SPICE (Simulation Program with Integrated Circuit Emphasis) models of the devices to aid in ORNL packaging efforts.

Technical Discussion

I. Device Testing

WBG devices acquired this year were SiC MOSFETs, normally off SiC JFETs, and SiC Schottky diodes. These devices were tested and characterized. The test results for these devices will be presented in the following sections. All the devices obtained were experimental samples.

1. SiC MOSFET

Static Characteristics

Static characteristics of a 1,200 V, 100 A SiC MOSFET in a half bridge module are shown in Fig. 1 for different operating temperatures at 20 V gate-source voltage (Vgs). This module is built using the commercial Si CM100DY-24A half bridge module package. At 15 V Vgs, the on-resistance initially decreased from 0.0194 Ω at 20°C to 0.0161 Ω at 100°C and then started to increase up to 0.0183 Ω at 175°C, as shown in Fig. 2. This behavior was noticed in the low amperage MOSFETs tested at ORNL in 2005. However, at 20 V Vgs the on-resistance increased from 0.0134 Ω at 20°C to 0.0162 Ω at 175°C. There is a significant change in the forward characteristics of the device at different gate voltages. This will affect the paralleling of the device for high-power modules.

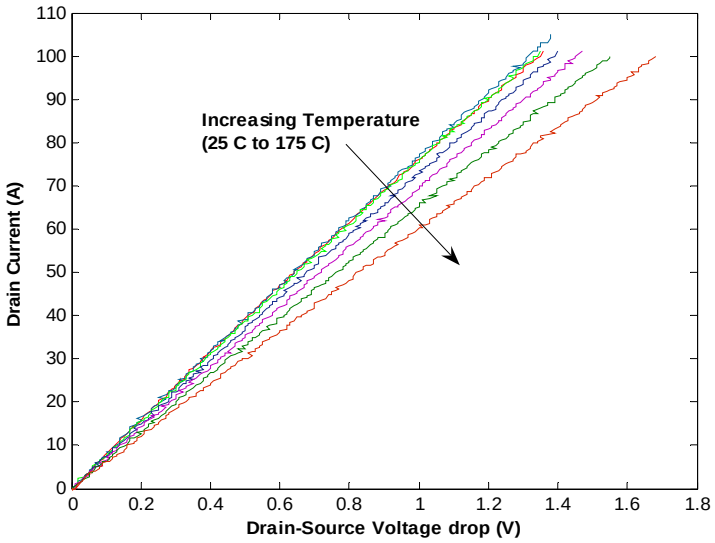

Fig. 1. Current-voltage (I-V) curves of a 1,200 V, 100 A SiC MOSFET.

Dynamic Characteristics

The SiC MOSFET was tested in a chopper circuit with double pulse switching to observe its dynamic characteristics. The double pulse circuit enables the use of an inductive load alone instead of the resistive and inductive load together. The current through the inductor builds up during the first pulse and peak forward current is adjusted by changing the width of the first pulse. The switch is turned off and turned on for short periods after the first pulse. The turn-on and turn-off energy losses can be obtained during the short pulse intervals. The gate driver used for obtaining the dynamic characteristics is a commercial gate driver (HCPL 316J). The gate voltage was switched from +15 V Vgs to -5 V Vgs. The diode in the half bridge module was used as the clamping diode with a 110 µH inductor as the load. The turn-on and turn-off energy losses of the MOSFET at 300 V and 50 A are shown in Table 1. The turn-on losses and turn-off losses do not change much with temperature.

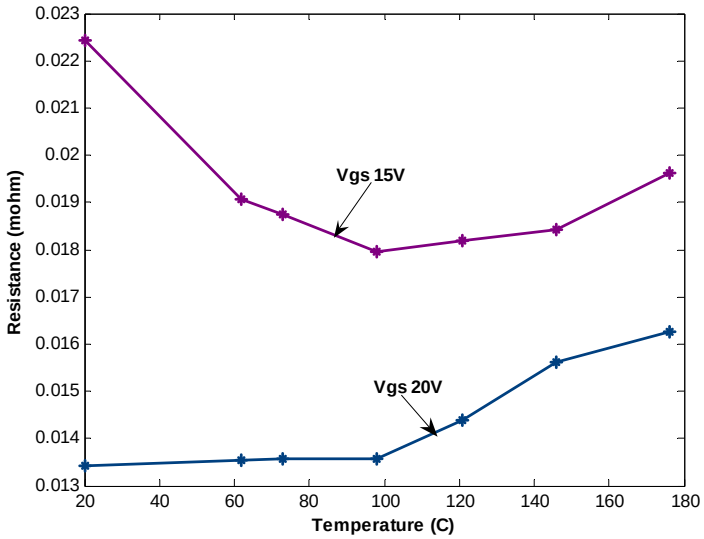

Fig. 2. On-state resistance of a 1,200 V, 100 A SiC MOSFET.

Table 1. Switching Energy Losses of SiC MOSFET

Temp (°C)	Eon (mJ)	Eoff (mJ)	Etot (mJ)
25	1.0544	1.0304	2.0848
100	1.1138	1.0344	2.1482
150	1.1318	1.0694	2.2012

2. SiC 1,200V, 100 A JBS diode

Static Characteristics

The static characteristics of a 1,200 V, 100 A SiC junction barrier Schottky (JBS) diode in the SiC MOSFET module were obtained across a wide temperature range (25°C–200°C) (Fig. 3). The forward voltage drop at 100 A current increased from 1.71 V at 25°C to 2.53 V at 200°C. The on-state voltage drop decreased from 0.78 at 25°C to 0.5014 at 200°C, as shown in Fig. 4. The on-state resistance increased from 0.0077 Ω at 25°C to 0.0176 Ω at 200°C for currents greater than 20 A. It should be noted that the diode has negative temperature coefficient below 20 A current.

Dynamic Characteristics

The SiC JBS diode was tested in the same chopper circuit as the SiC MOSFET with double pulse switching to observe its dynamic characteristics. The turn-off energy losses of the JBS diode at 300 V and 50 A are shown in Table 2. The turn-off losses do not change much with temperature, exhibiting temperature independent switching loss behavior.

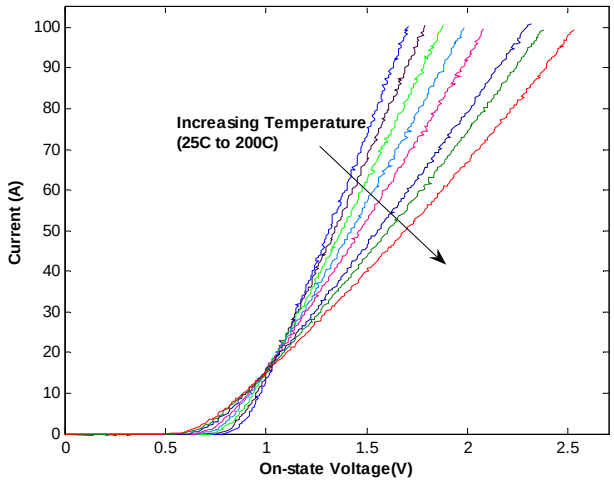

Fig. 3. I-V curves of a SiC 1,200 V, 100 A JBS diode.

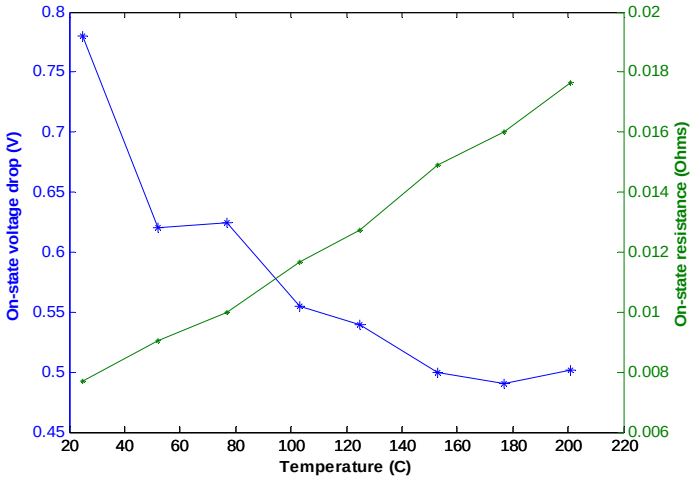

Fig. 4. On-resistance and on-state voltage of a SiC 1,200 V, 100 A JBS diode.

Table 2. Switching Energy Losses of 1,200 V, 100 A SiC JBS Diode

Temp (°C)	Eoff (mJ)
25	2.47
100	2.65
150	2.71

3. Normally off 1,200 V, 10 A SiC JFET

Static Characteristics

Static characteristics of a 1,200 V, 10 A normally off SiC JFET are shown in Fig. 5 for different operating temperatures. Normally off devices are the preferred type of devices in power converters for fail-safe operation. The forward characteristics were obtained for a gate voltage of 3 V. The on-resistance of the JFET increases from 0.093 Ω at 25°C to 0.2 Ω at 150°C and hence has a positive temperature coefficient (Fig. 6).

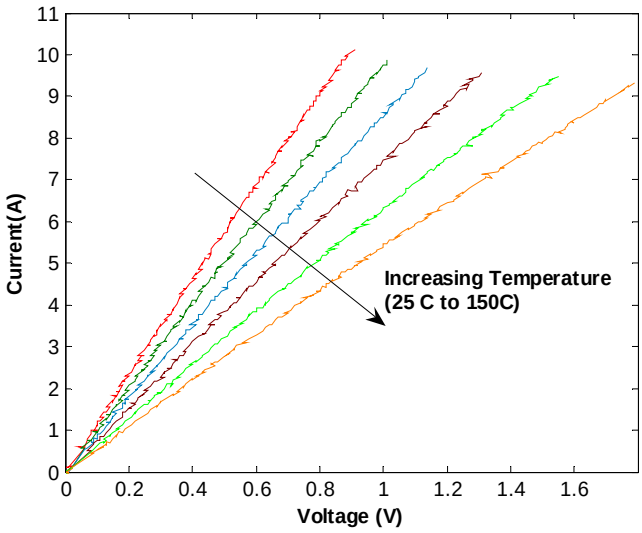

Fig. 5. I-V curves of a 1,200 V, 10 A normally off SiC JFET.

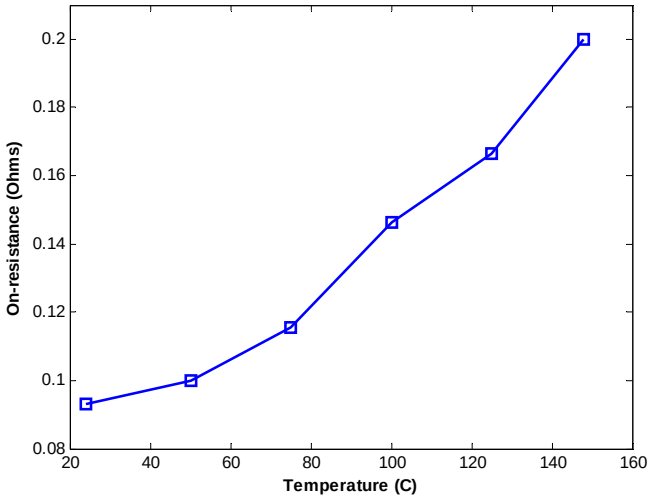

Fig. 6. On-resistance of a 1,200 V, 10 A normally off SiC JFET.

Dynamic Characteristics

The turn-on and turn-off energy losses of the 1,200 V, 10 A normally off SiC JFET were obtained using the double pulse circuit with a load inductance of 110 µH, and a 600 V, 10 A Cree Schottky diode was used as the clamping diode in the chopper circuit. The effect of the diode on the SiC JFET will be minimal because of the almost zero reverse recovery current of the diode. The gate drive used for the test was a commercial IDD414PI IXYS chip with 35 V, 14 A output drive capability. The device requires constant current to remain switched on, and this features demands more power from the gate driver. The data were obtained at 600 V dc for various currents at 25°C and 150°C. The total energy losses increase with an increase in current; however, the losses do not change much with increases in temperature (Fig. 7).

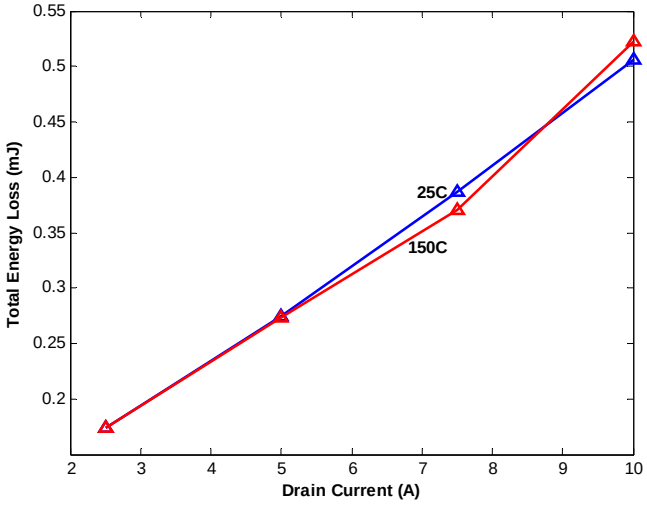

Fig. 7. Switching losses of a 1,200 V, 10A normally off SiC JFET.

4. Normally off 1,200 V, 50 A SiC JFET

Static Characteristics

A 1,200 V, 50 A normally off SiC JFET in an experimental SiC half bridge module was tested. The on-state characteristics were obtained at 3 V Vgs. Static characteristics of the JFET are shown in Fig. 8 for different operating temperatures. On-state resistance increased from 0.0369 Ω at 25°C to 0.1478 Ω at 175°C (Fig. 9).

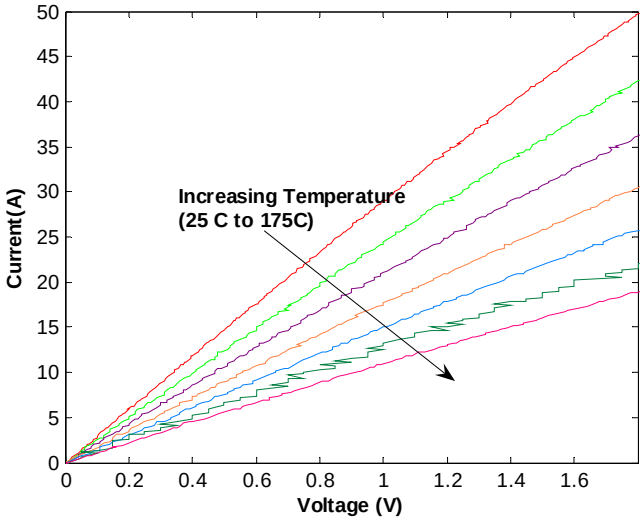

Fig. 8. I-V curves of a 1,200 V, 50A normally off SiC JFET.

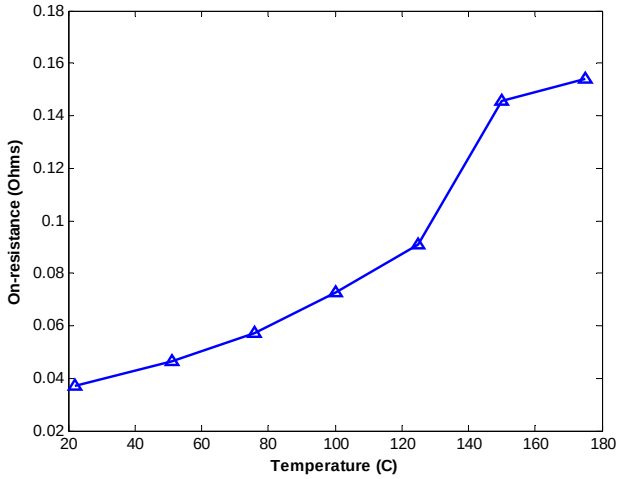

Fig. 9. On-resistance of a 1,200 V, 50 A normally off SiC JFET.

Dynamic Characteristics

The turn-on and turn-off energy losses of the JFET were obtained using the double pulse circuit with a load inductance of 110 µH, and the Schottky diode in the module was used as the clamping diode in the chopper circuit. The gate drive used for the test was a commercial IDD414PI IXYS chip with 35 V, 14 A output drive capability similar to the single JFET device. Similar to the single JFET, the device requires constant current for the device to remain switched on. The data were obtained at 600 V dc for various currents and for 25°C and 150°C. The total energy losses increase with an increase in current; however, the losses change very little with increases in temperature (Fig. 10).

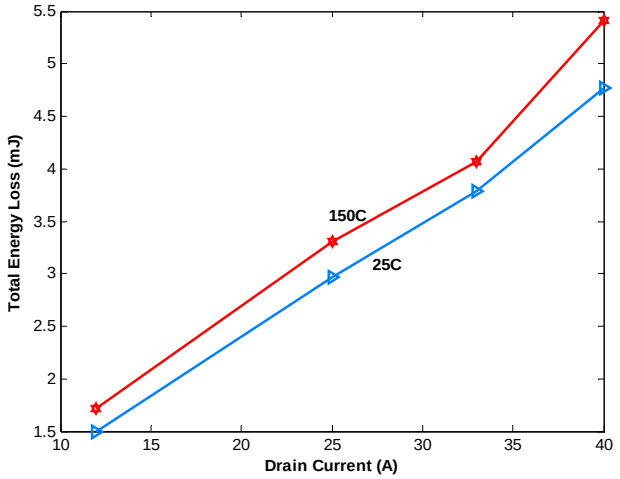

Fig. 10. Switching losses of a 1,200 V, 50A normally off SiC JFET.

5. SiC 1,200 V, 40 A Schottky Diode

Static Characteristics

The static characteristics of a 1,200 V, 100 A SiC Schottky diode in the SiC JFET module were obtained across a wide temperature range (25°C–175°C), as shown in Fig. 11. The on-state voltage drop decreased from 0.8514 V at 25°C to 0.6737 V at 175°C as shown in Fig. 12. The on-state resistance increased from

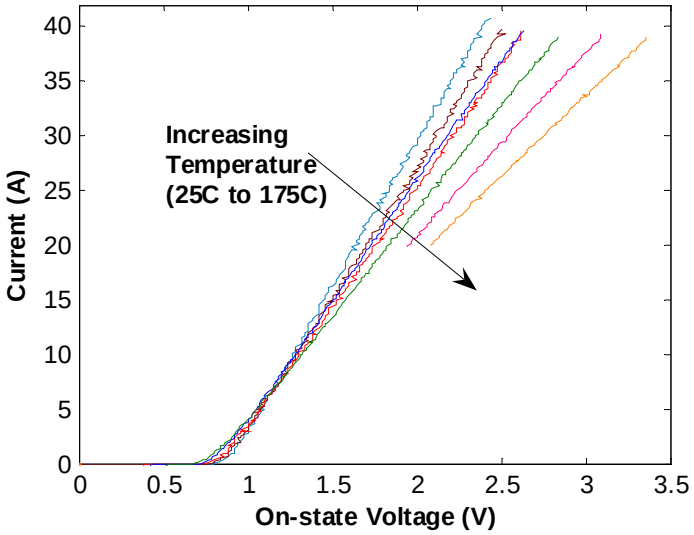

Fig. 11. I-V curves of a 1,200 V, 40A SiC Schottky diode.

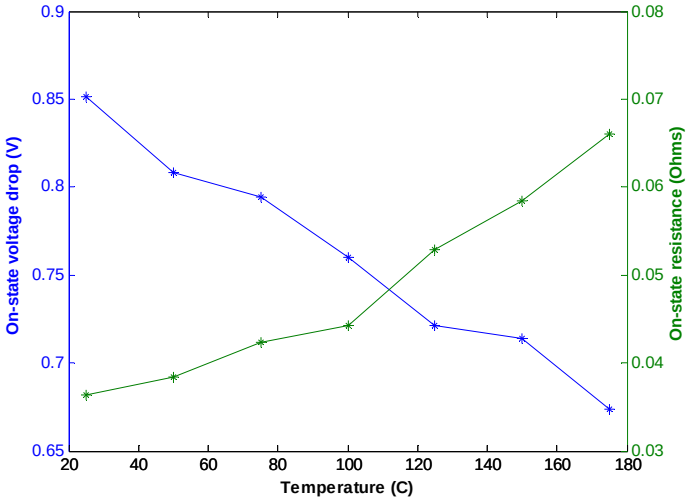

Fig. 12. On-resistance and on-state voltage of a 1,200 V, 40 A SiC Schottky diode.

0.0364 Ω at 25°C to 0.066 Ω at 175°C for currents greater than 5 A. It should be noted that the diode has negative temperature coefficient below 5 A current.

Dynamic Characteristics

The SiC Schottky diode was tested in the same chopper circuit as the SiC JFET with double pulse switching to observe its dynamic characteristics. The turn-off energy losses of the Schottky diode were obtained for 600 V and various currents at 25°C and 150°C. The turn-off losses increase with current and temperature as shown in Fig. 13.

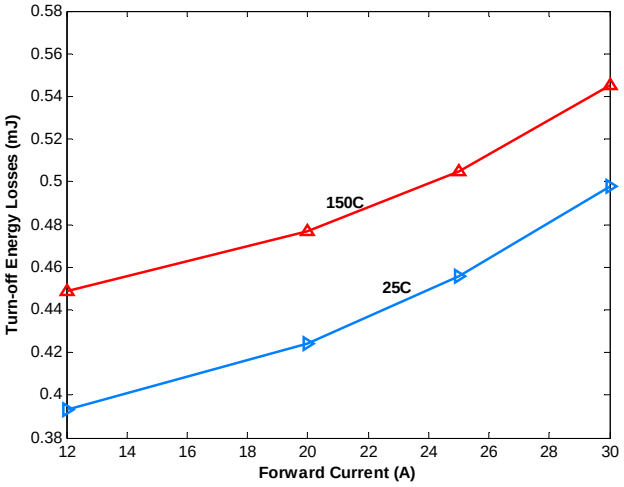

Fig. 13. Switching losses of a 1,200 V, 40A SiC Schottky diode.

II. SiC Inverter Testing

A high efficiency, high temperature SiC JFET inverter phase leg module is shown in Fig. 14. Each module is a single phase leg and is composed of six 1,200 V SiC JFETs; two 1,200 V Schottky diodes; and a thermistor to detect the temperature inside the module. Three SiC JFETs are in parallel to achieve a higher current rating (~30 A). The package is designed to work at an ambient temperature of at least 200ºC. The module is composed of several layers from top to bottom: SiC die, silver filled polyimide die attach, DBC on BeO (12 mil thick Cu on both sides of 25 mil thick BeO), silver filled polyimide substrate attach, and alloy 42 housing with glass hermetic seals. These layers are bonded together through silver filled polyimide die attach material, and electrical connections are made with 5 mil diameter aluminum wire bonds. A three-phase inverter was built using three single leg modules shown in Fig. 15. The dimensions of the inverter are 25 cm × 10 cm × 11 cm, including the extruded heat sink and control boards.

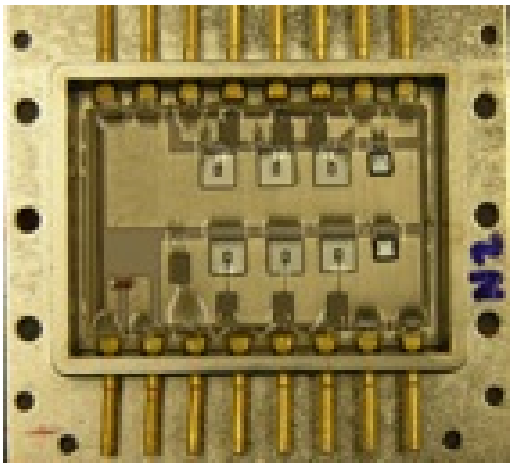

Fig. 14. SiC JFET phase leg module.

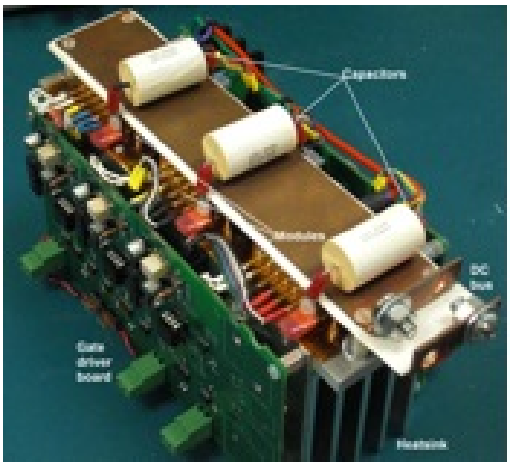

Fig. 15. Prototype SiC JFET inverter.

Experimental Results

The SiC inverter developed was tested with a resistor-inductor load. It was controlled by space-vector pulse-width modulation signals generated by a digital signal processing board, and the control program was developed in MATLAB Simulink. The direct current input voltage, current, and three-phase output voltage were monitored and measured by an oscilloscope and a PZ4000 power meter. Figure 16 shows some test results for a 60 Hz fundamental output frequency with a modulation index of 0.8 and three different switching frequencies (10, 15, 20 kHz). The maximum efficiency, 98.5%, was achieved at a switching frequency of 10 kHz at 4 kW output power. The temperature inside the modules was measured to be 64°C at this operating condition.

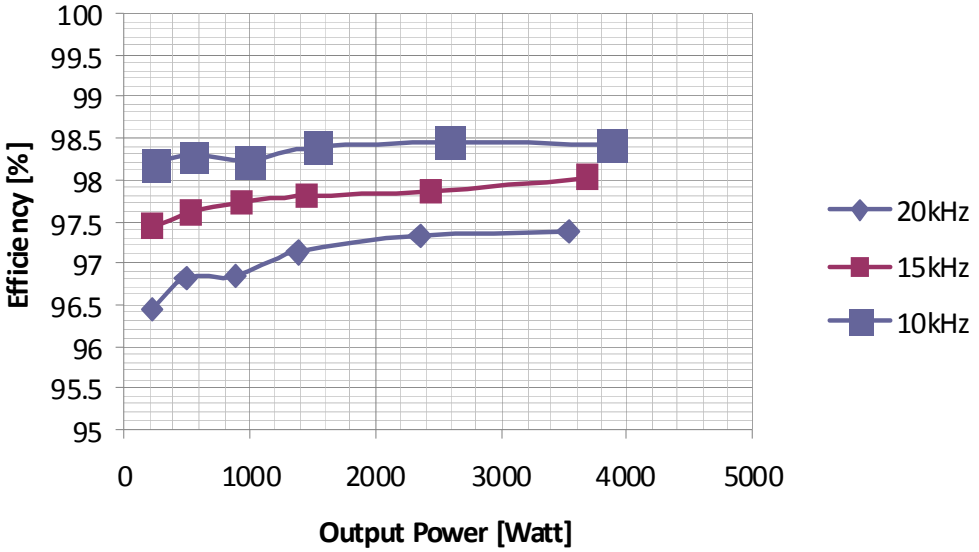

Fig. 16. Efficieny curves of all-SiC JFET inverter.

III. Air-Cooled Inverter

Several models were developed for the feasibility study. Three-dimensional models of the inverter designs were created in COMSOL. Only steady conduction analyses were performed for the initial feasibility simulations of the inverters. Based on the results of the conduction model analyses a single design was chosen for the air-flow study. Several air-flow models were assessed, and the model with minimum pressure drop and maximum velocity was selected. The inverter design was then simulated with the chosen air-flow pattern to obtain the temperature of each component in the design. The results showed that a 55 kW inverter with air cooling is possible with a device junction temperature of 200°C at 12 kW/L power density. This is well within the VTP 2010 targets for inverter power density. The design was also modified to minimize the bus inductance to keep the electrical parameter tradeoff for thermal performance to a minimum. This feasibility study clearly demonstrates the need for WBG device technology to be developed to meet the power electronics VTP power density target at elevated temperatures.

Conclusion

Several new SiC JFETs, MOSFETs, a Schottky diode, and a JBS diode were acquired, tested, and modeled. All the devices tested this year were 1,200 V devices as compared to the previous year's 600 V devices. A 10 kW SiC JFET-based inverter was tested to demonstrate the state-of-the-art technology for WBG applications. A feasibility study on a 55 kW air-cooled inverter design was completed, and results showed that air cooling is possible with a device junction temperature of 200°C, achieving a power density of 12 kW/L.

Publications

1. M. Chinthavali, H. Zhang, L. M. Tolbert, and B. Ozpineci, "Update on SiC-based Inverter Technology," Brazilian Power Electronics Conference, September 2009 (in press).
2. M. Chinthavali, P. Otaduy, and B. Ozpineci, "Performance Comparison Study of SiC and Si Technology for an IPM-based Drive System," International Conference on Silicon Carbide and Related Materials, October 2009 (in press).

4.2 An Active Filter Approach to the Reduction of the DC Link Capacitor

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Objectives

- To replace the bulky direct current (dc) link capacitor with a much smaller size active filter that imitates what a dc link capacitor does.
  - — Weight and volume of the traction inverter can be reduced while the reliability and lifetime of the inverter will be increased.

Approach

- Establish performance requirements for an active filter.
- Simulate an active filter that can replace a dc link capacitor for a traction inverter.

Major Accomplishments

- Built a simulation model of a traction drive system to establish the performance requirements for an active power filter (APF).
- Achieved an active filter approach to replace the dc link capacitor.
- Analyzed the parameter dependence of the APF and the underlying barriers of this method.

Future Direction

None: Project concluded at end of FY 2009.

Technical Discussion

Background

In an electric traction system composed of a battery, dc bus, three-phase inverter, and induction motor, harmonic current in the dc bus introduced by the switching behavior of the inverter is significant. Excessive harmonic current can greatly disturb the dc bus voltage and cause thermal stress on the dc bus capacitor, interference with the communication and control system, additional heat, audible noise, mechanical stress, and vibration [1].

The dc bus capacitor is used to filter the dc bus current harmonics and to reduce the dc voltage ripple. It occupies 35–40% of the whole traction inverter volume and weight and costs up to 23% of the inverter. Electric vehicle and hybrid electric vehicle manufacturers are interested in savings in the cost, weight, and volume of these capacitors. An APF could be one way to reduce the capacitor size. This project addresses

these issues by presenting a method to replace the bulky capacitor with an APF in a 55 kW traction drive system and analyzing the problems and barriers in this method.

Operating Principles

A typical traction drive system is shown in Fig. 1. It consists of a dc source, an APF, a three-phase inverter, and a traction motor, which in this case is an induction motor. The synthesis of a smooth sinusoidal current, with minimum harmonics, for the alternating current motor drive with a stiff dc voltage source requires a high rate of switching with different combinations of the inverter switches. The most commonly used modulation methods are sinusoidal pulse width modulation and space vector modulation. By using these modulation methods, the output current of the inverter can be modulated to a desired sinusoidal shape, but the dc side ripple current drawn from the battery can be significant. To demonstrate the waveforms of dc bus current, a specific example using a three-phase inverter feeding a squirrel cage induction motor is used. The system parameters are shown in Table 1.

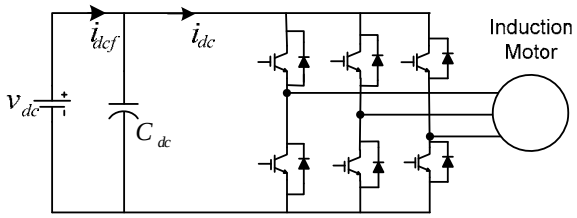


Fig.1. Hybrid electric vehicle traction drive system.

Table 1. Parameters of the Traction Drive System

Parameter	Value
dc bus voltage	500 V
dc bus capacitor	2,200 μF
Three-phase inverter switching frequency (f_{sw})	10 kHz
Three-phase inverter modulation frequency (f_m)	50 Hz
Output power	55 kW
Number of poles in induction motor (IM)	2
Stator resistance of IM	0.19 Ω
Rotor resistance of IM	0.39 Ω
Magnetizing inductance of IM	4 mH
Stator and rotor leakage inductance	270 μH

The dc bus current can be obtained through a MATLAB Simulink simulation using the PLECS toolbox. Figures 2 and 3 show the dc bus ripple current before filtering and the Fourier transform of this current, respectively. Without the smoothing of the dc bus capacitor, the current pulsates between −70 A and 220 A, which is the peak phase current for the motor in this simulation. From Fig. 3, we can see that the dc component is 110 A; there are high harmonic components at $f_{sw}\pm3\times f_m$, $2\times f_{sw}$, $2\times f_{sw}\pm6\times f_m$, $3\times f_{sw}\pm3\times f_m$, $4\times f_{sw}$, and $4\times f_{sw}\pm6\times f_m$; and there are some low harmonic components at higher frequency.

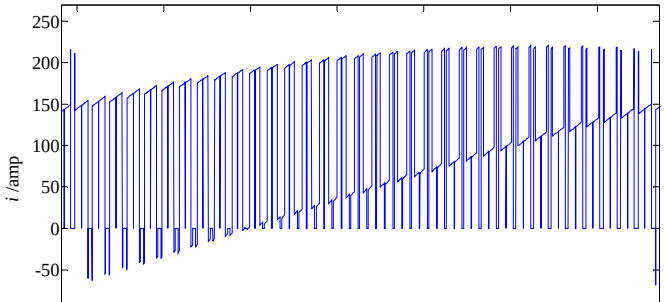


Fig. 2. The dc bus ripple current before filtering.

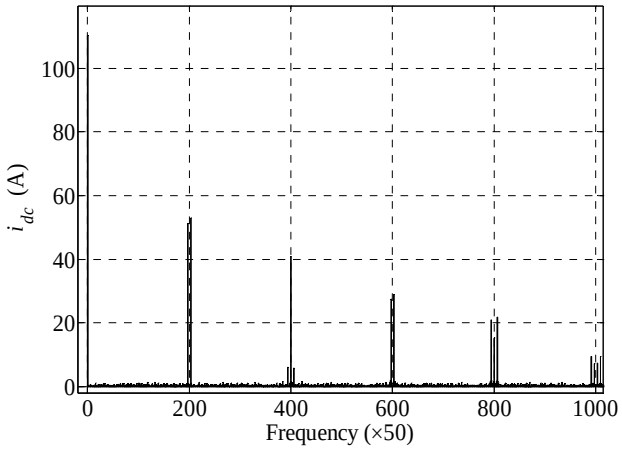


Fig. 3. Harmonic spectrum of the dc bus current.

The purpose of an APF is to absorb the ripple current and leave only the dc component. To fabricate the ripple current, an H-bridge current-source inverter topology, shown in Fig. 4, was used. It is composed of an inductor and a single full bridge inverter. A small capacitor is still necessary for some smoothing, but it is much smaller than the original dc bus capacitor. Note that the figure shows reverse blocking insulated gate bipolar transistors (IGBTs). Reverse blocking IGBTs have limited commercial availability with the highest available ones rated at 1,200 V and 55 A. In the simulation study for this project, conventional IGBTs were used with series diodes for reverse blocking.

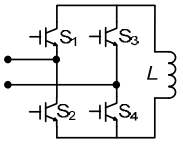
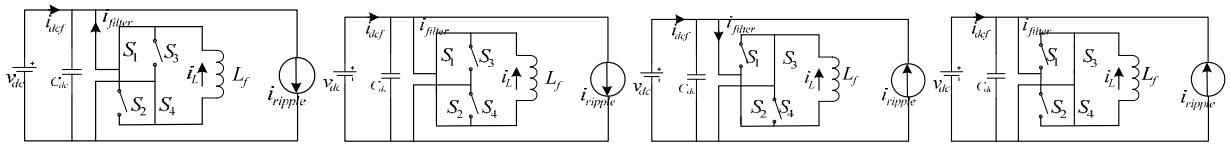


Fig.4. Active power filter.

To illustrate the operating principle, equivalent circuits of the traction drive system were derived as in [2] and are shown in Fig. 5. A ripple current source i_{ripple} imitates the input harmonic current of the three-phase inverter. According to the direction of the filter current and harmonic current, the APF can operate in four modes. Figure 6 illustrates the operating modes by indicating the current paths.



(a) Mode 1 **(b) Mode 2** **(c) Mode 3** **(d) Mode 4**

Fig. 5. Equivalent circuits under different operating modes.

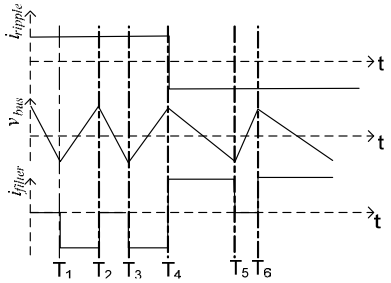


Fig. 6. APF operating current and voltage waveforms.

The operating modes are explained in detail as follows.

Mode 1: When the ripple current i_{ripple} flows into the load, which is defined as positive, filter switches S_1 and S_4 are closed (interval between time T_1 and T_2 in Fig. 6) and the inductor current i_L is injected into the dc bus. The direction of filter current i_{filter} in this mode is defined as negative. Because i_{filter} is larger than i_{ripple}, i_{filter} charges the capacitor and hence the dc bus voltage v_{dc} increases. The following equation describes v_{dc}:

$$C_{dc}\frac{dv_{dc}}{dt} = -i_{ripple} - i_{filter} \quad , \tag{1}$$

where C_{dc} is the dc bus capacitor; dv_{dc} and dt are the derivations of v_{dc} and time t.

Mode 2 starts once v_{dc} reaches the upper boundary of its preset hysteresis band.

Mode 2: To reduce v_{dc}, S_1 and S_2 are closed; i_L freewheels through them. Because the ripple current is still positive, it discharges the capacitor, and hence v_{dc} decreases. This can be described by

$$C_{dc}\frac{dv_{dc}}{dt} = -i_{ripple} \ . \tag{2}$$

When v_{dc} reaches the lower bound, this mode ends. It lasts from T_2 to T_3 (Fig. 6).

Mode 3: When the ripple current is negative, S_2 and S_3 are closed to produce positive $i_{filter;}$ i_{ripple} goes into the filter. Because i_{filter} is larger than i_{ripple}, the total current discharges the capacitor, and v_{dc} decreases as shown in interval T_4 to T_5 in Fig. 6. Once it reaches the lower boundary, mode 3 ends. Equation (3) describes the voltage of the dc bus during this period:

$$C_{dc}\frac{dv_{bus}}{dt} = -i_{ripple} - i_{filter} \quad . \tag{3}$$

Mode 4: In this mode, S_3 and S_4 are closed. The inductor current i_L freewheels through S_3 and S_4, and i_{ripple} charges the capacitor; thus, v_{dc} increases. This mode corresponds to the time interval T_5 to T_6 in Fig. 6 and can be described by

$$C_{dc}\frac{dv_{bus}}{dt} = -i_{ripple} \ . \tag{4}$$

According to the operation principle depicted above, the switching strategy of an APF is influenced by two variables: dc bus voltage ripple and the ripple current generated by the three-phase inverter. The control circuit of the APF is shown in Fig. 7. Two control loops are used to generate the control signals. A dc bus voltage v_{dc} is detected and filtered to get an average value, V_{dc}. Voltage ripple Δv_{dc} is obtained by subtracting the average value V_{dc} from v_{dc}, and then it is fed to a hysteresis-band controller to generate a logic signal C_1. To compensate for the loss in the inductor and keep the inductor current to the desired value I_L, i_L is controlled by a feedback proportional-integral (PI) controller, the error e_{iL} is taken through the PI controller, and the output is added to Δv_{dc}. In addition, the polarity of the current ripple is detected as signal C_2. A decoder is used to generate the switching signal for S_1, S_2, S_3, and S_4.

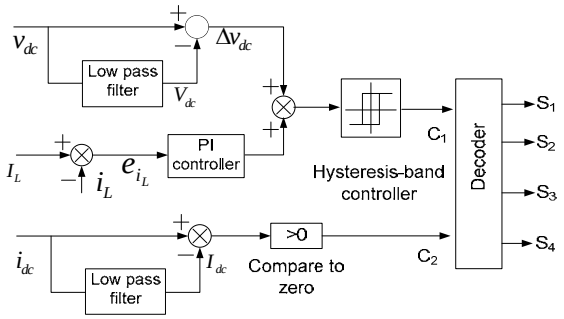


Fig. 7. APF control circuit.

Simulation Results

The motor drive system with APF was modeled and simulated using MATLAB Simulink with the PLECS toolbox according to the topology and operating principles described above. The system parameters were the same as listed in the preceding section except that a 100 μF smoothing capacitor was used instead of the 2,200 μF capacitor. Four IGBTs, two diodes, and a 5 mH inductor were used for the APF. For comparison purposes, only the case with the large capacitor filter was studied.

Figure 8 shows the simulation results. The left column shows current and voltage waveforms in the original single capacitor case with no APF, and the right column shows the results for the APF case. Figure 8(a) shows the dc bus current before and after filtering. Figure 8(b) shows the zoomed plot of the dc input current. The current ripple is between 160 A and 220 A before filtering. The fundamental frequency of dc bus current ripple is at 3 kHz, which is six times the modulation frequency because of the modulation of the three-phase inverter. In the passive method, the current ripple fluctuates from 3 A peak-to-peak (p-p), to 10 A p-p. While in APF method, the ripple current is also 10 A p-p because the control method is hysteresis control to keep the current within a bandwidth. Figure 8(c) shows the voltage ripple of dc bus. As with the current ripple in the passive method, the voltage ripple changes from 0.5 V p-p to 2 V p-p, while in the APF method it is strictly at 2 V p-p.

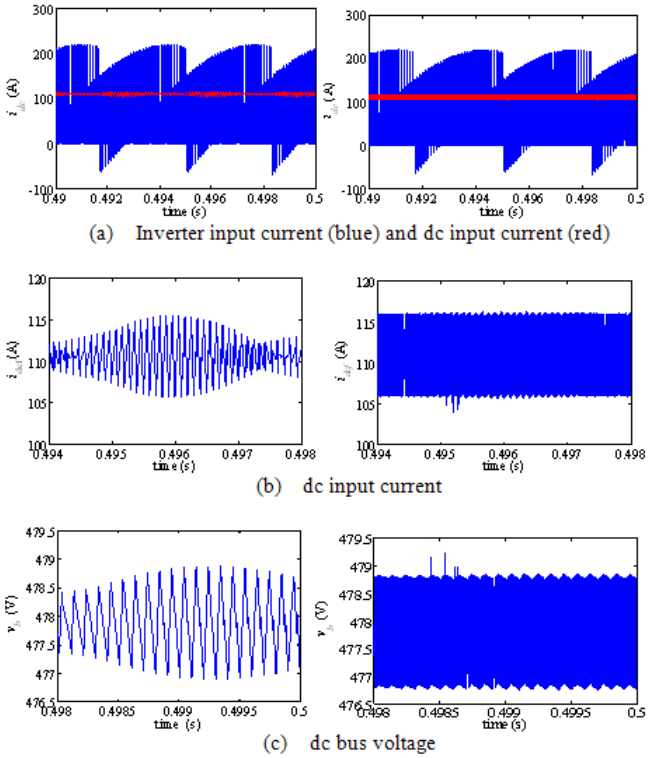


Fig. 8. Simulation results for the large capacitor only case (figures on the left) and APF case (figures on the right).

Figure 9 shows the frequency spectrum of the dc input current through 250 kHz for both cases. An enlarged figure is posted at the top right corner of each one. It can be seen from the frequency spectrum that harmonic components are almost eliminated leaving only the dc current. For the capacitor only case, there are small harmonic components at $f_{sw}\pm3\times f_m$, $2\times f_{sw}$, $2\times f_{sw}\pm3\times f_m$, $3\times f_{sw}\pm3\times f_m$, and so on. The highest magnitude harmonics are 2 A at $f_{sw}\pm3\times f_m$. For the APF case, the harmonic magnitude is much lower and spread throughout the spectrum; this is because the frequency of the ripple current is not constant in the APF method either.

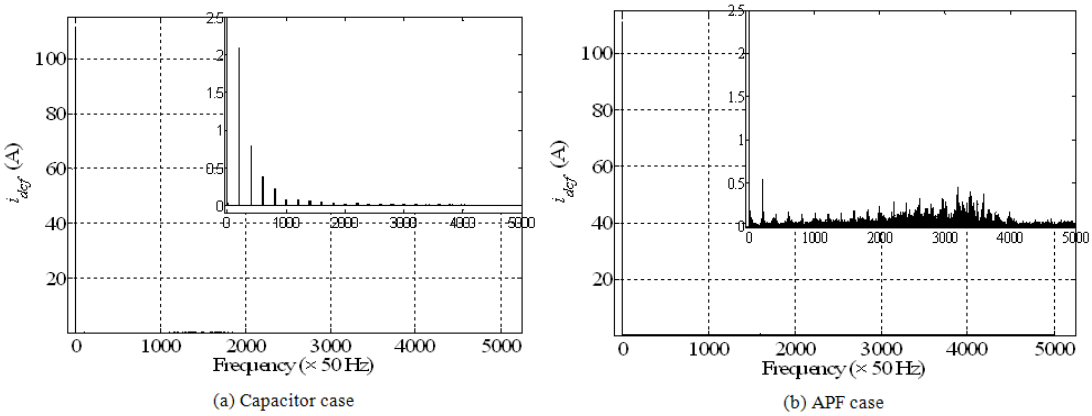


Fig. 9. Harmonic spectrum of input current.

Parameter Dependent Analysis and Barriers

As noted previously, the dc bus voltage ripple, which depends on the preset controller hysteresis band, can affect the dc input current ripple. Figure 10(a) shows the relationship between them. It is clear that, as the other circuit parameters and filter conditions remain the same, the current ripple increases as the voltage ripple monotonically increases. For instance, the current ripple is 10 A when the hysteresis band is 2 V, and is 25 A when the hysteresis band is 5 V. As shown in Fig. 5, it is clear that the sum of active filter current and load current charges or discharges the capacitor causing the voltage ripple in the capacitor, and the voltage change directly leads to the input current ripple. Therefore, current ripple can be controlled indirectly through the control of the voltage hysteresis band.

The switching losses in power switches are proportional to the switching frequency, suggesting that the switching frequency should be lower for reducing APF losses. According to the simulations, two crucial parameters affecting the APF frequency can be identified: dc bus voltage ripple and the smoothing capacitor value. Because the APF changes modes to charge or discharge the capacitor, increasing the voltage hysteresis band or capacitance can increase the time of reaching the voltage boundary, which means the APF can work at a slower frequency. The relation between frequency and voltage ripple is shown in Fig. 10(b). Since the bus ripple voltage is also proportional to the current ripple, it cannot increase too much. A tradeoff should be made to determine the voltage ripple band. A range of 2 to 3 V is acceptable in this situation. On the other hand, the capacitance of the smoothing capacitor is inversely proportional to the switching frequency. When the capacitor is 1 per unit (i.e., 100 μF in the simulation), the maximum switching frequency is 160 kHz; when the capacitor increases to 5 per unit, the frequency can decrease to 26 kHz, as shown in Fig. 10(c). This is a more practical switching frequency for the IGBTs, and because the capacitance is one-fourth of the original value, the reduction is still significant.

The parameter dependence relations can be explained by applying Coulomb's law to the dc bus voltage:

$$C \cdot \Delta V_{dc} = \Delta Q \quad , \tag{5}$$

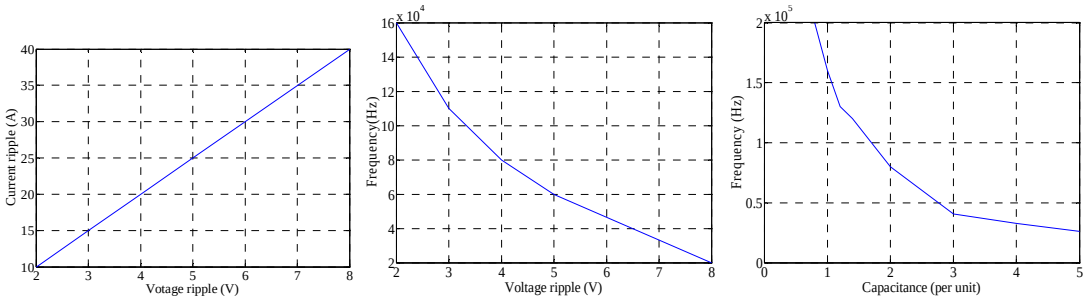
where ΔV_{dc} is the dc bus voltage ripple, C is the capacitance, and $\Delta Q = i \times \Delta t$, which is the change in the capacitor charge. The change in the capacitor charge depends on ΔV_{dc} and C. Thus, if C is kept constant, Δt, which is the charge or discharge time, is proportional to ΔV_{dc}. Moreover, the average switching frequency is inversely proportional to the voltage ripple.

On the other hand, if ΔV_{dc} is kept constant, then, the switching frequency is inversely proportional to the capacitance C.

Furthermore, the size of the APF inductor affects the filtering of the low frequency components. With a lower inductance, all the current and voltage waveforms show increasing low frequency ripple, as shown in Fig. 11. The frequency of oscillation is three times that of the inverter line frequency. This is because the inductance is too small to absorb the low frequency energy fluctuations in the dc bus.

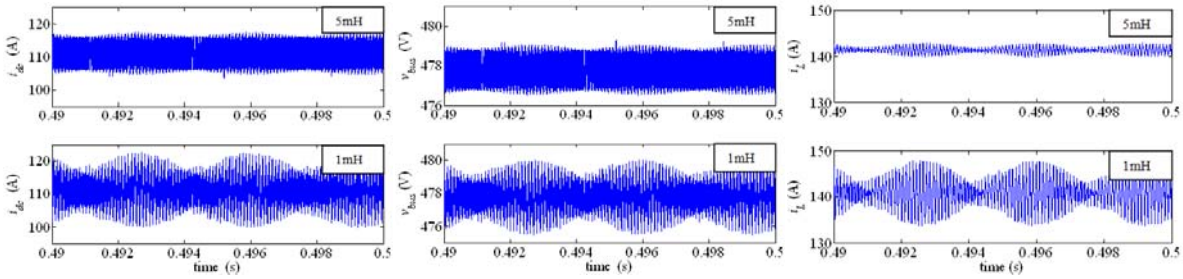
Although in theory an APF can replace or substantially reduce the capacitor size, there are several problems associated with the APF method which limit its practical application.

Essentially, this APF solution modulates the input harmonic current to a much higher frequency; thus, a small capacitor is enough for further filtering. High switching frequency is among the disadvantages with this solution. It will be hard to find power devices that can work at high frequencies at these power levels. Moreover, the switching losses of the APF make up a significant portion of the losses in the inverter.



(a) **(b)** **(c)**

Fig. 10. Parameter dependence: (a) = p-p current ripple vs p-p voltage ripple, (b) = switching frequency vs p-p voltage ripple, and (c) = switching frequency vs capacitance.



(a) **(b)** **(c)**

Fig. 11. Effects of filter inductance: (a) = input current, (b) = dc bus voltage, and (c) = APF inductor.

Another disadvantage is the high inductor current. The inductor current is around one-half of the maximum load current; in this case, it is 110 A. Thick coil wire is necessary for high inductor current. This means additional volume and weight for the inductor and high equivalent series resistance loss.

Although the inductor is much more reliable and long lasting than the capacitor, the power switches and diodes introduced in the APF method can decrease the reliability.

Conclusion

This project evaluates a solution for reduction of the bulky dc bus capacitor by using an APF in a three-phase traction system. Detailed operation modes are presented, and the simulation of this method is described. With this APF control method, the dc bus capacitor can be dramatically minimized, from 2,200 µF to 100 µF. However, because of the high operation frequency and the large inductor current, the size and weight of the APF, and the loss associated with the additional semiconductor switches, the APF method is still far from being practical in a traction drive inverter.

Publications

S. Li, B. Ozpineci, and L. M. Tolbert, "Evaluation of a Current Source Active Power Filter to Reduce the DC Bus Capacitor in a Hybrid Electric Vehicle Traction Drive," 2009 IEEE Energy Conversion Congress and Exposition.

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Patents

None.

4.3 High Temperature, High Voltage Fully Integrated Gate Driver Circuit

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Objectives

- Increase the current drive of the high temperature gate driver circuit.
- Improve the gate driver design to make it more robust against temperature variation.
- Incorporate three protective features with the core gate driver circuit: undervoltage protection, short circuit protection (SCP), and thermal shutdown.
- Insert multiple on-chip voltage regulators in the same die.

Approach

- Make use of the bipolar complementary metal-oxide semiconductor (CMOS)–double diffused metal-oxide semiconductor (DMOS) on silicon-on-insulator (SOI) process features to optimize the gate driver design for high ambient temperature operation.
- Test different types of wide bandgap semiconductor power switches with the driver circuit.

Major Accomplishments

- Designed and taped out the third generation (3G) gate driver circuit, which has current drive strength of more than 5 A at room temperature.
- Optimized design by making some of the critical functional blocks in the 3G gate driver circuit temperature-insensitive.
- Incorporated multiple voltage regulator circuits in the gate driver chip.
- Integrated SCP, undervoltage lockout (UVLO), and thermal shutdown circuitries with the core gate driver circuit.

Future Direction

- Results of 2009 chip research will be used to identify circuit blocks requiring design improvements, and design modifications.
- The circuit topology and layout will be enhanced to decrease the area of the gate driver chip and enhance robustness over a wide temperature range.
- Desaturation methods will be explored for SCP design.
- Power switch gate current monitoring circuitry will be added in the fourth generation gate driver chip.

Technical Discussion

The goal of this project is to develop an SOI-based high temperature, high voltage gate driver integrated circuit with high drive current capability for wide bandgap (WBG) power switches. Power electronics in

future electric vehicles (hybrid, plug-in hybrid, and full-electric) are expected to use WBG-based power devices which are capable of working at much higher ambient temperatures than the conventional silicon-based power switches of today. Implementation of these power modules in vehicles will allow the use of air cooling for electronics under the hood. To obtain the full advantage of the high temperature capability of WBG devices, the associated control electronics (such as gate driver circuits) also need to operate at higher temperatures with minimal thermal management. By placing the gate driver circuit close to the power switches, system reliability as well as performance can be improved.

Third Generation Gate Driver Circuit

Circuit design, simulation, layout, post layout simulation, and high temperature packaging of the 3G gate driver circuit with on-chip voltage regulators, SCP, UVLO circuit, and temperature supervisory circuit have been completed. Figure 1 shows the block diagram level schematic of the 3G gate driver circuit. Compared with its earlier prototype [second generation (2G)] this version of the gate driver circuit comprises several modifications and improvements in the core driver circuit.

The Schmitt trigger buffer added in the input stage of the gate driver circuit is designed to block any false or partial level-changing noise in the incoming logic signal. The output of the Schmitt trigger is a noise-free logic level signal. This input stage also incorporates a three-input NOR gate to generate an active high enable signal using the feedbacks received from the protective circuits (on-chip SCP unit, UVLO circuit, and thermal shutdown circuit) newly added to this prototype. If any of the three protection circuits sends a logic high signal indicating a fault condition then the enable signal becomes LOW and pulls down the logic input to V_{SS} (lowest rail voltage) so that the gate driver output is also pulled down to the lowest rail voltage to turn OFF the power switch.

An improved temperature-independent dead-time controller circuit has been included in this generation for complementary ON and OFF operation of the high voltage n-channel metal-oxide semiconductor (NMOS) transistors in the half bridge output stage. This will reduce the power consumption of the chip and will ensure the reliability of the circuit. Overlapping turn-on of both transistors will create a short circuit between the rail voltages, resulting in large short circuit or “crowbar” current. This large current will increase the die temperature much higher than the ambient temperature. To ensure a break-before-make type operation, a temperature-independent dead-time controller circuit has been designed to generate two nonoverlapping copies of the incoming logic signal.

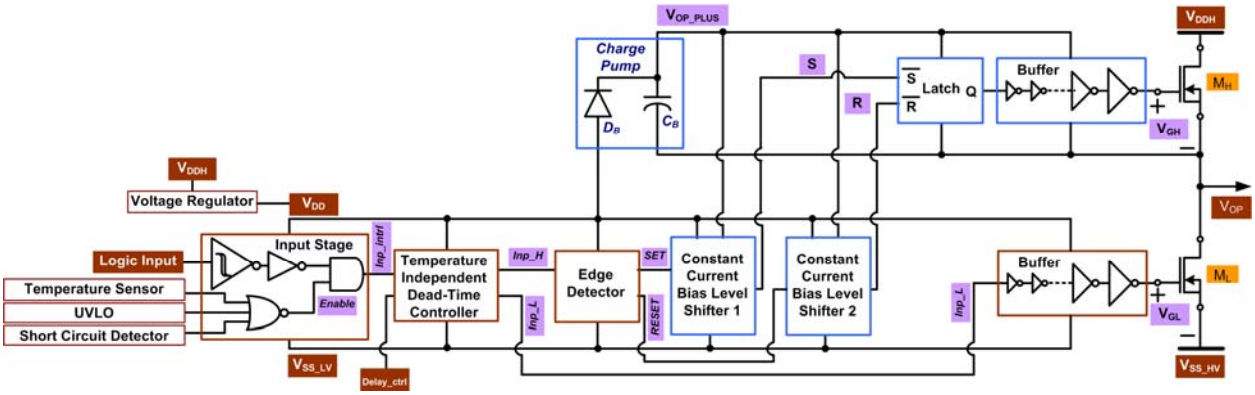

Fig. 1. Schematic of the high temperature, high voltage gate driver circuit with high output current.

Figure 2 shows the schematic of the proposed dead-time controller circuit. The main building block of this dead-time controller circuit is the adjustable delay controller circuit that can inject a temperature-independent phase lag to an incoming logic signal. A temperature-independent current bias circuit has been designed to provide constant current biasing to the adjustable delay controller circuit. Figure 3 shows the schematic of the temperature-independent current bias network developed using the zero-temperature coefficient (ZTC) [1] bias conditions of the NMOS and the p-channel metal-oxide semiconductor (PMOS) transistors. Figure 4 shows the schematic of the adjustable delay controller circuit with the temperature-independent bias network. Constant bias voltage is supplied to the gates of all the PMOS transistors, which source constant pull-up currents to the inverters, and thus capacitors get charged by a constant current across the entire temperature range. Similarly, the constant bias voltage is provided to all the NMOS transistors, which sink the constant pull down current from the inverters. This ensures the same rate of discharge of the capacitors over temperatures. Because the capacitors get charged and discharged by constant currents for the entire temperature range, the phase shift injected by this circuit remains virtually constant over the temperature range.

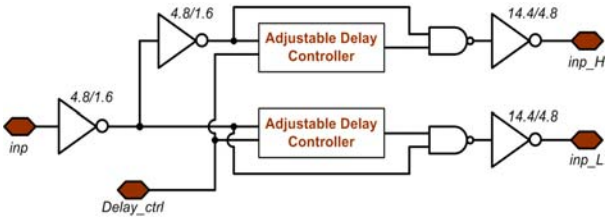

Fig. 2. Temperature-independent dead-time controller circuit.

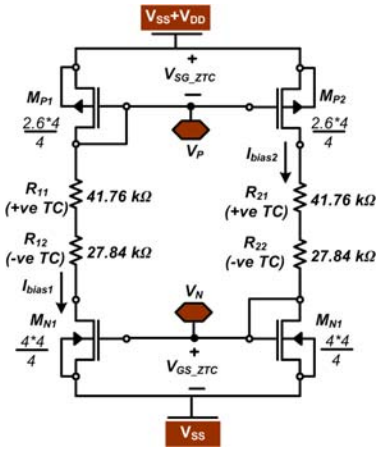

Fig. 3. Schematic of the temperature-independent current bias network.

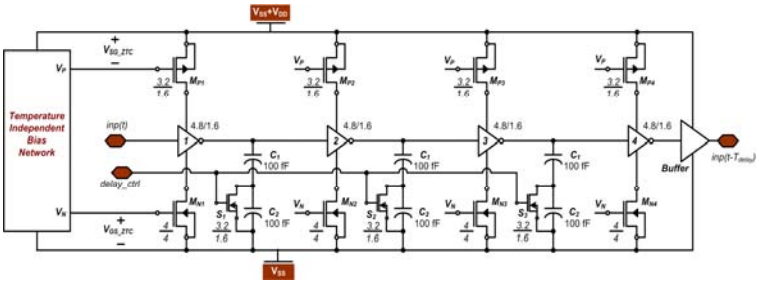

Fig. 4. Schematic of the temperature-independent adjustable delay controller circuit.

A constant current biased level shifter circuit has been designed for this version of the gate driver circuit. The main philosophy of the level shifter circuit is to convert the logic level voltage (SET and RESET) into currents and then, on the high voltage side, convert this current back into a voltage referenced to the high-side voltage. Constant current bias is guaranteed through the ZTC biasing of the PMOS and the NMOS current mirrors in the level shifter circuit as shown in Fig. 5.

The high-side (M_H) buffer (see Fig. 1) used to drive the M_H high voltage NMOS (HVNMOS) transistor has been redesigned using only low voltage devices (5 V PMOSs and NMOSs). In the previous design 45 V devices were used for this buffer to keep all the devices within the safe operating area. Because of this modification, the same buffer structure can be used for

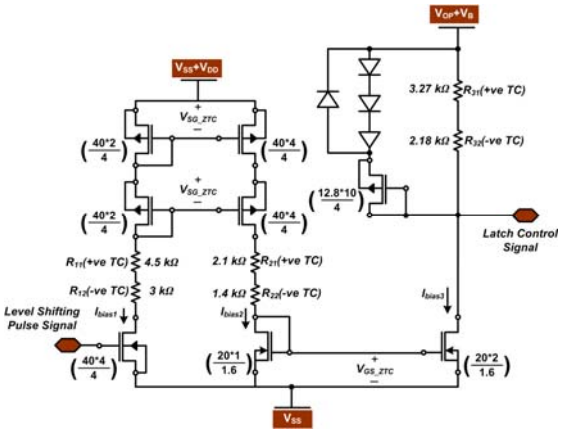

Figure 5. Schematic of the temperature-independent level shifter circuit.

both the HVNMOSs in the half bridge. This generates symmetric gate drive signals for both low side (M_L) and M_H transistors. This modification also makes both top side and bottom side buffers in the 3G design symmetric.

More HVNMOS transistors are included in the transistor array forming the half bridge output stage to increase the current driving capability of the driver circuit. In this version, a total of 900 high voltage (45 V) NMOS devices with aspect ratio of 40/1.6 are connected to form the M_H and M_L transistors. Figure 6 shows simulation results of the 3G gate driver circuit at −60°C, 95°C, and 250°C.

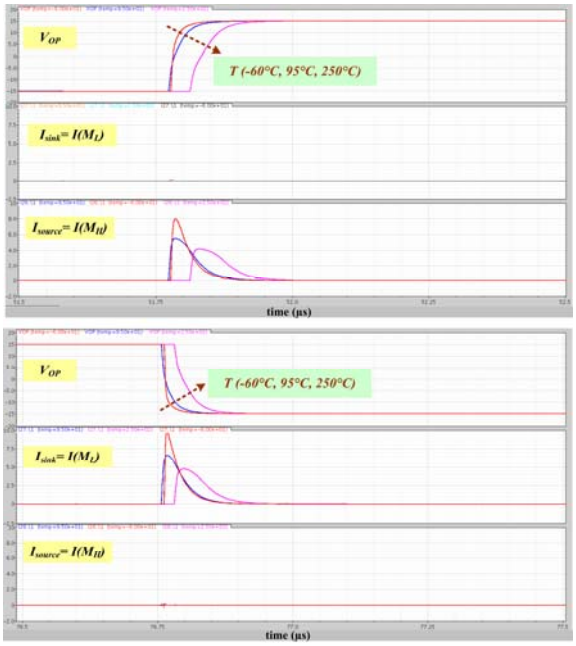

Fig. 6. Simulation results for the proposed high temperature gate driver circuit at different temperatures (*Red: −60°C, Blue: 95°C, and Pink: 250°C*).

On-Chip Voltage Regulator 1

The new on-chip voltage regulator incorporated with the 3G gate driver circuit has been designed based on the commercial LM723 regulator topology. Zener diodes have been used to provide reference voltages and generate bias currents. This 723 regulator topology generally consists of three subcircuit sections: reference voltage generator, error amplifier, and current drive. The specific needs of the gate driver project require additional considerations for this linear regulator. The supply voltage (V_{DDH}−V_{SS}) variation from 10 V to 30 V creates a need for pre-regulation of the supply to allow the regulator to accurately supply the required 5 V. Zener diodes were again used to generate a pre-regulation voltage of ~9.5 V to supply the regulator circuit. Pre-regulation stabilizes the output voltage and limits voltage across the devices implemented in the regulator, allowing more optimal devices to be used to generate the output voltage. The current requirement of the gate driver necessitates that the voltage regulator be able to supply high current levels without varying the output voltage. An HVNMOS pass device provides the current drive at the output.

Figure 7 shows the block diagram for the proposed 723-based voltage regulator design. The Zener reference generator provides a reference voltage of ~7.1 V, while the three-stage operational amplifier provides a linear gain to output of 5 V plus the VGS voltage (gate source voltage) of the pass device (~6 V). To create an accurate, robust voltage regulator, this design allows the output voltage to be mainly dependent on the Zener breakdown voltage. Changes in the device parameters of the devices other than the Zener diode yield a very small change in the output voltage. This device independence yields exceptional consistency for this voltage regulator topology. Figure 8 shows the transistor level schematic of the implemented voltage regulator circuit. For clarity, this schematic omits the start-up circuits for the pre-regulator and the reference generator subcircuits. MOS-capacitors limit the band width for feedback loops and enhance stability for the voltage regulator. An on-chip output capacitor (in addition to a much larger off-chip capacitor)

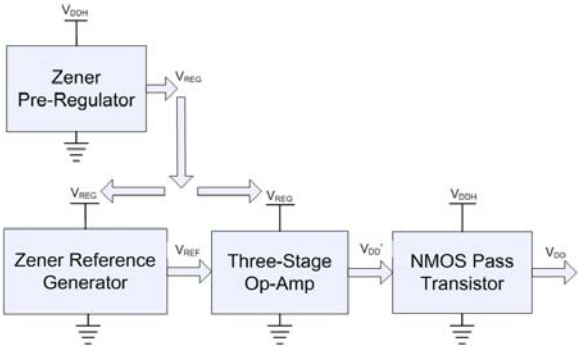

Fig. 7. Voltage regulator block diagram.

provides charge storage for the supply current during transient spikes, which occur during the switching cycles of the gate driver circuit. Figure 9 shows the voltage regulator output voltage versus temperature for various supply and load conditions.

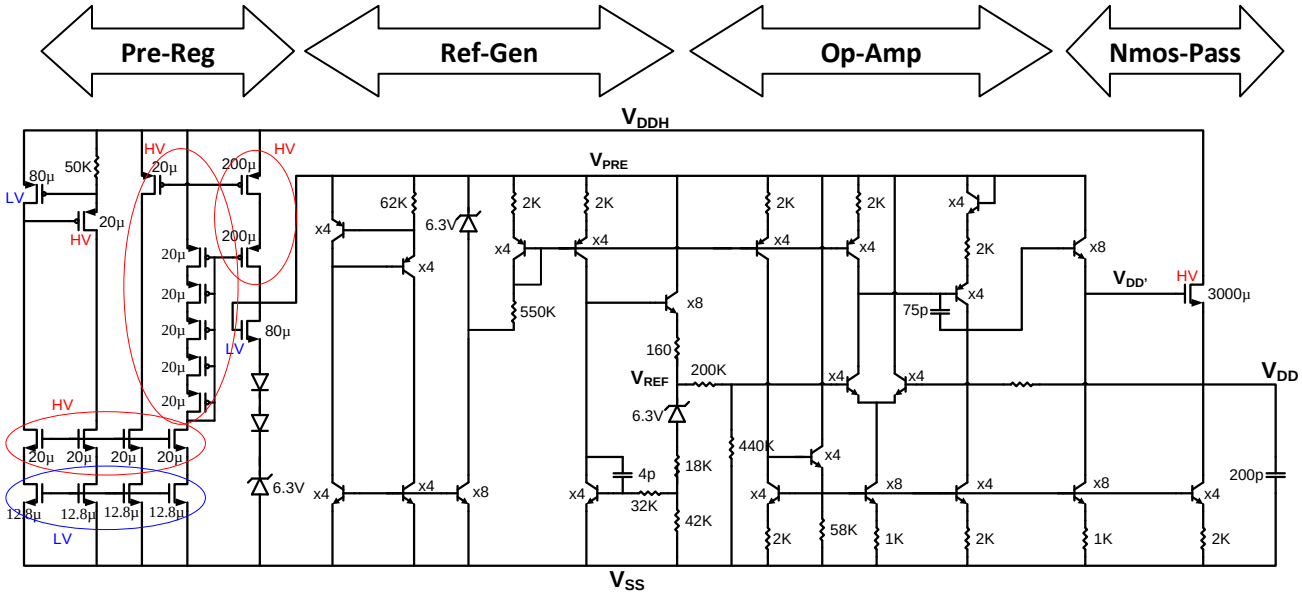

Fig. 8. Schematic of the new voltage regulator circuit.

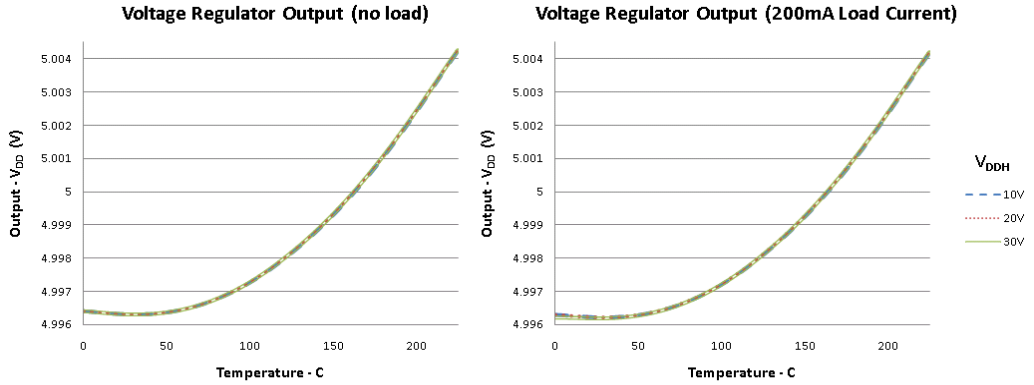

Fig. 9. Regulator 1 output voltage over temperature.

The variation of the output voltage for varying supply voltages and load currents is negligible when compared with the variation over the temperature range. The implementation of the pre-regulator and the supply rejection of the reference subcircuit allow for this negligible supply dependence over the 10 V to 30 V range. The Zener diode in the SOI process used for this chip development is designed with internal temperature compensation. The 18 kΩ resistor in series with the Zener diode at the reference voltage node provides additional temperature compensation for the reference voltage. This compensation allows the temperature variation for the voltage regulator to be reduced to less than 10 mV over a 225°C temperature range.

Figure 10 shows the Monte Carlo statistical results for 100 runs of process and mismatch variation. The nature of the 723 voltage-regulator design allows the output voltage to be nearly independent of all devices (except the Zener diode). Drastic changes in the parameters of the bipolar junction transistor and metal-oxide semiconductor field-effect transistor (MOSFET) devices as well the passive components yield negligible changes in the output of the regulator. Independence on the passive components (specifically resistors) is critical for accurate, consistent regulator performance due to the inherent inconsistency of the on-chip resistors. As a result of this robust design, the regulator will yield consistent results from chip to chip. In addition to robustness against fabrication related process variations and device mismatches, this regulator design will yield consistent results even with poor device models. (See Table 1 for a summary of the preceding.)

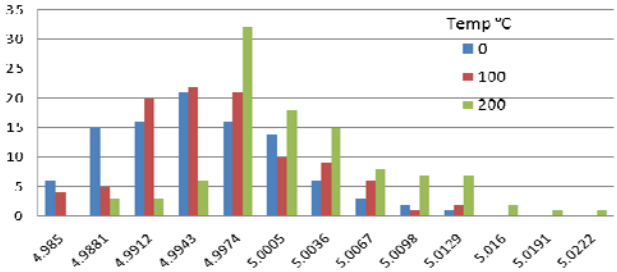

Fig. 10. Monte Carlo analysis for process and mismatch variation.

Table 1. Summary of Voltage Regulator Specifications

Nominal output voltage	5 V
Output current range	0–250 mA (ΔV_{DD} < 70 µV)
Supply voltage range (V_{DDH}–V_{SS})	8.4 V–45 V
Temperature variation	36 µV/°C
Line regulation	2 µV/V @ 200°C
Process and mismatch variation (100 runs)	~40 mV

On-Chip Voltage Regulator 2

The on-chip voltage regulator circuit which was first incorporated in the 2G gate driver circuit has been redesigned to increase its current drive strength. Figure 11 is a schematic of this modified high voltage, high temperature linear voltage regulator circuit. This step-down voltage regulator is needed to convert the unregulated high input dc voltage (V_{DDH}) to a regulated nominal CMOS voltage (V_{DD}). This step-down voltage regulator will supply voltage to the low-side buffer and other digital and analog circuits inside the gate driver circuit.

Fig. 11. Schematic of the high voltage, high temperature linear voltage regulator circuit.

This high temperature linear voltage regulator consists of a pre-regulator, bandgap voltage reference (BGR), temperature stable current reference, and voltage regulator. The pre-regulator reduces the V_{DDH} voltage to two separate supply voltages, 9 V and 5.6 V. The 9 V supply is connected to the cascode current mirror load of the error amplifier and the reference current generation circuit (IREF2). The 5.6 V supply is connected to the BGR, the reference current generation circuit (IREF1), and the input pair of the error amplifier. The pre-regulation scheme also helps enhance rejection of the supply noise in the V_{DDH} rail. Figure 12 depicts a simplified schematic of the voltage regulator circuit. Several high voltage n-type DMOS transistors are connected in parallel to work as a pass transistor. The error amplifier, the feedback resistor, and the pass transistor form a negative feedback loop.

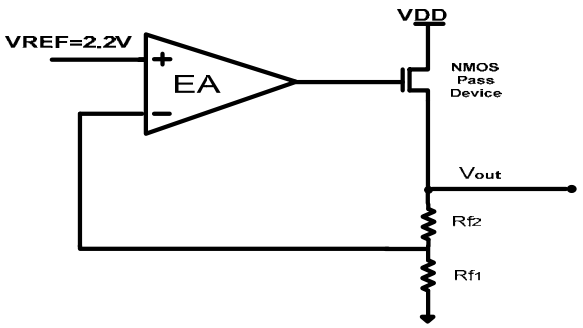

Fig. 12. Block diagram of linear voltage regulator.

The high temperature linear voltage regulator requires a high performance error amplifier. A temperature stable biasing current will prevent the power consumption of the error amplifier from increasing needlessly over temperature and preserve its stability. The design of a high performance wide temperature range error amplifier depends on the availability of a stable current reference. An error amplifier [operational transconductance amplifier (OTA)] is the fundamental building block of the linear voltage regulators. Its higher open-loop gain will enhance the overall performance of the high temperature linear voltage regulator. Figure 13 shows the schematic of a PMOS input pair folded cascode OTA, which has been selected as the error amplifier for this regulator. The PMOS input pair offer wider input common-mode range and empirically lower flicker noise compared to their NMOS counterpart. By using a cascode current mirror load at the output node, the folded cascode OTA has a higher common mode rejection ratio, power supply rejection ratio, and dc gain than simple Miller OTA topology.

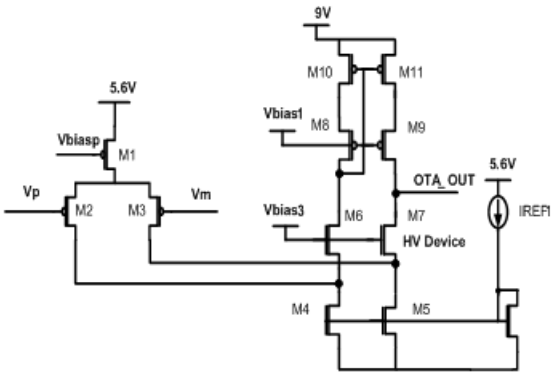

Fig. 13. Schematic of folded cascode amplifier.

Figure 14 shows the phase margin of the high temperature linear voltage regulator as a function of load current. The phase margin increases with increased temperature during heavy loading conditions. Figure 15 shows a simulation at 175°C of the high temperature linear voltage regulator that supplies 5.3 V to the V_{DD} rail of the gate driver circuit. The low-side buffer draws 125 mA dynamic current. The voltage regulator consumes a total of 0.6 mA quiescent current during zero load current condition at 175°C; the lower quiescent current can improve the efficiencies of both the regulator and the gate driver. The pole swap techniques proposed in this work can extend the range of the system stability to 4 decades of the load current (tens of µA to 200 mA) variations.

Specifications for the voltage regultor are summarized below.

- The voltage regulator can supply 200 mA and 5 V output.
- Includes pole swap compensation.
- Less than 100 mV voltage droop when loaded with the gate driver circuit.
- Wide load (10 µA to ~200 mA) range stability.

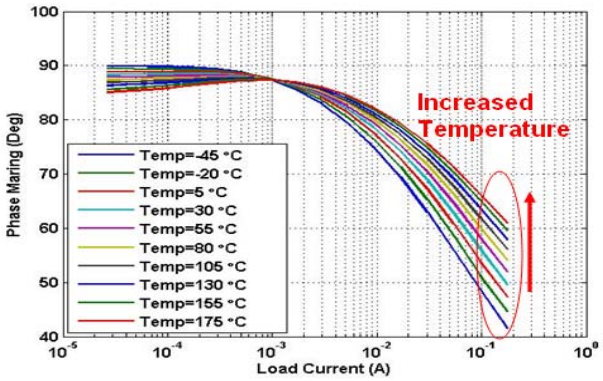

Fig. 14. Phase margin of the high temperature linear regulator at different temperatures.

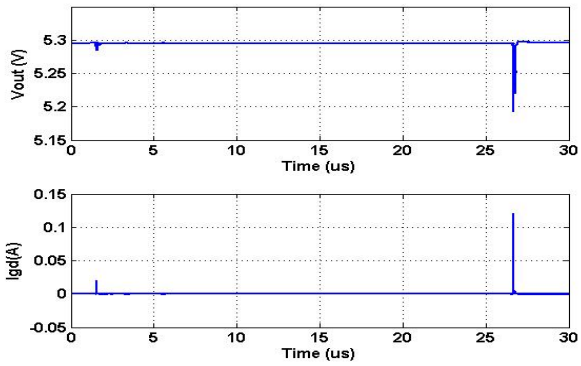

Fig. 15. Simulation of high temperature linear voltage regulator at 175°C.

Undervoltage Lockout Circuits

To prevent erroneous operation of the gate driver circuit due to significant droop in the rail-to-rail voltages, UVLO circuits have been incorporated in this chip. UVLO circuits monitor the different bias voltages and, in case of large voltage drops (below 80% of the desired levels), send a feedback signal to the gate driver circuit to indicate a fault condition. The gate driver circuit has two critical bias voltages:

1. V_{DD} to V_{SS} rail-to-rail voltage of 5 V and
2. V_{DDH} to V_{SS} rail-to-rail voltage which can vary from 10 V to 30 V depending on the power switch that this gate circuit is controlling.

Three different UVLO circuits have been designed to monitor these two critical rail-to-rail voltages. Figure 16 shows the configuration of these UVLO circuits. "UVLO 1" monitors the V_{DDH}–V_{SS} rail-to-rail voltage, and both the "UVLO 2" and "UVLO 3" circuits monitor the V_{DD}–V_{SS} voltage difference. The UVLO 2 circuit is biased by the V_{DDH} voltage whereas UVLO 3 is biased by the same V_{DD} voltage that this circuit is monitoring. This redundancy is provided to find the optimum UVLO circuit topology for future iterations of the chip.

Outputs from these three UVLO circuits are passed through an OR gate to generate a single feedback signal for the gate driver circuit. The dotted blue lines in Figure 16 represent off-chip connections in the test board. These external connections allow the independent tests of each of the three UVLO circuits.

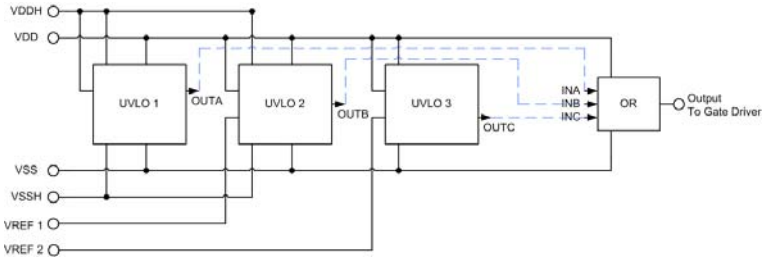

Fig. 16. Interconnections for different UVLOs.

Figure 17 shows the top level design of a UVLO circuit. A fraction of the V_{DD} voltage, generated by using the resistive divider, is compared to a reference voltage. This reference voltage can either be generated by an on-chip bandgap reference circuit or be supplied from an off-chip source. Output of the comparator circuit is then passed through a Schmitt trigger to prevent oscillation due to partial removal of the fault in the rail voltage. This circuit will generate logic low output as long as the V_{DD} rail voltage remains at or above 80% of its desired value. However, if the rail voltage drops below this threshold level, then this UVLO circuit will generate a logic high signal indicating a fault condition in the system.

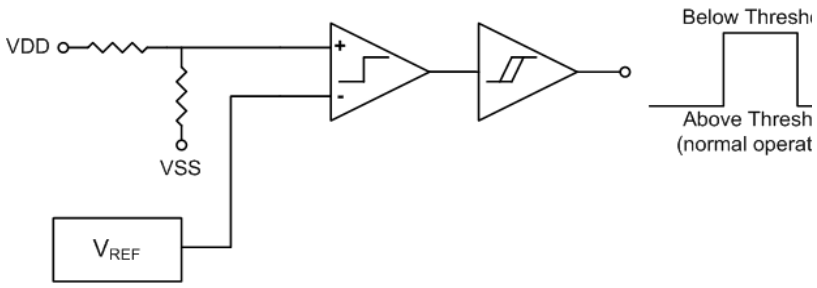

Fig. 17. UVLO (V_{DD} to V_{SS}) circuit topology.

Figure 18 shows the UVLO 1 circuit which monitors the V_{DDH} to V_{SS} rail-to-rail voltage. This voltage difference can be 30 V, 20 V, or 10 V depending on the type of WBG power switch that this gate driver is driving. This circuit uses a comparator with hysteresis. R_1 and R_2 in the figure are actually a network of resistors in a resistor bank. This gives the user an option to select the resistance needed from the bank depending on the voltage difference from V_{DDH} to V_{SSH}. The voltage, V_{REF}, is set using a resistor and a Zener diode, and its value is around 6 V to 7 V. Figure 19 shows the schematic of the comparator circuit with internal hysteresis. This comparator also has an internal clamping circuit on the output to limit the output voltage swing from 0 V to 5 V.

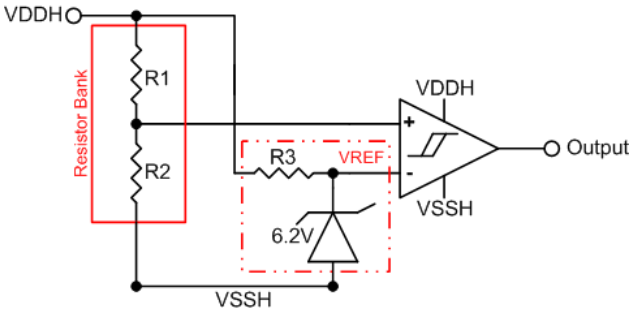

Fig. 18. UVLO (V_{DDH} to V_{SSH}) circuit topology.

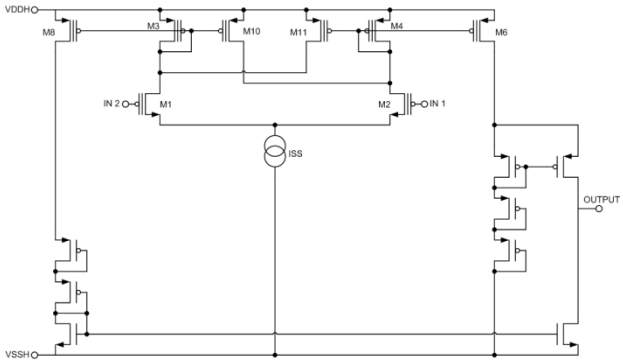

Fig. 19. Schematic of the comparator circuit with hysteresis.

Table 2 summarizes the schematic level simulation results of all three UVLO circuits for both room temperature and 200°C ambient temperature.

Table 2. UVLO Circuit Simulation Results (output of the OR gate)

30 Volt Test			**20 Volt Test**			**10 Volt Test**		
UVLO 2-3 (V)	Temp (C)	% of Supply Voltage	UVLO 2-3 (V)	Temp (C)	% of Supply Voltage	UVLO 2-3 (V)	Temp (C)	% of Supply Voltage
4.587	27	91.74	4.5215	27	90.43	4.614	27	92.28
4.534	200	90.68	4.534	200	90.68	4.587	200	91.74
UVLO 1 (V)	Temp (C)		UVLO 1 (V)	Temp (C)		UVLO 1 (V)	Temp (C)	
24.156	27	80.52	16.55	27	82.75	8.831	27	88.31
28.228	200	94.093	18.25	200	91.25	9.57	200	95.7
UVLO 1-2-3 (V)	Temp (C)		UVLO 1-2-3 (V)	Temp (C)		UVLO 1-2-3 (V)	Temp (C)	
4.574	27	91.48	4.5215	27	90.43	4.6407	27	92.814
27.43	27	91.433	18.3	27	91.5	9.2019	27	92.019
4.601	200	92.02	4.654	200	93.08	4.68	200	93.6
27.036	200	90.12	18.3	200	91.5	9.387	200	93.87

Short Circuit Protection

Power transistors used in motor drive applications typically need protection against failure under external fault conditions. Such faults mostly result from the occurrence of a short circuit at the load end and can cause very high surge currents flowing through the power devices. Hence in most power switch applications, SCP circuits are used to sense faults and turn OFF the transistors by shutting down the gate driver output. Figure 20 shows the SCP block in connection with the gate driver circuit and the power switch that this driver is controlling.

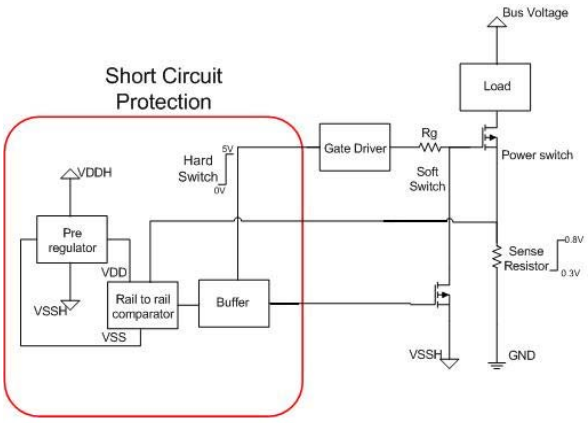

Fig. 20. Block diagram of short circuit protection.

To sense the current passing through the power switch, an off-chip shunt resistor is placed in the load current path. Voltage across this resistor senses the load current. This voltage is then fed to the on-chip SCP block where it is compared to a reference voltage to determine whether there exists a fault condition or not. One main feature of this circuit is its ability to work for both MOSFET and junction field-effect transistor switches, which require very different gate voltages for their switching operations.

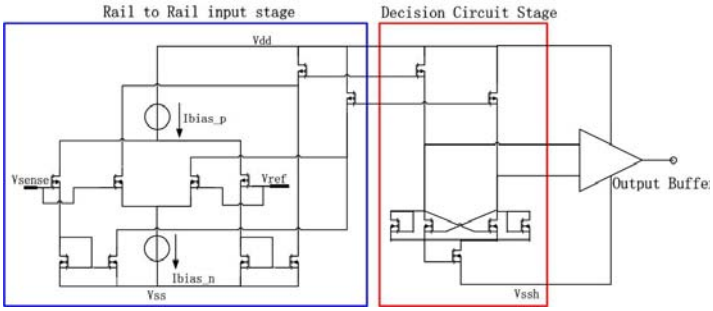

Fig. 21. Rail-to-rail comparator block.

A rail-to-rail comparator (shown in Fig. 21) is designed to fit in different supply voltages. This comparator circuit consists of three stages: the input rail-to-rail preamplifier, a positive feedback decision stage, and an output buffer. The preamplifier stage isolates the input of the comparator from switching noise coming from the decision circuit. The decision circuit uses positive feedback to increase the speed of determining whether there is a fault current. The output buffer amplifies this information and outputs a digital signal. The latter two stages also work like a level shifter which converts a ground referred input signal to a 5 V signal which is in reference to the lowest voltage supply (V_{ss}).

This SCP block can provide hard switch fault (HSF) protection to the gate driver circuit. HSF refers to the condition when there is a large fault current going through the power switch. This action will trigger the SCP to lower the load current by decreasing power switch gate voltage. If the fault current still exists after several microseconds, then a logic high signal is sent to the gate driver circuit to turn off the power switch completely.

Figure 22 shows the simulation result for HSF protection. This figure reveals that whenever HSF occurs the gate voltage of the power switch is first lowered by several volts and then the switch is turned OFF by the gate driver. Simulations for this SCP circuit were performed over a wide voltage range (−15 V to 15 V) at temperatures ranging from −50°C to 250°C. The main design features of this circuit can be summarized as follows.

- Working temperature range—50°C to 250°C.
- Working rail-to-rail voltage range—10 V to 30 V.

- Power device turn OFF time less than 10 µs.
- Limits the peak fault current (current level set by the sense resistor) by lowering the device gate voltage.
- Insensitive to noise and nuisance trips (transient overcurrent ignored).
- Does not affect the switching and conduction performance of the power switch.

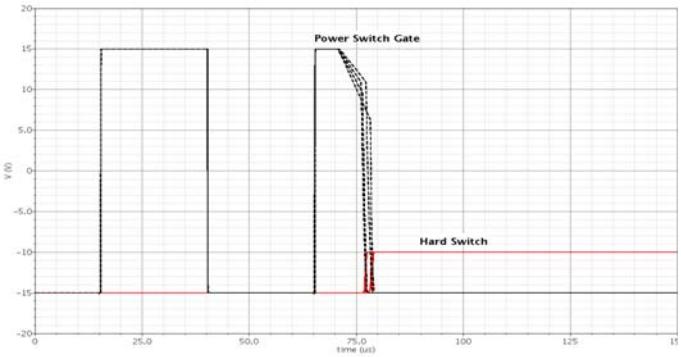

Fig. 22. Simulation result of HSF condition.

Ultralow-Power Thermal Shutdown Circuit

A new on-chip temperature supervisory circuit has been integrated in the 3G gate driver chip to provide protection against excessive die temperature. This circuit is capable of detecting die temperatures greater than 150°C based on the exponential increase in diode leakage current with increase in temperature and using this to keep the power consumption of this circuit at a very low level in the desired temperature range (≤200°C). Figure 23 shows the measured and the simulated leakage current variation versus temperature plots for a p-n junction diode. As this figure shows, the diode leakage current remains negligibly small until the die temperature reaches 150°C and beyond, when it increases exponentially.

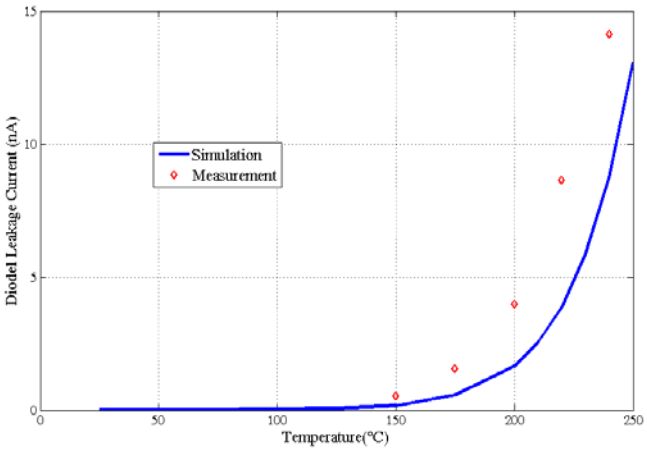

Fig. 23. Diode leakage current vs temperature.

Three different diode array blocks are used in the layout to select different upper levels of the allowed die temperature during testing. In all three cases, 15°C hysteresis is inserted between the fault activating threshold temperature and the fault removing threshold.

Figure 24 shows the schematic of the proposed temperature sensor circuit. The core temperature sensing element of this circuit is the reverse-biased diode, D_{sense}. Several (M number) p-n junction diodes are connected in parallel to increase the total leakage current, which depends on the die temperature. Diode leakage current, which is typically in the nA range, is first multiplied by the PMOS current mirror with 1 : 30 ratio and then converted to a voltage signal by the resistor R_L. The voltage drop across the resistor R_L is applied to the input of a Schmitt trigger which is buffered using a digital inverter circuit to drive the output node. With the increase in die temperature, voltage drop across R_L goes high, and once it exceeds the low-to-high threshold voltage of the Schmitt trigger, V_{out} transitions to a logic high (V_{DD}) indicating a fault condition. This feedback signal is sent to the input stage of the gate driver circuit. The high-to-low threshold voltage of the Schmitt trigger is set at a lower value corresponding to a 15°C reduction in die temperature. This hysteresis will prevent the circuit from being inappropriately triggered by a temporary recovery of the fault condition.

Figure 25 shows the sensor output signal, V_{out}, with the increase in die temperature for two different settings (*M=20* and *M=5*) of the reverse-biased diodes used as sensing elements. Twenty diodes in parallel set the fault triggering temperature to 230°C, whereas five diodes set the fault triggering

temperature to 263°C. Figure 25 also shows the logic high-to-low transition for V_{out} when the die temperature decreases. By proper design of the Schmitt trigger, 15°C hysteresis was provided in the sensor circuit. Power consumption of this sensor circuit is only 0.6 μW at 150°C, which goes to just under 10 μW at 200°C.

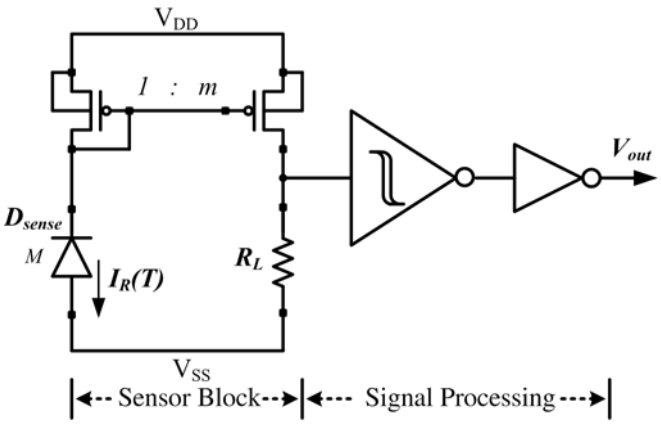

Fig. 24. Schematic of the proposed low-power on-chip temperature supervisory circuit.

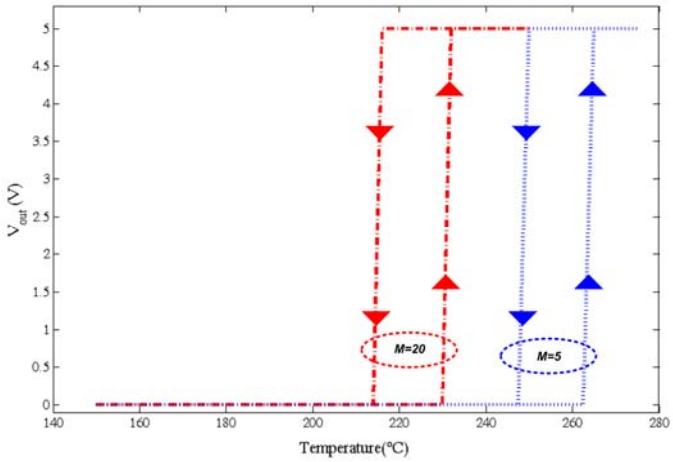

Fig. 25. Thermal shutdown circuit's output with the increase and decrease of die temperature.

High Temperature Packaging and Test Plan

Third generation gate driver bare dies have been assembled using 144-pin ceramic pin grid array packages as shown in Fig. 26. Several high temperature test boards made of polyimide materials are built to test the individual components in the gate driver chip. After completing the ongoing exhaustive individual component tests, the gate driver circuit will be tested in conjunction with the voltage regulator and all the protection circuits.

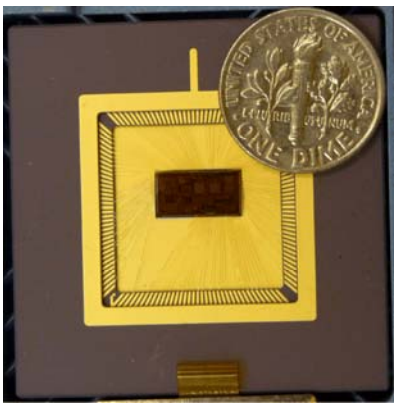

Fig. 26. Ceramic packaged 3G gate driver chip.

Conclusion

This challenging project involves the development and demonstration of a high temperature, high voltage gate driver circuit with large current sourcing/sinking capability to drive different types of WBG power switches. Successful integration of this gate driver circuit with WBG power switches will result in smart power converter modules with reduced volume and weight compared to the conventional all-silicon-based topologies. The 3G gate driver chip designed in 2009 has the current drive strength of 6 A at −50°C and 4 A at 200°C. Based on simulations, this driver can drive 10 nF capacitive loads in less than 50 ns at −50°C and less than 70 ns at 200°C. The switching frequency of the driver can reach 500 kHz, which will help to reduce the required size of the power converters by reducing the size of the filtering elements. Monte Carlo simulation across the wide temperature range (−50°C to 250°C) shows very little variation in the gate driver circuit performance.

The new on-chip voltage regulator incorporated in this chip is designed to generate 5 V bias voltage with 0 to 250 mA peak output current from the wide range of supply voltage (10 V to 30 V) made available to the driver circuit. It exhibits only 10 mV variations over 225°C temperature swings. The voltage regulator

design, which was first incorporated in the previous (2G) gate driver chip, has been redesigned to increase its current capability to 200 mA. Voltage droop for this second regulator circuit is less than 100 mV, and it exhibits good stability for a wide range of load currents (10 µA to 200 mA).

The SCP monitors the load current through the power switch that this gate driver chip is controlling. The UVLO circuits protect the gate driver from erroneous operation due to droop (below 80% of nominal) in the rail-to-rail voltages. The thermal shutdown circuit, which is designed to protect the chip from excessive die temperature (≥220°C), consumes less than 10 µW up to 200°C. In case of any fault, detected by one of these three protective circuits, a feedback signal is send to the gate driver circuit. In response to this fault detection, the gate driver circuit turns OFF the power switch to prevent system failure.

Publications

1. M. A. Huque, L. M. Tolbert, B. Blalock, and S. K. Islam, "SOI-based high-voltage, high-temperature integrated circuit gate driver for SiC-based power FETs," *IET Proceedings on Power Electronics,* Vol. 3, 2010, (*in press*).
2. M. A. Huque, L. M. Tolbert, B. J. Blalock, and S. K. Islam, *A High-Temperature, High-Voltage SOI Gate Driver IC with High Output Current and On-Chip Low-Power Temperature Sensor,* accepted for publication in 42nd International Symposium on Microelectronics (IMAPS 2009), San Jose, California, November 1–5, 2009.
3. M. A. Huque, S. K. Islam, B. J. Blalock, and L. M. Tolbert, "Diode leakage current based low power, on-chip high temperature sensor circuit," in *Proc. of 18th Annual Symposium on Micro- and Nano-technologies for Electronics, Photonics, Biosensors, and Alternate Energy Sources* (CMOC 2009), Yale University, New Haven, Connecticut, March 11, 2009, pp. 57–58.
4. M. A Huque, S. K. Islam, B. J. Blalock, C. Su, R. Vijayaraghavan, and L M. Tolbert, "Silicon-on-insulator based high-temperature electronics for automotive applications," in *Proc. of IEEE International Symposium on Industrial Electronics* (ISIE 2008), Cambridge, UK, June 30–July 2, 2008, pp. 2538–2543.
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1. F. S. Shoucair, "Analytical and experimental methods for zero-temperature-coefficient biasing of MOS transistors," *Electronics Letters,* Vol. 25(17), 1989, pp. 1196–1198.

Patents

None

4.4 Current Source Inverter

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Objectives

- Overall project objectives
  - Eliminate the drawbacks of the voltage source inverter (VSI) by switching to a current-source–based topology.
  - Reduce inverter cost and volume by 25% compared with the Toyota Prius inverter.
  - Improve inverter and motor lifetime.
  - Increase motor efficiency (10% loss reduction).
  - Increase constant-power speed range.
  - Reduce the cost and size of batteries in plug-in hybrid electric vehicles (HEVs).
  - Enable silicon carbide- (SiC-) based inverters to operate in elevated-temperature environments.
- Objectives for FY 2009 effort
  - Produce a design for a 55 kW current source inverter (CSI) to evaluate technical feasibility of the CSI for operation with a 105°C coolant.

Approach

- Use insulated gate bipolar transistor (IGBT) and diode chips with maximum junction temperature rated at 175°C.
- Redesign digital signal processing (DSP) and gate drive boards using components rated in the automotive temperate range of -40 to ~125°C.
- Estimate the switching and conduction losses of the IGBTs and diodes using an average loss modeling technique to generate heat loads.
- Determine requirements for the heat sink using an equivalent thermal circuit.

Major Accomplishments

- Derived analytical equations for computing the average losses of IGBTs and diodes in the CSI topology.
- Completed a custom IGBT module design for the CSI switch leg using Infineon IGBT and Semikron diode chips rated with maximum junction temperature of 175°C.
- Completed a design for a 55 kW CSI for operation with a 105°C coolant using the custom IGBT modules. The total capacitance is 390 μF. Estimated IGBT and diode junction temperatures are 148.2°C and 134.1°C, respectively, which are well within their safe operating region.
- Designed and fabricated DSP and gate drive boards for operation in the 105°C coolant environment using components rated in the automotive temperate range of -40 to ~125°C.

Future Direction

- Perform feasibility study of the V-I converter-based CSI for HEV electrical drive configurations using more than one motor.
- Continue the development of alternative inverter topologies using the CSI technology.

Technical Discussion

Background

Current electric vehicles (EVs) and HEVs use inverters that operate off a voltage source. They are called VSIs (Fig. 1a) because the most readily available and efficient energy storage devices, batteries, are inherently voltage sources. The VSI, however, possesses several drawbacks that make it difficult to meet FreedomCAR goals for volume, lifetime, and cost for an inverter operating with a high temperature (105°C) coolant. A VSI requires a very-high-performance direct current (dc) bus capacitor to maintain a near-ideal voltage source. Also, currently available capacitors that can meet the demanding requirements are costly and bulky, taking up one-third of the inverter volume and cost. The reliability of the inverter is also limited by the capacitors and further hampered by possible "shoot-through" of the phase legs making up a VSI (S_1-S_2, S_3-S_4, and S_5-S_6 in Fig. 1a). In addition, steep rising and falling edges of the output voltage in the form of pulse trains generate high electromagnetic interference (EMI) noises, which impose high stresses on the motor insulation, produce high-frequency losses in the copper windings and iron cores of the motor, and generate bearing-leakage currents that erode the bearings over time.

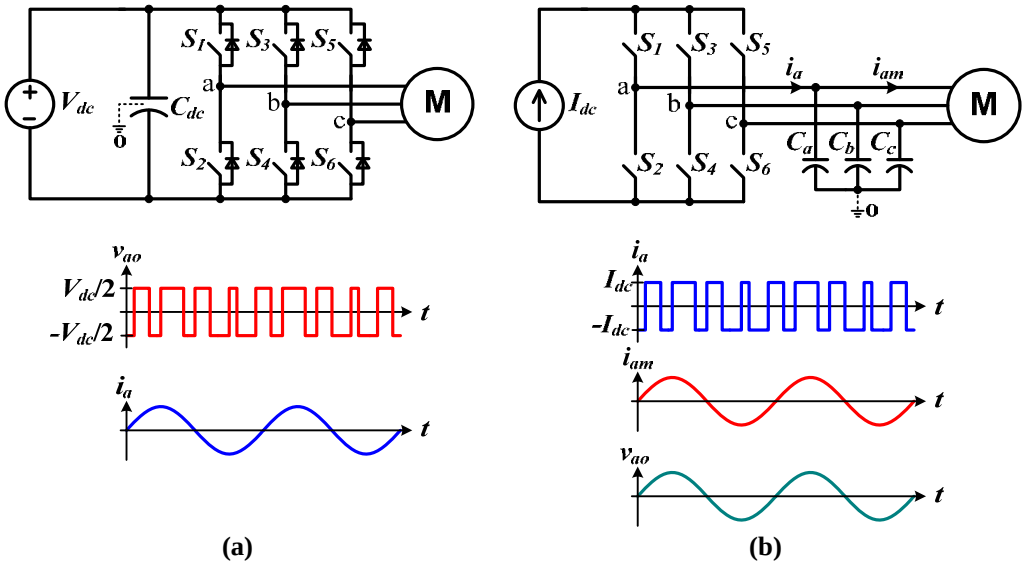

Fig. 1. Schematics of the two types of inverters and typical output voltage and current waveforms: (a) the VSI and (b) the CSI.

As the maximum operating junction temperature of the latest silicon IGBTs increases, the capacitor, in fact, presents the most difficult hurdle to operating a VSI in automotive high temperature environments. The function of the dc bus capacitor is twofold: (1) to maintain a near-ideal voltage source and (2) to absorb the ripple current generated by the switching actions of the inverter.

The root mean square value of the ripple current is proportional to the motor current with a maximum ratio of 50 to ~60%, depending on the pulse-width modulation (PWM) scheme. Currently, two types of dielectrics, polymer film and ceramics, are being pursued for use in high temperature environments. The polymer-film capacitor is the technology choice for HEVs currently on the market because of its benign failure mode and adequate ripple-current handling capability at lower coolant temperatures (about 70°C);

however, its ripple-current handling capability rapidly diminishes as the temperature increases. As a result, a significantly larger capacitor would be required in a higher operating temperature environment. On the other hand, although ceramic capacitors can still provide adequate ripple-current capability even at higher temperatures, their tendencies to produce catastrophic failures and their higher cost have made them unacceptable for HEV applications.

In addition, for the VSI to operate from a low voltage battery, a bidirectional dc-dc converter is needed. Figure 2 shows a widely used inverter topology with such a converter, where two additional IGBTs and an inductor are used for interfacing with a low voltage battery.

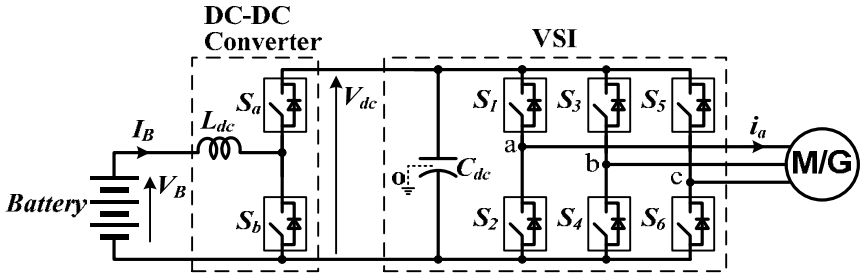

Fig. 2. A voltage source inverter with a bidirectional dc-dc converter for interfacing with a low-voltage battery.

All these problems could be eliminated or significantly reduced by the use of another type of inverter, the (CSI (Fig. 1b). The CSI requires no dc bus capacitors and uses only three alternating current (ac) filter capacitors of a much smaller capacitance. The total capacitance of the ac filter capacitors is estimated at approximately one-fifth that of the dc bus capacitor in the VSI. In addition, the CSI offers many other advantages important for EV applications: (1) it does not need antiparallel diodes in the switches, (2) it can tolerate phase-leg shoot-through, (3) it provides sinusoid-shaped voltage output to the motor, and (4) it can boost the output voltage to a higher level than the source voltage to enable the motor to operate at higher speeds. These advantages could translate into a significant reduction in inverter cost and volume with increased reliability, a much higher constant-power speed range, and improved motor efficiency and lifetime.

Two factors, however, have so far prevented the application of CSIs in HEVs. The first is the difficulty of incorporating batteries into a CSI as energy-storage devices; the second is the limited availability of power switches that can block voltages in both forward and reverse directions. IGBTs with reverse-blocking capability are being offered as engineering samples, and the technology is rapidly reaching the maturity needed for commercial production. This research aims to remove the remaining hurdles and bring the advantageous CSI to HEV applications by offering a new inverter topology based on the CSI but with a novel scheme to incorporate energy-storage devices. By significantly reducing the amount of capacitance required, the CSI-based inverter with silicon IGBTs will be able to substantially decrease the requirements for cooling systems and, further, could enable air-cooled power inverters in the future when wide-bandgap-based switches become commercially viable.

The overall objective of the research is to design, fabricate, test, and evaluate a 55 kW inverter prototype based on the novel CSI topology to replace the VSI for EV and HEV applications. Three major tasks will be carried out over a 3-year period: (1) modeling and simulation; (2) design, fabrication, and testing of a 55 kW prototype for operation with a 70°C coolant; and (3) feasibility evaluation of the CSI for operation with a 105°C coolant. In FY 2007, computer modeling and simulation was conducted to down-select an optimal interfacing circuit, and a conceptual design of a 55 kW inverter system was produced. Building on the FY 2007 activities, a 55 kW prototype was designed, fabricated, and successfully tested in

FY 2008. Test results show that (1) total capacitance was reduced to 195 µF, (2) a voltage boost ratio of up to 3.47 was attained, (3) an output voltage total harmonic distortion factor lower than 12.5% was achieved, and (4) measured motor leakage current at each motor terminal voltage was as low as 1.146 mA/V. The third task, feasibility evaluation for operation with a 105°C coolant, was carried out this year (FY 2009).

Average Loss Modeling for the Proposed CSI

Figure 3 shows a schematic of the proposed CSI with a battery-interfacing circuit. The interfacing circuit—with the help of the dc choke, L_{dc}—transforms the voltage source of the battery into a current source to the inverter bridge by providing the capability to control and maintain a constant dc bus current, I_{dc}. More important, the interfacing circuit also enables the inverter to charge the battery during dynamic breaking without the need for reversing the direction of the dc bus current.

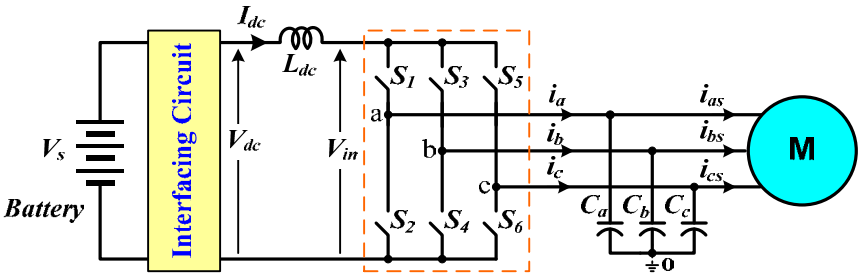

Fig. 3. Schematic of the proposed current-source-based inverter.

Whereas the VSI produces a voltage pulse train, the CSI generates a current pulse train in each phase output by turning on and off the switches, S_1–S_6, in the bridge according to a PWM strategy. The pulsed phase currents are then filtered by a simple filter network of the three capacitors, C_a, C_b, and C_c, leaving near sinusoidal currents as well as sinusoidal voltages to the electrical motor. The sinusoidal voltages are desirable for the motor because they eliminate problems with the VSI output voltages. These include pulse trains with steep rising and falling edges, which generate high EMI noises that impose high stresses on the motor insulation, produce high-frequency losses in the copper windings and iron cores of the motor, and generate bearing-leakage currents.

Generally, modulation schemes can be categorized into two main groups: carrier-based and space-vector schemes. Because of the duality between the VSI and CSI, it is possible to translate the modulation schemes between the two types of inverters. Switching tables of the VSI and the CSI are given in Table 1 and Table 2, respectively. The space-vector diagrams are given in Fig. 4.

Table 1. Switching Table of the VSI

Voltage vector	Top devices			Bottom devices			Phase voltages		
	S_1	S_3	S_5	S_2	S_4	S_6	V_{ao}	V_{bo}	V_{co}
V_0	0	0	0	1	1	1	0	0	0
V_1	1	0	0	0	1	1	V_{dc}	0	0
V_2	1	1	0	0	0	1	V_{dc}	V_{dc}	0
V_3	0	1	0	1	0	1	0	V_{dc}	0
V_4	0	1	1	1	0	0	0	V_{dc}	V_{dc}
V_5	0	0	1	1	1	0	0	0	V_{dc}
V_6	1	0	1	0	1	0	V_{dc}	0	V_{dc}
V_7	1	1	1	0	0	0	V_{dc}	V_{dc}	V_{dc}

Table 2. Switching Table of the CSI

Current vector	Top devices			Bottom devices			Phase currents		
	S_1	S_3	S_5	S_2	S_4	S_6	i_a	i_b	i_c
I_1	1	0	0	0	0	1	I_{dc}	0	$-I_{dc}$
I_2	0	1	0	0	0	1	0	I_{dc}	$-I_{dc}$
I_3	0	1	0	1	0	0	$-I_{dc}$	I_{dc}	0
I_4	0	0	1	1	0	0	$-I_{dc}$	0	I_{dc}
I_5	0	0	1	0	1	0	0	$-I_{dc}$	I_{dc}
I_6	1	0	0	0	1	0	I_{dc}	$-I_{dc}$	0
I_7	1	0	0	1	0	0	0	0	0
I_8	0	1	0	0	1	0	0	0	0
I_9	0	0	1	0	0	1	0	0	0

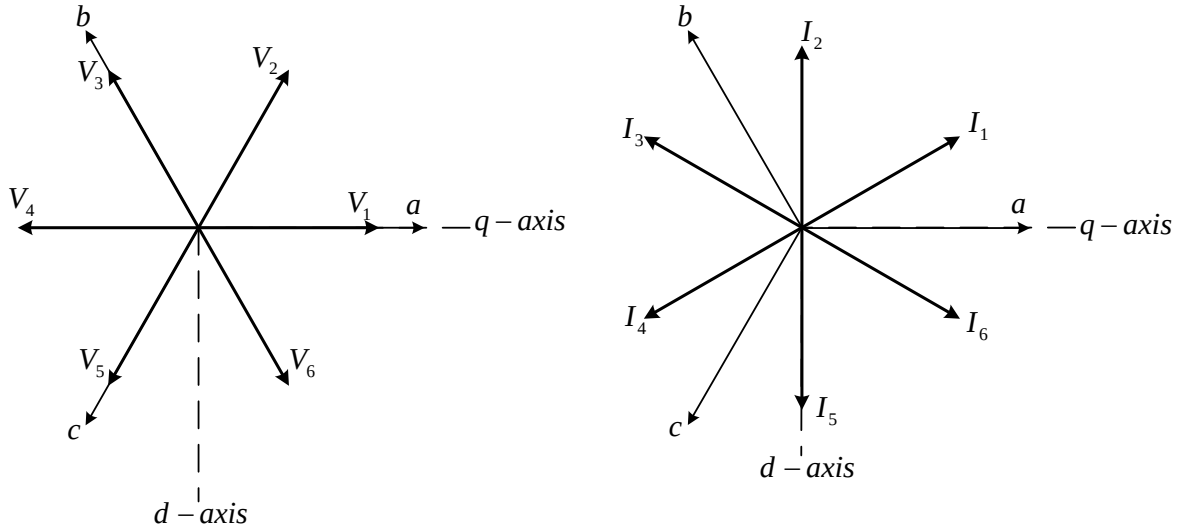

Fig. 4. Space-vector diagrams for the VSI (left) and CSI (right).

The voltage vector of the VSI can be mapped to the current vector of the CSI according to the rules given in Eq. (1), and the switching functions of the CSI can then be mapped from that of the VSI according to Eq. (2).

$$\begin{aligned} V_1 &\rightarrow I_6 & V_2 &\rightarrow I_1 \\ V_3 &\rightarrow I_2 & V_4 &\rightarrow I_3 \\ V_5 &\rightarrow I_4 & V_6 &\rightarrow I_5 \end{aligned} \quad . \tag{1}$$

$$\begin{aligned} S_{1i} &= S_{1v} \cdot S_{6v} + S_{0i} & S_{3i} &= S_{3v} \cdot S_{2v} + S_{0i} \\ S_{5i} &= S_{5v} \cdot S_{4v} + S_{0i} & S_{2i} &= S_{2v} \cdot S_{5v} + S_{0i} \\ S_{4i} &= S_{4v} \cdot S_{1v} + S_{0i} & S_{6i} &= S_{6v} \cdot S_{3v} + S_{0i} \end{aligned} \quad , \tag{2}$$

where the subscript "*v*" represents the switching function of the VSI and the subscript "*i*" represents that of the CSI; S_{0i} represents the zero sequence states of the CSI, I_7, I_8, and I_9. The zero sequence signals are there to balance the "ON" time intervals for the switches and will not affect the fundamental component; however, they can be used to minimize the switching losses. Table 3 gives the optimal zero sequence for each switching state.

Table 3. Optimal Zero Sequence

Current active vector	Next active vector	Sector	Optimal zero sequence
I_6	I_1	*I*	I_7
I_1	I_2	*II*	I_9
I_2	I_3	*III*	I_8
I_3	I_4	*IV*	I_7
I_4	I_5	*V*	I_9
I_5	I_6	*VI*	I_8

It should be noted that because of the phase angle difference between the voltage vectors and the current vectors, the direct mapping of the space vectors of the VSI to those of the CSI produces a 30° phase shift between the output current and the reference current.

The triangle carrier-based modulation produces two active zones, each composed of two active states arranged with different sequences. Zero states are located at both the beginning and the end of each active zone. The sawtooth carrier-based modulation, on the other hand, removes the zero state between the two active zones and combines the two active zones into one. Therefore, the latter may further reduce the amount of device switching over a switching cycle.

Space-vector PWM is another attractive method for digital control because of its inherent advantage of enabling direct calculations in the *qd* reference frame and straightforward implementation in digital controllers. The space-vector modulation methodology of a VSI can also be adapted to a CSI. The goal is to optimally use the three variables—two active vectors "a" and "b" and a zero vector—to generate the desired current vector. The process of implementation can be divided into three steps: (1) transformation of the commands from the abc stationary reference frame to the q-d stationary reference frame, (2) calculation of the time intervals of the vectors "a" and "b", and (3) generation of modulation signals based on the time intervals. Table 4 gives the normalized time interval for the two active and zero vectors for each sector.

Table 4. Normalized Time Intervals for the Two Active and Zero Vectors for Each Sector

Sector	First active vector (t_a)	Second active vector (t_β)	Zero vector (t_0)
I	$-\frac{i_c}{I_{dc}}$	$-\frac{i_b}{I_{dc}}$	$1-\frac{i_a}{I_{dc}}$
II	$\frac{i_b}{I_{dc}}$	$\frac{i_a}{I_{dc}}$	$1+\frac{i_c}{I_{dc}}$
III	$-\frac{i_a}{I_{dc}}$	$-\frac{i_c}{I_{dc}}$	$1-\frac{i_b}{I_{dc}}$
IV	$\frac{i_c}{I_{dc}}$	$\frac{i_b}{I_{dc}}$	$1+\frac{i_a}{I_{dc}}$
V	$-\frac{i_b}{I_{dc}}$	$-\frac{i_a}{I_{dc}}$	$1-\frac{i_c}{I_{dc}}$
VI	$\frac{i_a}{I_{dc}}$	$\frac{i_c}{I_{dc}}$	$1+\frac{i_b}{I_{dc}}$

The carrier-based PWM scheme can be realized by direct mapping from VSI counterparts and is thus simple and easy to implement with analog circuits. The active state intervals are calculated indirectly, and the sequence and ordering of the active states are implicit for the carrier-based PWM schemes; however,

with the space-vector PWM algorithm, the sequence, the ordering, and the period of the active states are all explicitly computed. Moreover, the sequence of the active states and null state can be arranged arbitrarily as long as the total time period for each switching cycle meets the desired value. The space-vector PWM algorithm is therefore good for digital control and was used in the prototype development.

Assume the interface circuit generates the output voltage, V_{dc}, proportional to the input voltage, V_s; that is,

$$V_{dc} = M_{dc} \cdot V_s \quad , \tag{3}$$

where M_{dc} is a control signal. The CSI switch network can be modeled by

$$i_a = S_1 \cdot I_{dc} - S_2 \cdot I_{dc}, \quad i_b = S_3 \cdot I_{dc} - S_4 \cdot I_{dc}, \quad i_c = S_5 \cdot I_{dc} - S_6 \cdot I_{dc} \quad . \tag{4}$$

The ac filter capacitors and dc link inductor can be described by Eqs. (5) and (6), respectively.

$$Cdv_{ao} / dt = i_a - i_{as}, \quad Cdv_{bo} / dt = i_b - i_{bs}, \quad Cdv_{co} / dt = i_c - i_{cs} \quad ; \tag{5}$$

$$L_{dc} pI_{dc} = V_{dc} - V_{in} \quad . \tag{6}$$

The input voltage, V_{in} can be calculated from the switching functions and the ac capacitor voltages as

$$V_{in} = v_{ao}\left(S_1 - S_2\right) + v_{bo}\left(S_3 - S_4\right) + v_{co}\left(S_5 - S_6\right) \quad . \tag{7}$$

The equivalent circuit of the CSI, which is essentially a boost converter, is shown in Fig. 5, in which the switching device *G* represents the switches of the CSI while the RL load represents a motor.

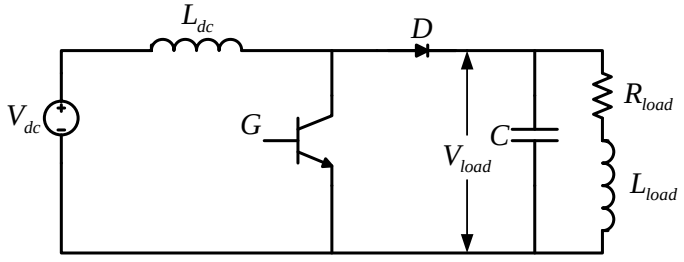

Fig. 5. Equivalent circuit of the CSI for voltage boosting.

The input and output voltages of the boost converter are related by

$$\frac{V_{load}}{V_{dc}} = \frac{1}{1 - D_{on}} \quad , \tag{8}$$

where D_{on} is the duty ratio of the switching device G. The duty ratio is equal to the shoot-through ratio and can be found for balanced three-phase stator currents by

$$D_{on} = 1 - \frac{3}{\pi} M \quad , \tag{9}$$

where *M* is the modulation index for the CSI. Equation (8) can be expressed as

$$V_{load} = \frac{\pi}{3M} V_{dc} \quad . \tag{10}$$

It is now apparent from Eq. (10) that the load voltage increases when the magnitude of the modulation index decreases. When the desired output currents are given, the multiplication of the dc link current and the modulation signals is fixed. Hence, if the modulation signals decrease, the dc link current needs to be increased to track the desired output phase current.

Design of Custom IGBT Switch Module

CSIs require switches capable of blocking voltage in both forward and reverse directions. While the reverse blocking IGBTs being developed by Fuji and other power device manufacturers work nicely in the CSI, the current ratings of the available modules do not yet meet the required power rating, and the maximum junction temperature of 150°C makes it challenging to design a cooling system for operating with a 105°C coolant [1][2]. Custom IGBT modules were therefore designed using IGBT and diode chips with maximum junction temperature rated at 175°C. The custom IGBT module is constructed using two pairs, each consisting of one IGBT and one diode in series connection, each pair forming a switch as shown in Fig.6(a). We selected the Infineon IGBT chip rated at 600 V/200 A and 175°C, part number SIGC100T60R3, and the Semikron diode chip rated at 175°C, SEMICELL CAL-Diode, for this application. Each switch comprises three IGBT chips connected in parallel and three diode chips also connected in parallel to obtain the required current rating, as shown in Fig.6(b). The chips are soldered on an AlN direct bonded copper substrate. The dimensions of the module are given in Fig.6(c), (d), and (e).

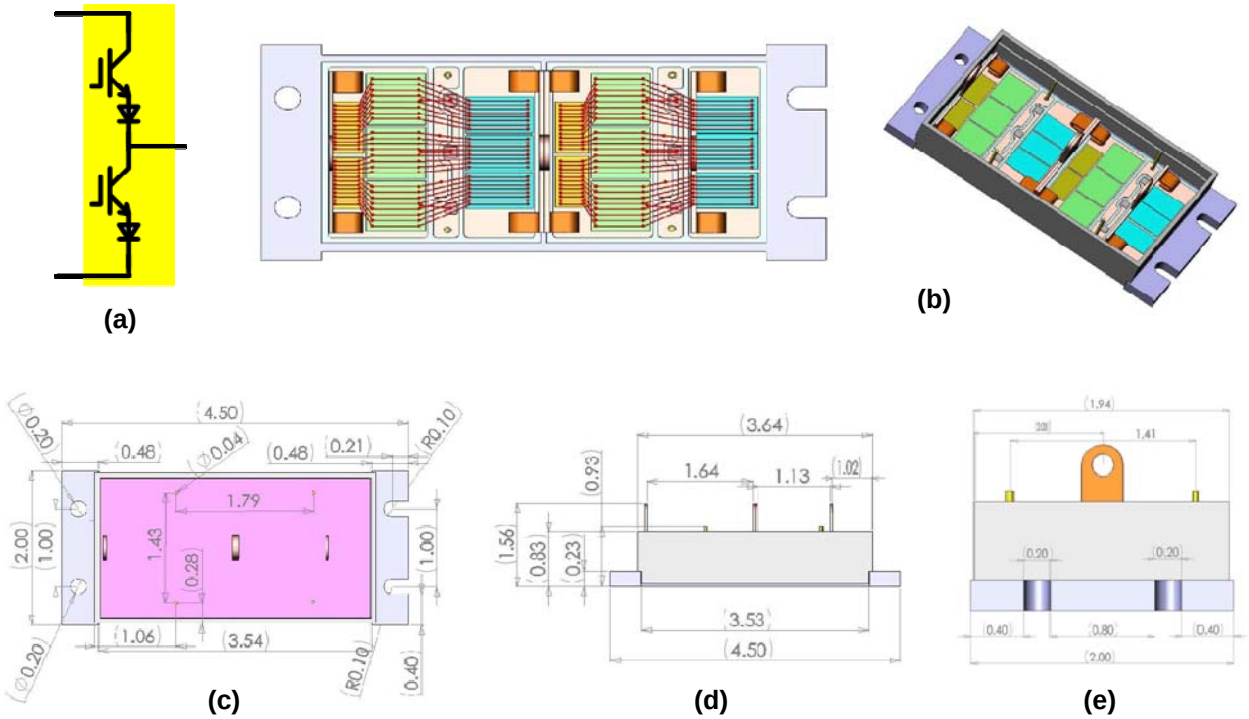

Fig. 6. Custom CSI switch leg module design: (a) switch configuration, (b) two views of chip layout, (c) top view, (d) front view, and (e) right view.

Since there must be one switch in the top and one in the bottom conducting, conduction loss, P_{Cont}, can be computed by

$$P_{Cont} = 2I_{dc}[(V_{CE(sat)} + V_{DF}) + I_{dc}(r_{igbt} + r_d)] \quad , \tag{11}$$

where $V_{CE(sat)}$ and V_{DF} are the IGBT saturation voltage and diode forward voltage drop, respectively; r_{igbt} and r_d are the IGBT and diode forward conducting resistance, respectively.

The averaged total switching loss, P_{SW}, can be computed by

$$P_{SW} = f_{sw}(E_{igbt(on)} + E_{igbt(off)} + E_{d(off)}) \frac{4\sqrt{3}I_{dc}V_{load}}{\pi I_{ref}V_{ref}} \left[1 - \frac{3}{\pi}\sum_{j=1}^{\infty} \sin\left(\frac{2j\pi}{3}\right) \frac{\cos[2j(\theta + \pi/6)]}{j(4j^2 - 1)}\right] \quad , \tag{12}$$

where f_{sw} is the switching frequency; $E_{igbt(on)}$, $E_{igbt(off)}$, and $E_{d(off)}$ are the IGBT turn-on, turn-off, and diode turn-off energy losses at the given voltage, V_{ref}, and current, I_{ref}, respectively; and θ is the phase angle between the motor phase current and voltage. The inverter output voltage, V_{Load}, can be determined by Eq. (10).

Passive Components

Table 5 gives the specifications of the selected passive components. The total capacitance is increased to 390 μF due to the increase in the dc input capacitance from 195 μF in the 55 kW prototype for operation with a 70°C coolant. The selected dc input capacitor has a voltage rating of 500 Vdc, much higher than the requirement of 350 Vdc, because the high ripple current film capacitor is not available at 300 V.

Table 5. Passive Components

Item	Specification	Quantity
Link dc inductor	Metglass amorphous C-core, AMCC-320, copper foil winding, 300 μH	1
Output ac filter capacitor	CDE SFS33S30L288L-F, 330Vac, 30μF, 105˚C	3
Input dc capacitor	UL32Q157K, 500Vdc, 150μF, 105˚C	2

Cold Plate and Thermal Calculation

A high performance aluminum cold plate from Lytron Inc., part number CP30, was selected for the prototype design [3]. The cold plate contains high performance corrugated aluminum fins brazed into the cavity of the cold plate. The fins create turbulence to minimize the fluid boundary layer and reduce thermal resistance. Figure 7 gives performance curves of the cold plate.

At 55 kW output, the estimated losses are 1,675.6 W for the CSI bridge (385.4 W per IGBT, 173.2 W per diode) and 319.2 W for all other components. Thermal resistances for the heat dissipation paths are estimated as follows: IGBT junction-to-case, 0.068°C/W; diode junction-to-case, 0.07°C/W; IGBT module case-to-cold plate, 0.0125°C/W; and cold plate at a flow rate of 2 gpm: 0.005˚C/W. Estimated IGBT and diode junction temperatures with a 105°C coolant are 148.2°C and 134.1°C, respectively, which are well within their safe operating region.

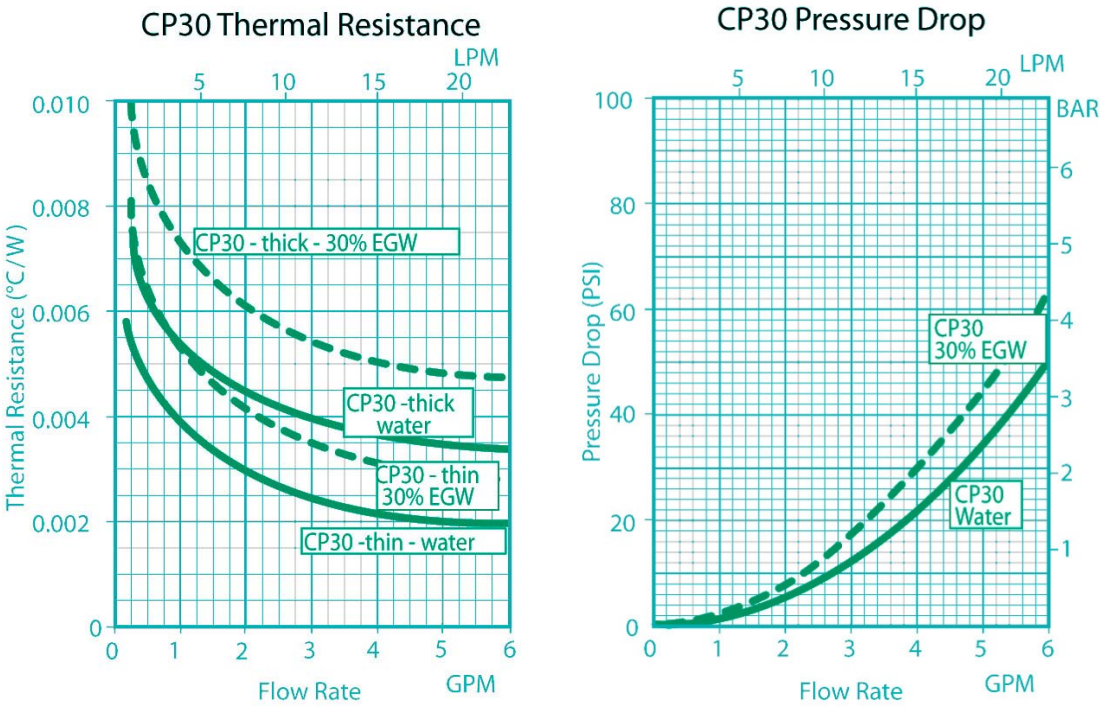

Fig. 7. Performance curves of the Lytron cold plate, CP30 [3].

Control Boards

DSP and gate drive boards for operation in the 105°C coolant environment are designed and fabricated using components rated in the automotive temperate range of -40 to ~125˚C. The TI 32-bit floating-point DSP, TMS320F28335ZJZS, and a Zilinx CPLD for CSI PWM generation are used in the DSP control board. Figure 8 shows a photo of a complete DSP board. Transformer-based signal isolation is used to replace the opto-couplers in the gate drive board. In addition, an overcurrent protection logic circuit is included in the gate drive board to prevent the occurrence of open circuit events in the CSI bridge.

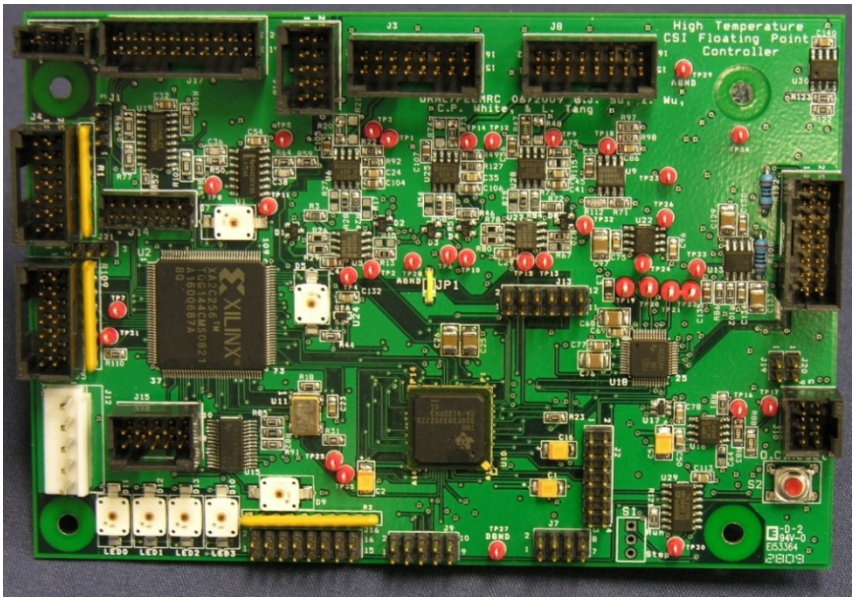

Fig. 8. Photo of the DSP board. Size: 5.7 in. width by 3.9 in. depth.

Final Assembly

Final assembly of all the components was carried out using three-dimensional (3D) layout software from Alibre. Figure 9 shows the 3D layout of the CSI design.

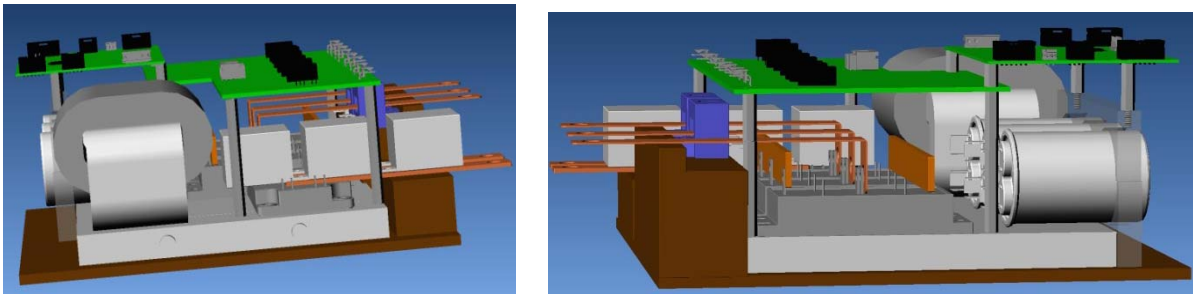

Fig. 9. Three-dimensional layout of the CSI design.

Conclusion

A high performance motor drive using a current-source–based inverter has been examined for HEV applications. The CSI offers many advantages, including (1) high reliability as a result of eliminating dc bus capacitors, (2) ability to endure phase-leg shoot-through, (3) improved motor efficiency and lifetime as a result of sinusoid-shaped voltage and current to the motor, (4) increased constant-power speed range owing to the voltage boosting capability, and (5) reduced requirements for battery storage capacity in plug-in HEVs. A 55 kW CSI was designed, fabricated, and tested in the previous fiscal year and test results confirmed the aforementioned advantages.

This year, a design for a 55 kW CSI for operation with a 105°C coolant was completed using custom IGBT modules comprising Infineon IGBT and Semikron diodes rated with a maximum junction temperature of 175°C and DSP and gate drive boards comprising components rated in the automotive temperate range of -40 to ~125°C. Estimated IGBT and diode junction temperatures are well within their safe operation region. The total capacitance is 390 μF, which is still much lower than the required capacitance in a comparable VSI.

Publications

G. J. Su, L. Tang, and Z. Wu, "Extended Constant-Torque and Constant-Power Speed Range Control of Permanent Magnet Machine Using a Current Source Inverter," in Proceedings of the 5th IEEE Vehicle Power and Propulsion Conference (VPPC'09), pp. 109–115, Sept. 7-11, 2009, Dearborn, MI.

Z. Wu and G. J. Su, "High-Performance Permanent Magnet Machine Drive for Electric Vehicle Applications Using a Current Source Inverter," in Proceedings of the 34th Annual Conference of the IEEE Industrial Electronics Society (IECON'08), pp. 2812–2817, November 10-13, 2008, Orlando, Florida.

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1. M. Takei, Y. Harada, and K. Ueno, "600V-IGBT with reverse blocking capability," in *Proceedings of IEEE ISPSD'2001* (2001), pp. 413–416.
2. E. R. Motto, J. F. Donlon, M. Tabata, H. Takahashi, Y. Yu, and G. Majumdar, "Application characteristics of an experimental RB-IGBT (reverse blocking IGBT) module," in *Proceedings of IEEE IAS 2004 Annual Meeting* (2004), pp. 1504–1544.
3. Lytron data sheet; available at http://www.lytron.com/cold-plates/standard/cold-plates-CP30.aspx?tab=Graphs.

Patents

Gui-Jia Su, "Power Conversion Apparatus and Method," application US12/399,486, March 6, 2009, pending.

4.5 Using the Traction Drive Power Electronics System to Provide Plug-In Capability for Hybrid Electric Vehicles

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Objectives

- Overall project objectives
  - — Reduce cost and volume by 90% compared with stand-alone battery chargers.
  - — Provide rapid charging capability for use at high-power charging stations.
  - — Enable plug-in hybrid electric vehicles (PHEVs) as mobile power generators.
  - — Investigate hardware and software requirements for implementing smart charging and vehicle-to-grid capabilities.
- Objectives for FY 2009 effort
  - — Modify and test the hybrid electric vehicle (HEV) power electronics system prototype consisting of a 55 kW motor inverter and a 30 kW generator inverter to evaluate its mobile power generation capability.
  - — Characterize mobile power generation efficiency performance.

Approach

- Modify the prototype of a 55 kW motor inverter and a 30 kW generator inverter built in FY 2008 for mobile power generation operation.
- Develop digital signal processing (DSP) code to implement mobile power generation for both battery-powered and engine-powered operations.
- Test and evaluate the prototype's power generation capability and performance.

Major Accomplishments

- Designed, fabricated, and successfully tested an HEV power electronics system prototype consisting of a 55 kW motor inverter and a 30 kW generator inverter for operation as a battery charger and mobile power generator.
- Attained a maximum charging efficiency greater than 95% with a 120 V input and greater than 98% with a 240 V input.
- Attained a grid current harmonic distortion factor less than 9% at 120 V input and less than 7% at 240 V input at rated power during charging operation.
- Attained a maximum efficiency of 80% with a 120 V output in engine-powered generation mode.
- Attained a maximum efficiency of 97% at 240 V output and 94% at 120 V output in battery-powered generation mode.

Future Direction

None: Project completed in FY 2009.

Technical Discussion

Background

PHEVs are emerging as a pre-fuel-cell technology that offers greater potential than hybrid vehicles currently on the market to reduce oil consumption and carbon dioxide emissions. In PHEVs, the energy storage capacity of the battery needs to be increased significantly to enable a driving distance of at least 40 miles in an all-electric mode, the distance needed to substantially reduce oil consumption for daily commuting. A charger is also required to replenish the battery after it is depleted, typically done overnight to leverage energy costs by taking advantage of off-peak electricity rates.

Stand-alone battery chargers, however, impose an extra cost on already expensive HEVs and have other limitations. A typical stand-alone battery charger for PHEVs consists of a diode rectifier and a unidirectional dc-dc converter (i.e., it can only charge the battery) that uses power semiconductor switches, diodes, inductors, and capacitors, as shown in Fig. 1. A charger with a low charging capability of 1 to ~3 kW can cost almost 30% as much as the electric traction system for a midsize PHEV-20 car ($690) [1]. The limited charging capability results in a long charging time (about 6 to 8 hours), which could negatively impact the acceptance of PHEVs.

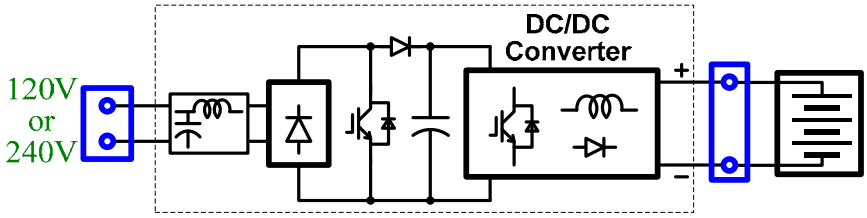


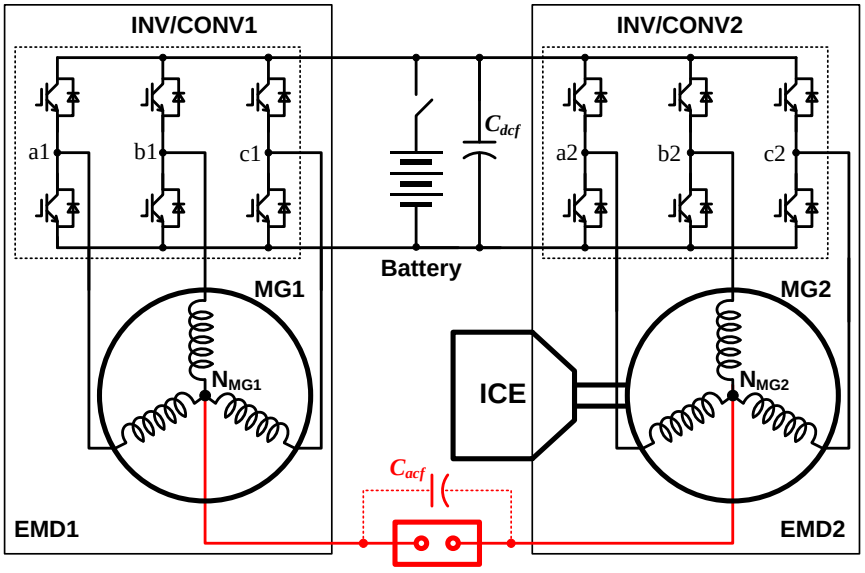
Fig. 1. A schematic showing major components in a stand-alone battery charger.

To minimize the cost of the charger, this project is investigating the use of the power electronics and motors already aboard the vehicle to fulfill the charging requirements. It is expected that, compared with a stand-alone battery charger, the proposed approach will impose virtually no additional cost or will significantly reduce the cost, depending on the configuration of the onboard traction drive system. The proposed approach is to integrate the battery charging function into the traction drive system and eliminate or minimize the number of additional components. Because traction power inverters have a greater current-carrying capability, the integrated charger can reduce the charging time significantly. Another benefit of this approach is that it enables PHEVs to function as mobile generators at little or no additional cost. Another objective is to investigate hardware and software requirements for implementing smart charging and vehicle-to-grid capabilities.

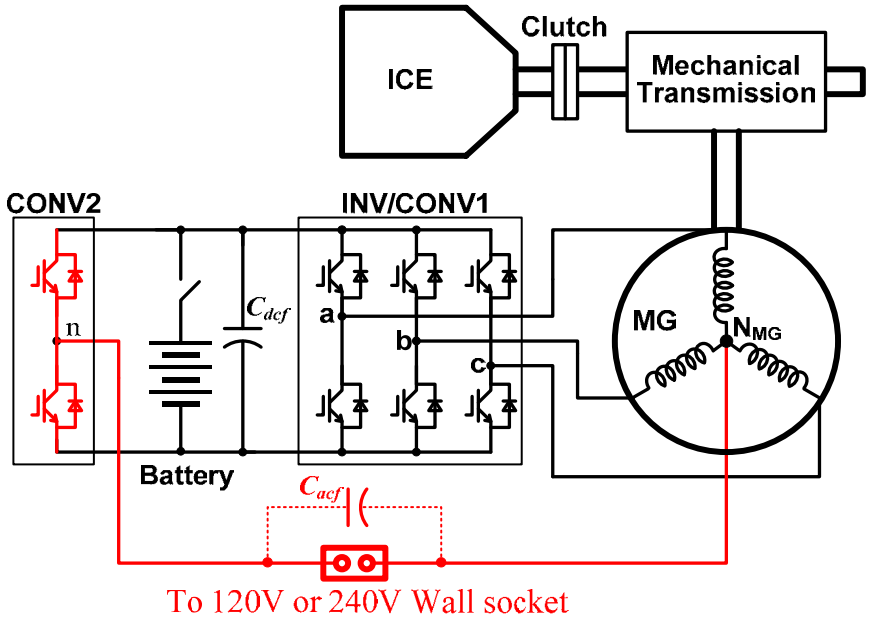
Description of the Reduced-Part dc-dc Converter

Figure 2 shows topologies for using the onboard electrical drive system to provide plug-in charging and mobile generation capabilities for HEVs. The onboard electrical drive system may consist of one or more electrical motor drive units, all connected to a common dc bus. Each motor drive unit typically uses a three-phase inverter/converter (INV/CONV) and a three-phase motor/generator (MG) with a Y-connection to the motor and the neutral point (N_{MG}) brought out. At least one drive unit is coupled to the engine shaft through a mechanical transmission device. The basic idea is to use the MGs as inductors by connecting their neutral points to an external charging source to charge the battery or to external loads to supply power to them. The external charging source can be a dc or single-phase or multiphase ac power supply, depending on the number of onboard drive units. Figure 2(a) illustrates an arrangement for a

series HEV in which two INV/CONVs and two MGs are used. For such vehicles, no additional components other than some wiring and connectors are required. An ac filter capacitor may also be needed to meet grid interface power quality requirements. For parallel HEVs, in which only one INV/CONV and MG are used, two switches must be added, as shown in Fig. 2(b).



(a)



(b)

Fig. 2. Topologies for using the onboard electrical drive system to provide plug-in charging and mobile generation capabilities for HEVs: (a) for HEVs using two inverters and motors; (b) for HEVs using a single inverter and motor. (Red denotes added components.)

All the switch legs in each INV/CONV collectively function as a single switch leg and the MG as an inductor. Together, the drive units form a single-phase or multiphase converter, operating in the charging mode, to regulate the dc bus voltage. In the generation mode, the drive units form a single-phase or multiphase inverter to supply external loads. In this mode, the MG of the drive unit coupled to the engine shaft is driven by the engine to generate power to supply the dc bus and ultimately the external loads. Alternatively, power can be drawn from the battery for short operating intervals.

Figure 3 shows a schematic of the circuit in Fig. 2(a) during operation in charging mode. All three switch legs (a1, b1, c1 and a2, b2, c2) in INV/CONV1 and INV/CONV2 collectively function as a single switch leg, and the MGs function as two impedance networks. The MG stators comprise zero sequence impedance networks, ZSIN1 and ZSIN2. Each ZSIN consists of three branches and each branch comprises the stator winding phase resistance (R_{ms1} or R_{ms2}) and the stator phase leakage inductance (l_{m0s1} or l_{m0s2}). Together, the two drive units form a single-phase converter to regulate the battery voltage, V_{bat}, or the charging current, I_{bat}. Normally, the single-phase converter is controlled so as to maintain a unity power factor by keeping the source current, i_s, in phase with the source voltage, v_s. An additional benefit of operating the three-phase converters as single leg converters is the reduction in harmonic current components resulting from interleaving the gating signals of the three legs.

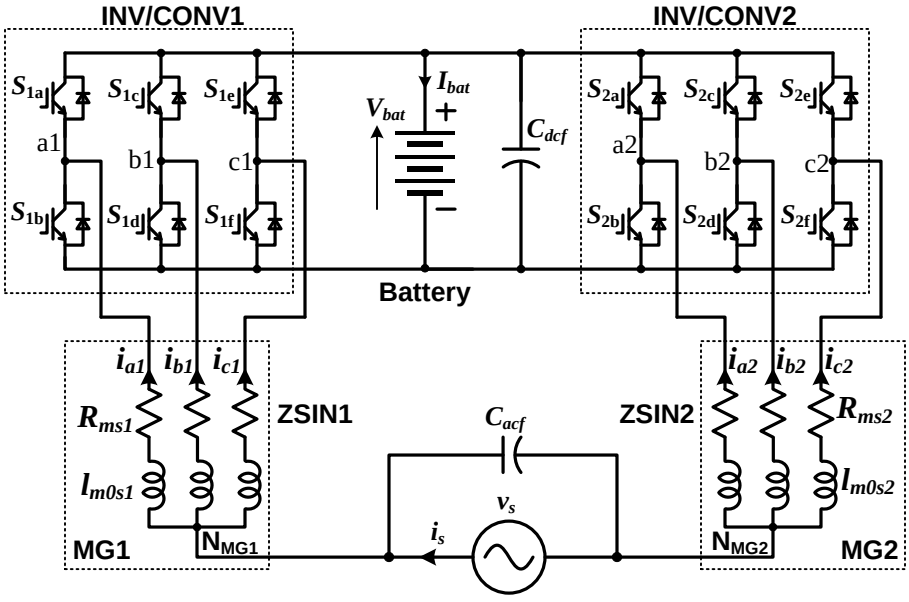


Fig. 3. Schematic of a circuit for battery charging mode.

Figure 4 shows a schematic of the circuit in Fig. 2(a) during operation in mobile generation mode. There are two available power sources, the battery and the engine. Figure 4(a) illustrates the case in which the battery is the source. In this case, all three switch legs in each of the two INV/CONVs collectively function as a single switch leg and the MGs as two impedance networks. Together the two drive units form a single-phase inverter to regulate the load voltage, v_{Load}.

Figure 4(b) illustrates the case in which power is generated by the MG2 driven by the engine. In this case, the three switch legs in INV/CONV1 collectively function as the first single switch leg of a single-phase inverter and the MG1 functions as an impedance network. INV/CONV2 has dual functions. It first operates as a three-phase converter to regulate the dc bus voltage, V_{dc}, by drawing power from the generator; at the same time, its three phase legs collectively form the second switch leg of the single-phase inverter to regulate the load voltage, v_{Load}.

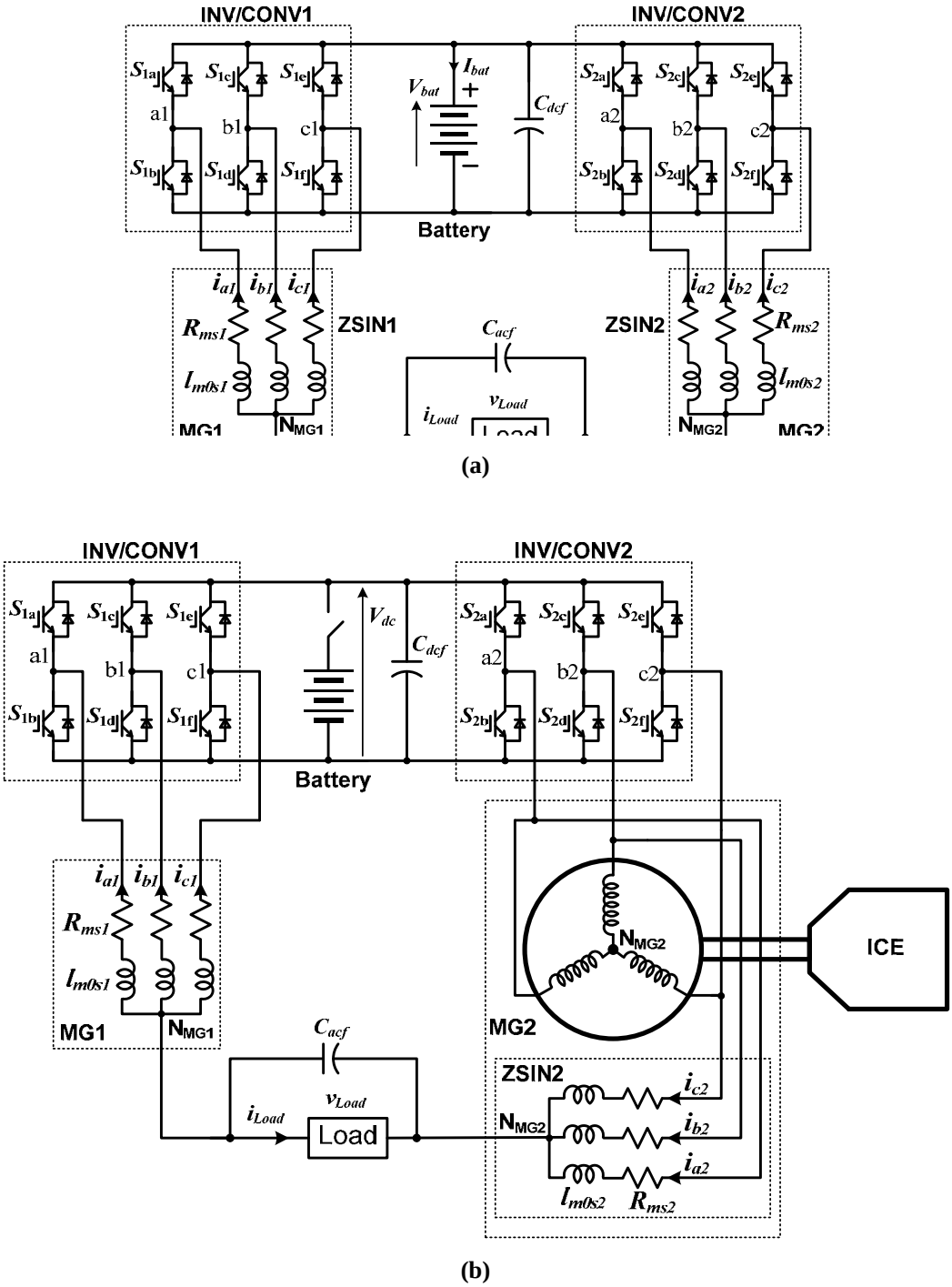


Fig. 4. Schematic of circuits for mobile generator mode: (a) battery-powered generation mode (i.e., using the battery as the power source); (b) engine-powered generation mode (i.e., using the motor MG2 driven by the engine as the power source).

Prototype Modification and Testing

An HEV drive inverter system prototype consisting of a 55 kW motor inverter and a 30 kW generator inverter with a plug-in charging capability of 20 kW was designed, built, and tested in charging operation in FY 2008. Figure 5 is a photo of the prototype. The 55 kW motor inverter was implemented with a

six-pack insulated gate bipolar transistor (IGBT) module rated at 600 V and 600 A (part number PM600CLA060 from Powerex), and the 30 kW generator inverter was implemented with a six-pack IGBT module rated at 600 V and 300 A (part number PM300CLA060 from the same vendor). The bus capacitor bank was constructed using four film capacitors (Electronic Concepts, Inc., part number UP33BC0375), rated at 600 Vdc and 375 μF. These components are mounted on a 12 × 7 in. cold plate. The prototype was modified by adding a voltage sensor and signal conditioning circuitry and tested operating in the mobile generator mode.

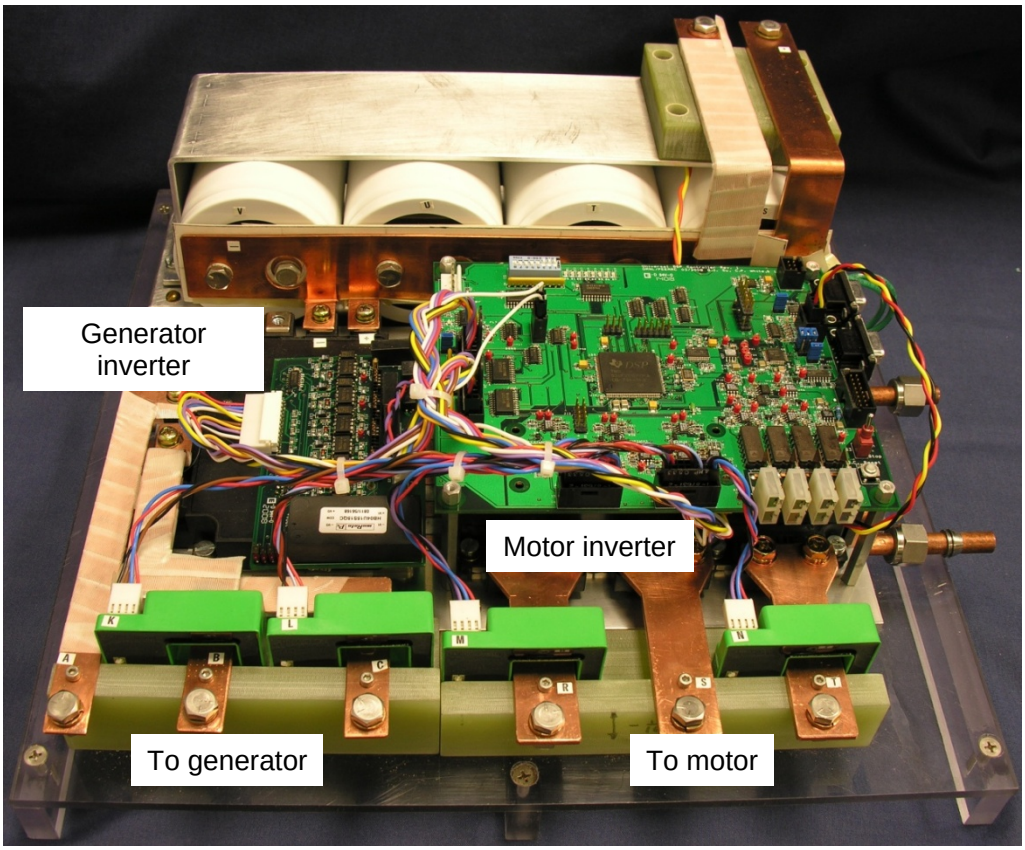
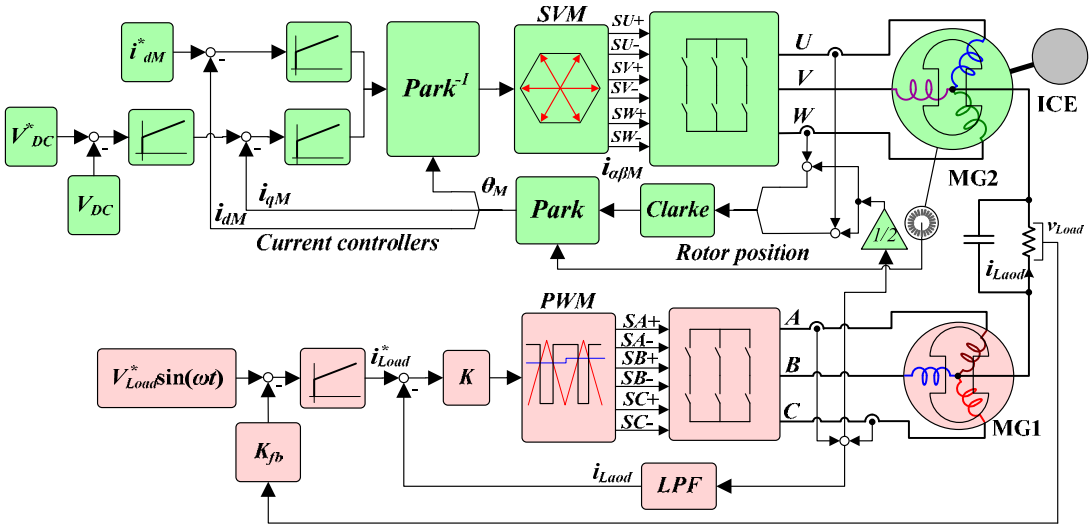


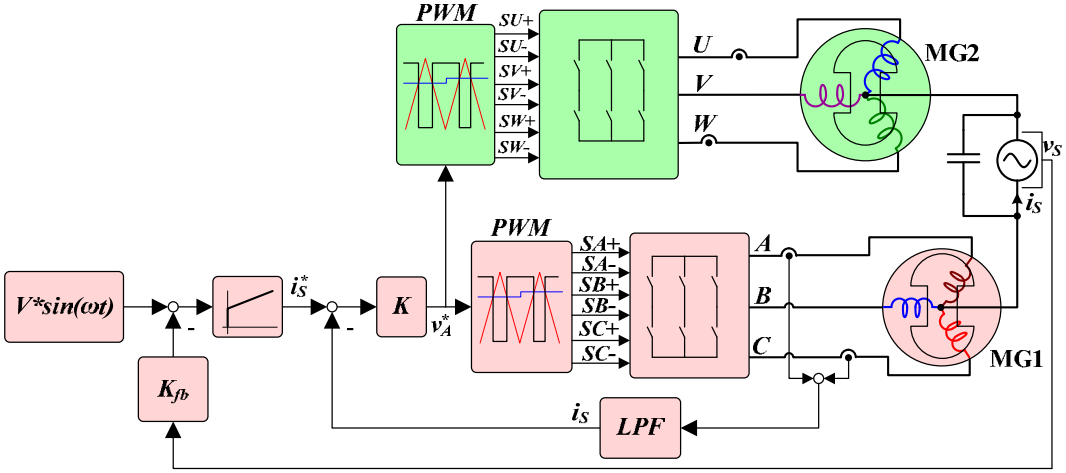
Fig. 5. A photo of a prototype consisting of a 55 kW motor inverter and a 30 kW generator inverter with plug-in charging and mobile power generation capabilities. The heat sink footprint is 12 in. width by 7 in. depth.

DSP code was then developed to implement the mobile power generation control algorithms for both battery-powered and engine-powered operations. Figure 6 shows control block diagrams for mobile power generation. In 6(a) the system operates in the engine-powered generation mode using the motor MG2 driven by the engine as the power source. Using the field orientation technique and space vector pulse-width modulation (PWM) method, the *d* and *q* axis currents, i_{dM} and i_{qM}, of MG2 are controlled with the motor inverter to maintain the inverter dc bus voltage at the commanded level, V^*_{DC}. The generator inverter is used to control the output voltage with the help of an inner current loop to improve the dynamic response. Both synchronized and interleaved PWM schemes were used for the generator inverter to investigate the impact on the efficiency by the switching schemes. Due to the PWM generation hardware limitation of the digital signal processor, a software implementation of the interleaved PWM based on a single carrier was developed. In 6(b) the system operates in battery-powered generation mode using the high voltage battery as the power source. Both inverters are used to control the output voltage with the help of an inner current loop to improve the dynamic response. The following combinations of

PWM schemes were used for the inverters to assess the impact on the efficiency by the switching schemes: (1) synchronized PWM for both inverters, (2) interleaved PWM for both inverters, and (3) unipolar PWM for motor (MG2) inverter and interleaved PWM for generator inverter (MG1).



(a)



(b)

Fig. 6. Control block diagrams for mobile power generation: (a) engine-powered generator mode; (b) battery-powered generator mode.

A 10.9 kW induction motor and a permanent magnet (PM) motor rated at 8.2 kW were used in the testing. Table 1 gives their zero sequence resistances. The resistance values of Toyota Camry motors are also given for comparison. Notice the combined resistance of the two test motors is more than 5 times larger than that of the Camry motor owing to the large resistance of the induction motor. This had a significant impact on efficiency.

Table 1. Motor Zero Sequence Resistance

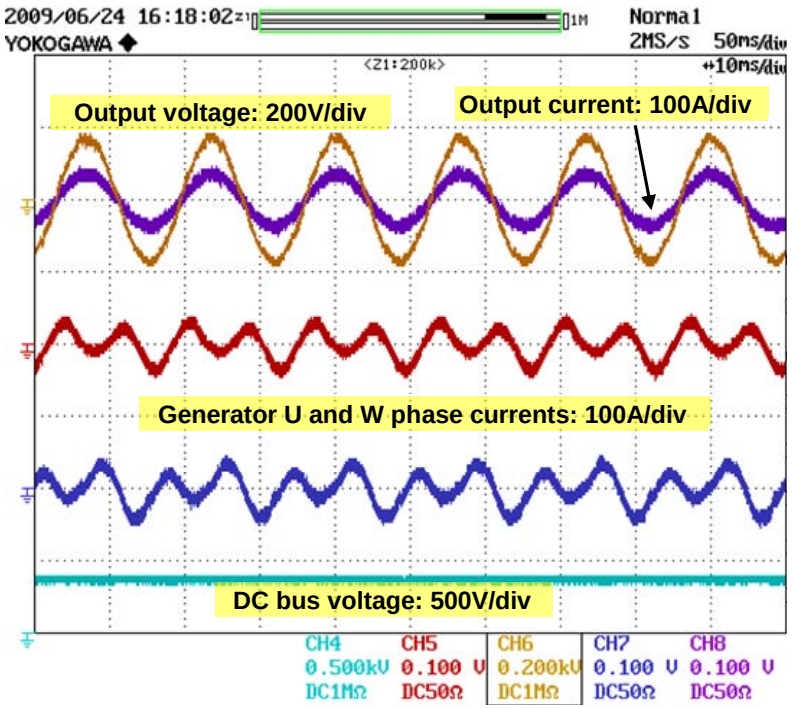
Test motor 1	165.74 mΩ	Camry generator	21.58 mΩ
Test motor 2	23.8 mΩ	Camry motor	10.75 mΩ
Combined	189.54 mΩ	Combined	32.32 mΩ

The prototype was tested in engine-power generation mode with 120 V output and battery-powered generation mode at 120 V and 240 V output for varying resistive load power. Figure 7 illustrates test results showing operating waveforms in the engine-powered generator mode. The smooth sinusoidal output voltage and current waveforms and flat dc bus voltage indicate excellent performance of the controller. Because one-third of the 60 Hz load current is superimposed as a zero-sequence component on the original generator current, the generator phase currents are no longer sinusoidal.

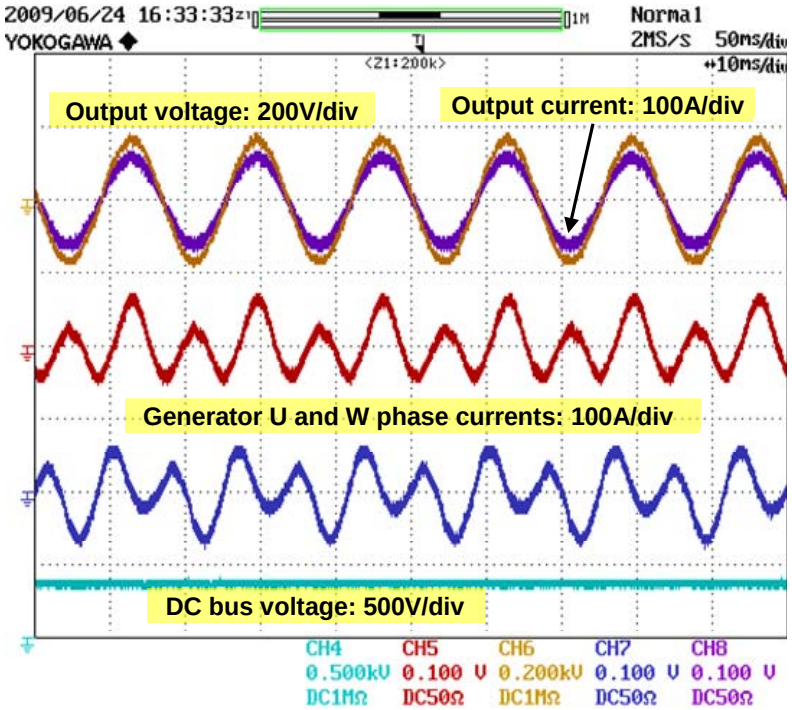
Figure 8 plots measured efficiency against output power. Due to the relatively low efficiency (<85%) of the small PM generator, the system efficiency does not exceed 80%. However, it is estimated that a maximum efficiency greater than 92% could be achieved with a production PM generator efficiency of 95% because the inverter efficiency can reach 97%, as will be shown later. In addition, a 1% improvement is attained with the interleaved switching over the synchronized switching.

Figure 9 illustrates test results showing operating waveforms in the battery-powered generator mode, where the output voltage is set at 120 V in 9(a) and 240 V in 9(b). Again, the smooth sinusoidal output voltage and current waveforms and flat dc bus voltage in both output voltages indicate excellent performance of the control method. In this operation mode, both motors are used as inductors and one-third of the 60 Hz load current is flowing in each phase winding as a zero-sequence component, as indicated by the identical two-motor phase currents in the test results.

Figure 10 plots measured efficiency against output power. At the output voltage of 240 Vac as shown in 10(a), significant efficiency improvement is achieved with the interleaved and unipolar switching over the synchronized switching PWM scheme due to the significant reduction of switching loss through the interleaved and uniploar switching method. The maximum efficiency reaches 97% at the output power of 6.2 kW. Figure 10(b) shows the measured efficiency at the output voltage of 120 Vac with the interleaving and unipolar switching scheme. The maximum efficiency in this case is 94% at the output power of 2.1 kW. It is observed in both cases that the efficiency drops as the output power increases due to substantial copper loss at high load current in the high stator resistance of the test motors. This efficiency decrease is faster in the case of 120 V output because at a given output power the current is larger than in the 240 V output, which in turn generates even larger copper loss in the form of I^2R. It is therefore expected that much better efficiency could be attained with production PM motors whose resistance is much lower than those of the test motors.



(a)



(b)

Fig. 7. Test results showing operation in engine-powered generator mode for (a) output power = 3.0 kW at 120V and (b) output power = 5.0 kW at 120 V.

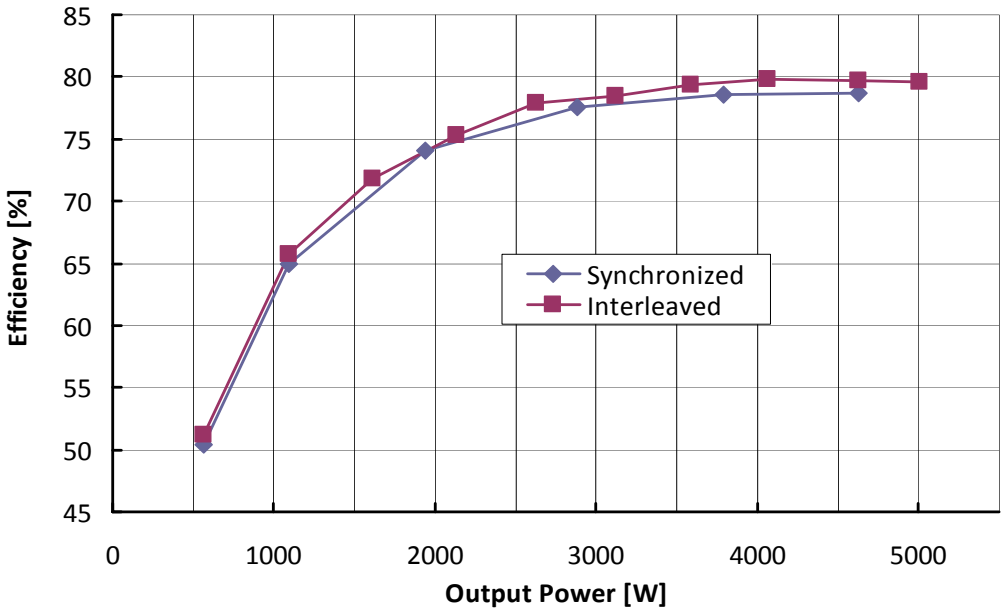


Fig. 8. Measured efficiency in engine-powered generator mode.

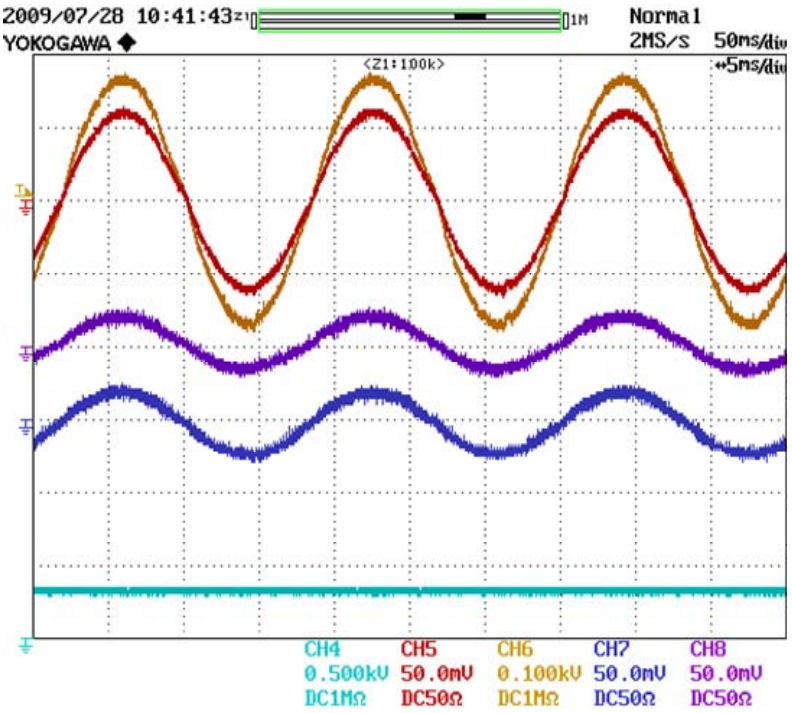


Fig. 9(a). Test results showing operation in the battery-powered generator mode for output power = 5.1 kW at 120 V.

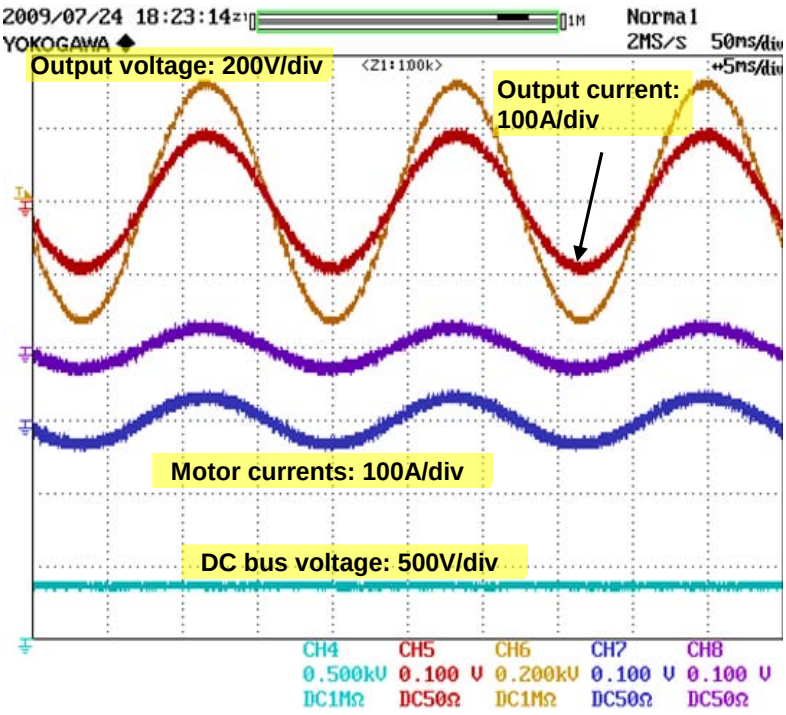
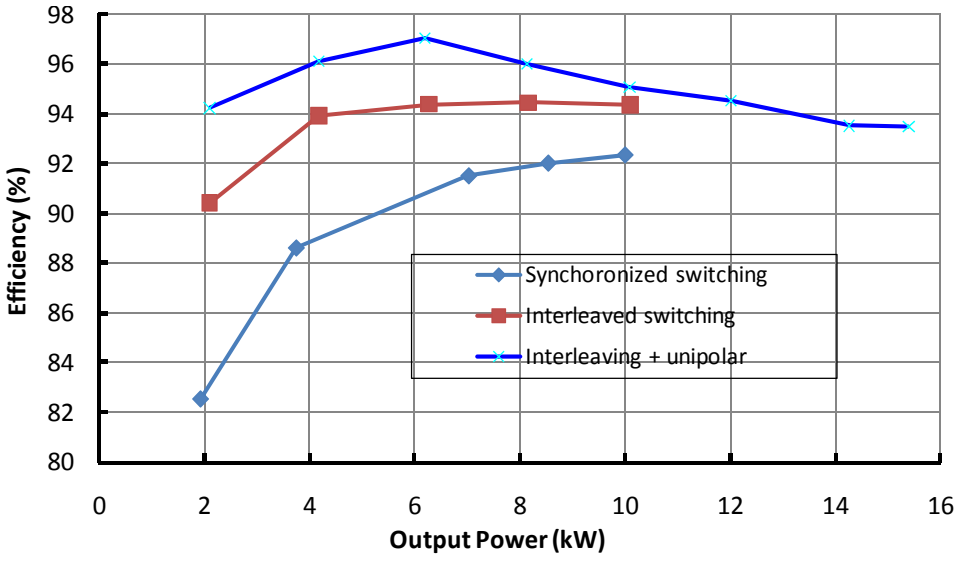


Fig. 9(b). Test results showing operation in the battery-powered generator mode for output power = 14.7kW at 240 V.



(a)

Fig. 10(a). Measured efficiency in the battery-powered generator mode at output voltage of 240 Vac.

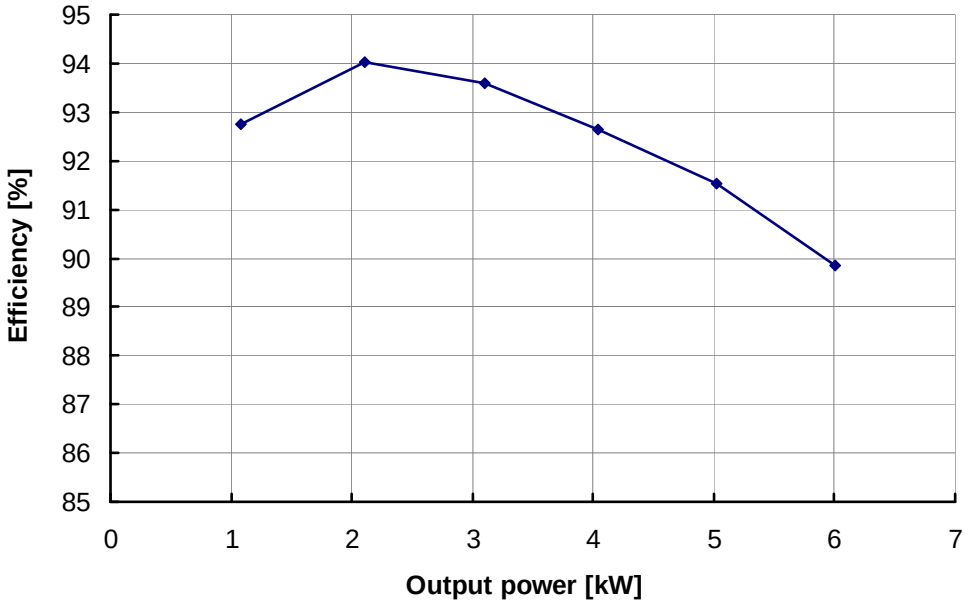


Fig. 10(b). Measured efficiency in the battery-powered generator mode at output voltage of 120 Vac.

Conclusion

This project explored ways of using the onboard electrical drive system in different HEV configurations to provide plug-in charging and mobile power generation capabilities. The proposed charging schemes offer many benefits, including (1) significantly reducing the cost and volume of battery chargers in PHEVs, (2) providing rapid charging capability, and (3) enabling the use of PHEVs as mobile generators. Detailed circuit simulations were first carried out, and the simulation results proved the concepts and validated the rapid charging and mobile generation capabilities.

An HEV power electronics system prototype made up of a 55 kW motor inverter and a 30 kW generator inverter was designed, fabricated, and successfully tested in FY 2008 for operation as a battery charger. Test results confirmed high efficiency, high power factor, and low harmonic distortion in the charging mode. The prototype was modified and successfully tested during FY 2009 as a mobile power generator. Test results show high efficiency with the proposed PWM switching scheme.

- Attained a maximum efficiency of 97% at 240 V output and 94% at 120 V output in the battery-powered generation mode.
- Attained a maximum efficiency of 80% with a 120 V output in engine-powered generation mode.

Publications

L. Tang and G. J. Su, "A Low-Cost, Digitally-Controlled Charger for Plug-In Hybrid Electric Vehicles," IEEE Energy Conversion Congress and Exposition (ECCE), September 20—24, 2009, San Jose, California, pp. 3923–3929.

References

1. *Advanced Batteries for Electric-Drive Vehicles*, Report 1009299, Electric Power Research Institute, May 2004.
2. Electric Auto Association Plug-in Hybrid Electric Vehicle, "*Battery chargers, PHEV applications,*" http://www.eaa-phev.org/wiki/Battery_Chargers.

Patents

Gui-Jia Su, "Electric Vehicle System for Charging and Supplying Electrical Power," Patent Application US2008/0094013A1, pending.

4.6 A Segmented Drive System with a Small DC Bus Capacitor

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Objectives

- Overall project objectives
  - — Significantly reduce the amount of inverter dc bus capacitance by reducing the ripple current by more than 60%.
- Objectives for FY 2009 effort
  - — Perform a simulation study to prove the concept.
  - — Assess the effect of various pulse-width modulation (PWM) schemes on the reduction of ripple current to determine the optimal PWM method.
  - — Conduct a conceptual design for a 55 kW prototype.

Approach

- Use a segmented drive system topology that does not need additional switches or passive components but will enable the use of optimized PWM schemes to significantly reduce the dc link ripple current and thus the capacitance.
- Perform studies of various carrier-based and space-vector PWM techniques using PSIM simulation software to assess their impact on the capacitor ripple current.
- Build and test a 55 kW prototype (in FY 2010) to experimentally validate the simulation study.

Major Accomplishments

- Validated the segmented drive concept by a simulation study.
- Achieved more than 65% reduction in capacitor ripple current as compared to the standard inverter configuration.
- Achieved 80% reduction in battery ripple current.
- Achieved 70% reduction in dc bus ripple voltage.
- Achieved 50% reduction in motor ripple current.
- Completed a conceptual design for a 55 kW prototype.

Future Direction

- Finalize the design; build and test a 55 kW prototype.
- Apply the segmented drive concept in an integrated traction drive system.

Technical Discussion

Background

The standard voltage source inverter- (VSI-) based traction drive is widely used in present hybrid electric vehicles (HEVs). Figure 1 shows a block diagram of the VSI-based drive system. The VSI is mainly composed of six power semiconductor switches—typically insulated gate bipolar transistors (IGBTs)—and a dc bus filter capacitor switches the battery voltage according to a certain PWM scheme to regulate the motor current and voltage. In doing the switching operations, it generates large ripple currents in the dc link, thus necessitating the use of the dc bus filter capacitor to absorb the ripple currents so that a relatively constant current flows into the battery. Figure 2 shows simulated motor current, i_a, i_b, i_c; capacitor ripple current, i_{Cbus} and $i_{Cbus(rms)}$; inverter dc link current, i_{inv}; and battery current, i_{bat}, in a typical 55 kW HEV inverter. The capacitor ripple current reaches as much as 200 Arms, and thus a bulky and costly dc bus capacitor of about 2,000 µF is required to prevent this large ripple current from flowing into the battery.

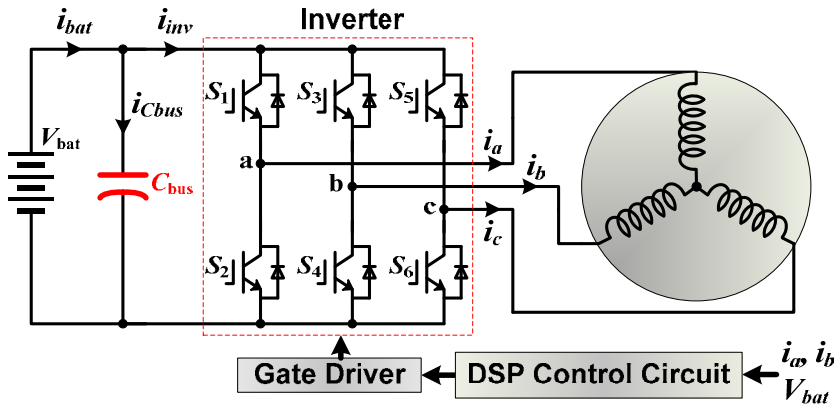

Fig. 1. Standard VSI-based drive system.

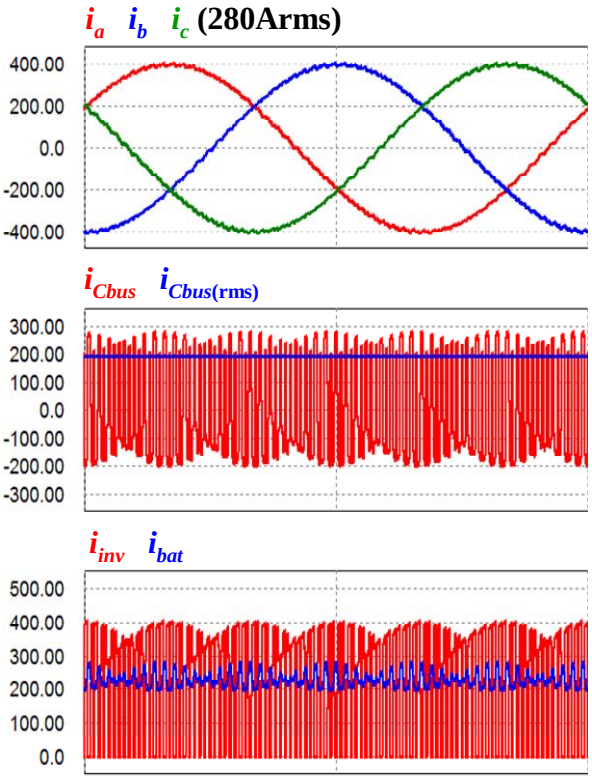

Fig. 2. Simulated waveforms in the standard VSI-based drive system.

The dc bus capacitor, therefore, presents significant barriers to meeting the targets of cost, volume, and weight for inverters. Currently, it contributes

- cost and weight of up to 23% of an inverter and
- volume comprising up to 30% of an inverter.

The large ripple currents become even more problematic for film capacitors (the capacitor technology of choice for electric vehicles/ hybrid electric vehicles (EVs/HEVs) in high temperature environments as their ripple current handling capability decreases rapidly with rising temperatures, as indicated in Fig. 3. For example, as the ambient temperature rises from 85 to 105°C, the weight, volume, and cost of capacitors could increase by a factor of 5 due to a decrease of ripple current capability from 50 A to 11 A.

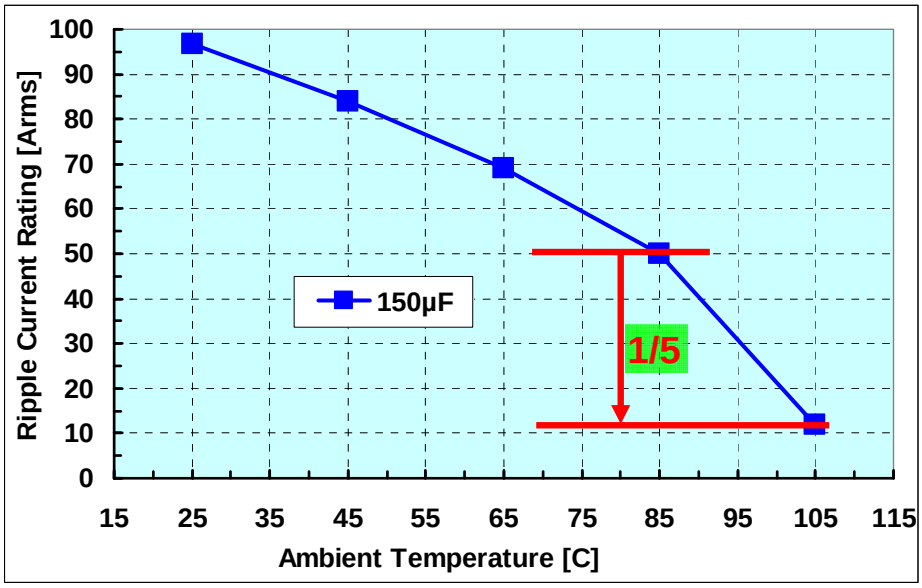

Fig. 3. Ripple current capability vs ambient temperature (Electronic Concepts UL31 Series) [1].

Thus there is an urgent need to reduce the ripple currents all together or to divert them from the bus capacitor. The following factors, however, make this a difficult task: (1) increasing the switching frequency, while reducing the motor current ripples, has little impact on the bus capacitor ripple currents because the capacitor ripple currents depend on the motor peak current, and (2) the major components of the capacitor ripple currents have frequencies of multiples of the switching frequency (nf_{sw}) or their side bands ($nf_{sw} \pm f_m$, $nf_{sw} \pm 2f_m$, …), as given by the equation below and illustrated in Fig. 4. The high-frequency nature makes it impractical to actively filter out the ripple components because doing so requires the use of very high switching frequencies in an active filter.

$$i_{inv} = I_{dc} + \sum_{k=0}^{\infty}\sum_{n=1}^{\infty} I_{n,k} \sin[2\pi(nf_{sw} \pm kf_m)t + \alpha_{n,k}],$$

where f_{sw}: switching frequency and
f_m: motor fundamental frequency.

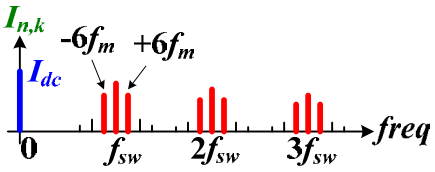

Fig. 4. Ripple components in the dc link current in the standard VSI-based drive system.

Description of the Proposed Segmented Drive and Simulation Results

A segmented drive system topology was examined in this project. Because the technology is under patent review, details of the topology will not be shown in this report. However, the segmented topology does not need additional switches or passive components but enables the use of optimized PWM schemes to significantly reduce the dc link ripple current generated by switching of the inverter output currents.

The uniqueness of this technology is that, while being able to significantly reduce the capacitor ripple current, it *does not*

- need additional silicon or passive (L or C) components,
- need additional sensors, or
- add control complexity.

The following positive impacts are expected.

- Substantially reduce the bus capacitance (at least 60%) and thus inverter volume and cost.
- Reduce battery losses and improve battery operating conditions by eliminating battery ripple current.
- Significantly reduce the motor torque ripples (up to 50%), and reduce switching losses by 50%.

A simulation study using PSIM was carried out to prove the concept and to assess the effect of various PWM schemes on the reduction of ripple current to determine the optimal PWM method. The following five cases were examined: (a) standard VSI: triangle-sine comparison, (b) standard VSI: space-vector PWM, (c) segmented drive: PWM 1, (d) segmented drive: PWM 2, and (e) segmented drive: optimized PWM.

Figure 5 shows simulated motor currents, i_a, i_b, i_c; capacitor ripple current, i_{Cbus} and $i_{Cbus(rms)}$; inverter dc link current, i_{inv}; and battery current, i_{bat}, at the maximum motor current of 280 Arms for the five cases. The calculated capacitor ripple currents are (a) 222 Arms, (b) 190 Arms, (c) 157 Arms, (d) 95 Arms, and (e) 75 Arms. Compared with the standard VSI with the frequently used triangle-sine-comparison PWM method (case a), the proposed segmented drive with the optimal PWM scheme (case e) results in a 66% reduction in the capacitor ripple current and a significant reduction of battery ripple current—from greater than 100 A peak-to-peak (p-p) to less than 15 A.

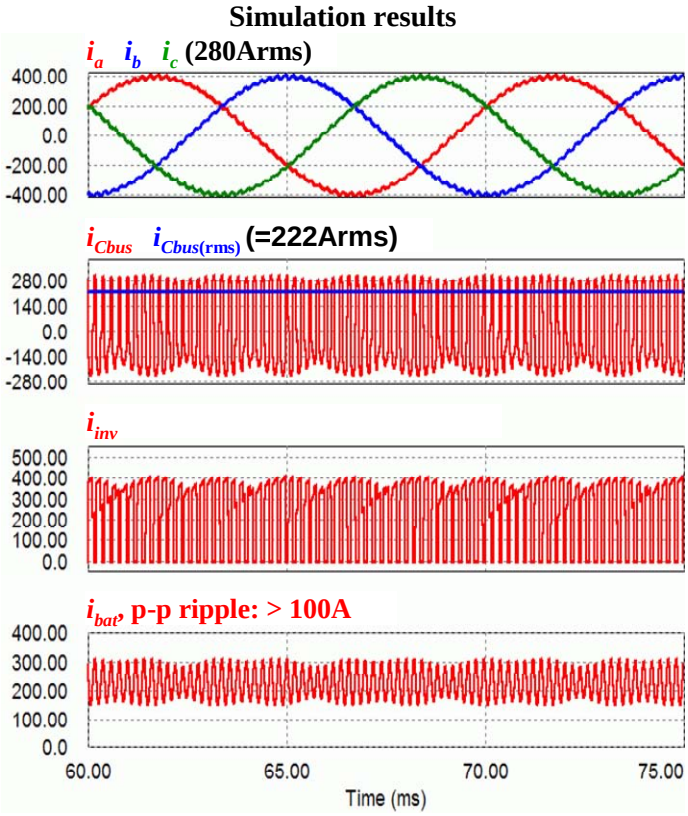

Fig. 5(a). Standard VSI: triangle-sine comparison.

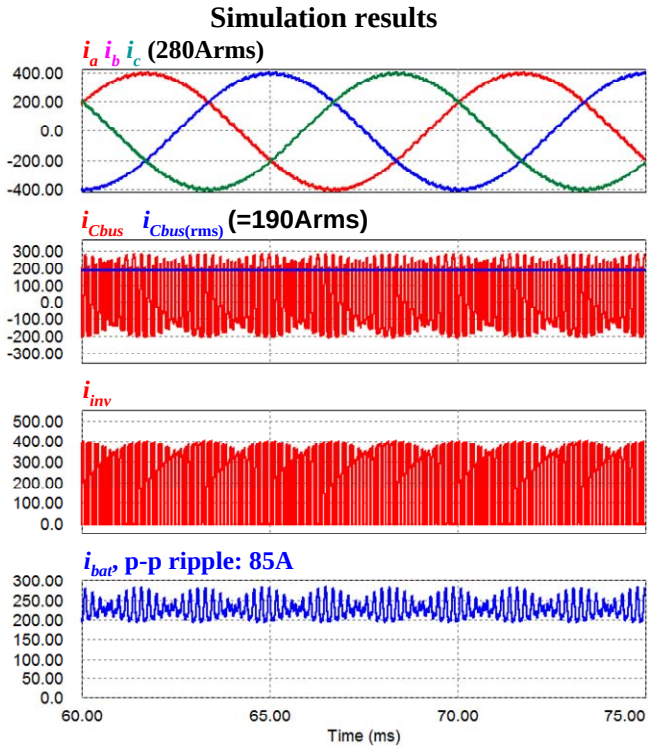

Fig. 5(b). Standard VSI: space-vector PWM.

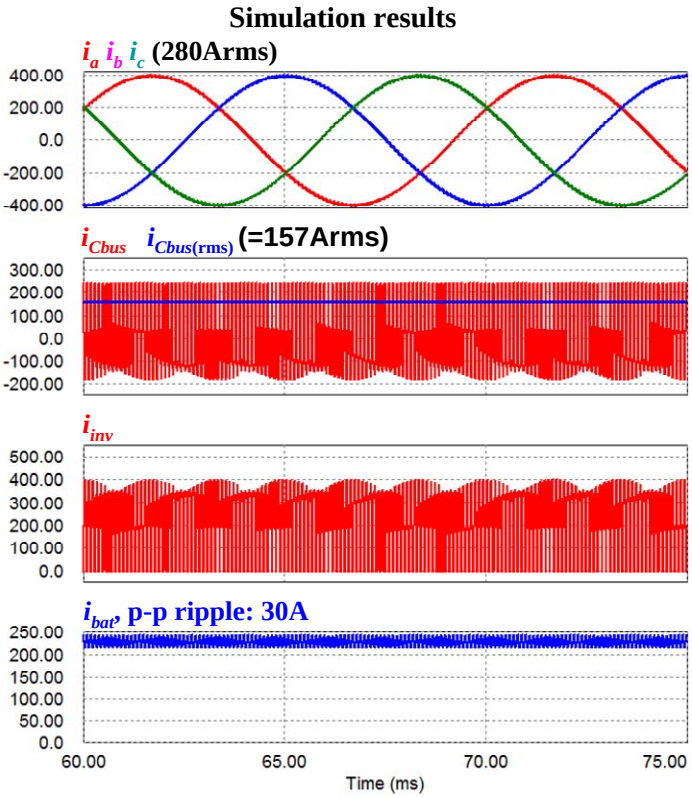

Fig. 5(c). Segmented drive: PWM 1.

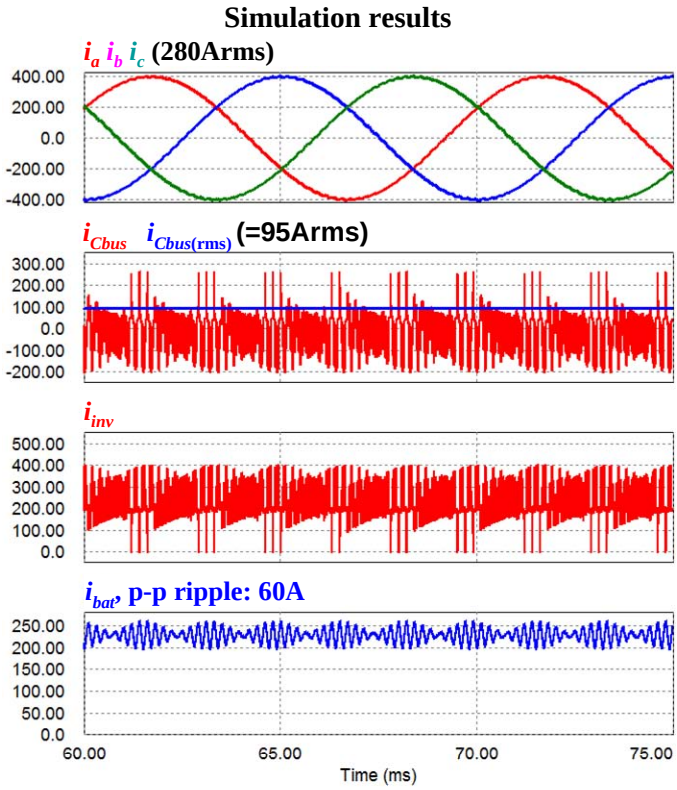

Fig. 5(d). Segmented drive: PWM 2.

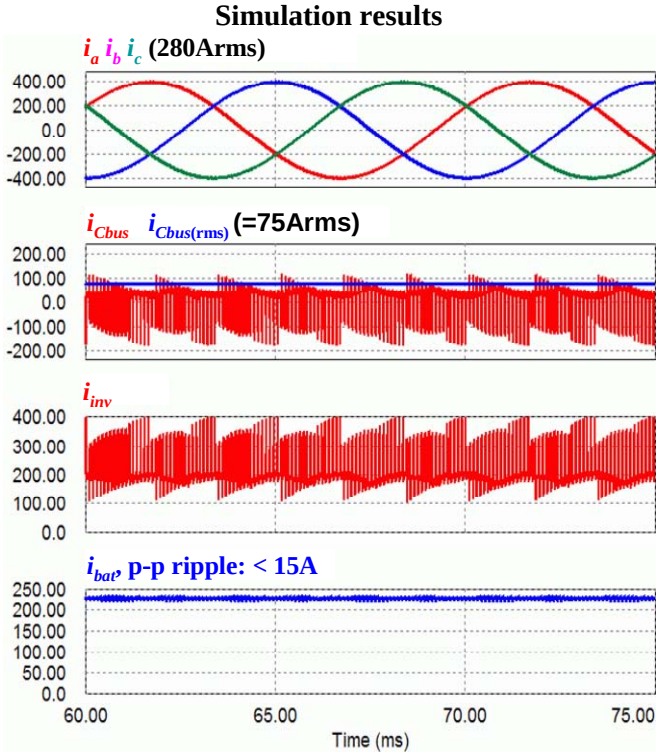

Fig. 5(e). Segmented drive: Optimized PWM.

Figure 6 plots the capacitor ripple currents at various levels of motor current for the five cases. As expected, the capacitor ripple current is proportional to the motor current and the proposed segmented drive with the optimal PWM scheme always generates the lowest capacitor ripple current—less than 35% of that in case (a).

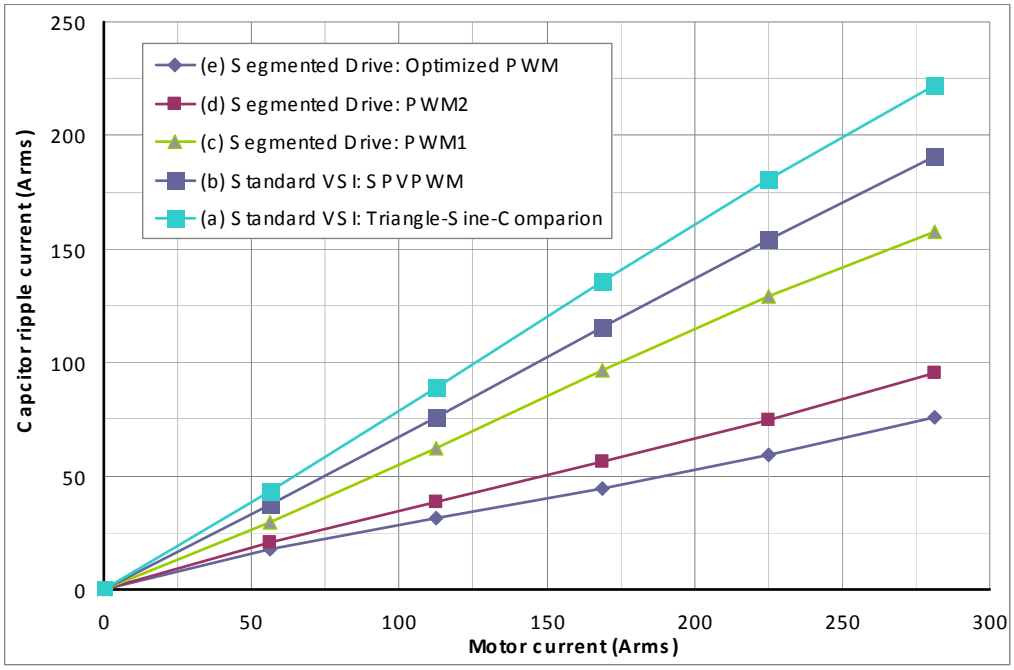

Fig. 6. Comparison of capacitor ripple current vs motor current.

Conceptual Design for a 55 kW Inverter Prototype

Based on the simulation results, a conceptual design for a 55 kW inverter prototype has been completed and the following major components selected.

- IGBT: Powerex Intellimod L-Series IGBT module, PM150CLA060
- Capacitor; Electronic Concepts, Inc. (required ripple current rating, 75 Arms), UL35Q157K, 150 µF/78 Arms

Conclusion

The proposed technology involves modifying the standard drive topology and optimizing the PWM scheme to significantly reduce the ripple current flowing into the capacitor

- *without* additional silicon or passive (L or C) components,
- *without* additional sensors, and
- *without* control complexity.

Simulation results have shown that the proposed segmented drive can

- substantially reduce the bus capacitance (at least 60%) and thus the inverter volume and cost,
- reduce battery losses and improve battery operating conditions by reducing the battery ripple current,
- significantly reduce the motor torque ripples (up to 50%) and reduce switching losses by 50%,
- increase inverter reliability, and
- enable high temperature inverter operation.

Reference

16. Electronic Concept Datasheet, http://www.eci-capacitors.com/product_details.asp?productid=29.

4.7 High Dielectric Constant Capacitors for Power Electronic Systems

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Objectives

- Develop ceramic dielectric films that have potential to reduce size, weight, and cost, concomitant with increased capacitance density and high temperature operation, for capacitors in HEV, PHEV, and FCV power electronic systems.
- Current DC bus capacitors occupy a large fraction of the volume and weight of the inverter module, cannot tolerate temperatures >120°C, and suffer from poor packaging, inadequate reliability, and deleterious failure modes.
- Traditional capacitor architectures with conventional dielectrics cannot adequately meet all of the performance goals for capacitance density, weight, volume, and cost.
- Meeting these goals requires a dielectric with high permittivity and breakdown field that tolerates operating at high temperature, is packaged in architecture with high volumetric efficiency, and exhibits benign failure features.

Approach

- Develop high performance, low-cost ferroelectric (PLZT) dielectric films on base-metal foil ("film-on-foil") that are either stacked on or embedded directly into the printed wire board.
- Use of base-metals and solution-based deposition techniques reduce the cost.
- Ferroelectrics possess high dielectric constants, breakdown fields, and insulation resistance. With their ability to withstand high temperatures, they can tolerate high ripple currents at under-the-hood conditions.
- Stacked and/or embedded capacitors significantly reduce component footprint, improve device performance, provide greater design flexibility, achieve high degree of volumetric efficiency with less weight, and offer an economic advantage.
- R&D efforts focus on examining the issues that underpin the performance of film-on-foil capacitors, establishing fabrication protocols that are commercially robust and economically viable.

Major Accomplishments

- Demonstrated film-on-foil PLZT dielectrics with dielectric constant (relative permittivity), k >1300, breakdown field >6 MV/cm, and leakage current $<10^{-8}$ A/cm^2 at room temperature.
- Measured k ≈210 at 300 V and ≈115 at 600 V applied bias on a ≈3.0 μm-thick PLZT film at room temperature.
- Fabricated a 12-mm diameter film-on-foil dielectric (≈1.15 μm-thick PLZT) with capacitance of 0.9 μF at zero bias and 0.3 μF at 30 V.
- Fabricated and characterized PLZT dielectrics on nickel metal foils with self-clearing electrodes. The key to large-area yield is to electrically isolate the defect spots that compromise the integrity of the dielectric layer.

- PLZT film-on-foil capacitors were thermally cycled ≈1000 times between -50°C and 150°C with no measurable degradation in k.
- Preliminary highly accelerated lifetime tests (HALT) predicted mean time-to-failure of ≈4000 h at 100°C under 260 kV/cm steady-state DC field.
- Presented program status and future direction to DOE APEEM projects kickoff and Annual Merit Review meetings.
- Published six papers in peer reviewed international journals and three papers in conference proceedings.
- Presented the results at four scientific conferences.

Future Direction

- Optimize processing conditions investigated in FY09 to produce high-voltage capable film-on-foils. Using small area top electrodes, the R&D effort in FY09 has demonstrated that the properties of PLZT film-on-foils are suitable for power electronics operating at under-the-hood temperatures. Important processing issues such as substrate polishing, defects in the films, clean room processing, pyrolysis and crystallization temperatures have been identified to make large area capacitors with the desired dielectric properties.
- In collaboration with Pennsylvania State University, characterize the dielectric properties and high temperature reliability of film-on-foils.
- Investigate electrode material and architecture to achieve benign failure in multilayers.
- Develop new fabrication methodology (dip-coating, aerosol deposition, tape casting) to reduce the capacitor cost.
- Build prototype multilayer film-on-foil capacitors and provide them to ORNL to test the device's performance and benchmark it against APEEM goals.
- Identify industrial partner to manufacture multilayer capacitors.

Technical Discussion

Argonne National Laboratory's (Argonne) capacitor R&D program addresses the technology gap in an innovative manner. We are developing high performance, low cost capacitors that are either stacked on printed wire board (PWB) or embedded directly into the PWB. In these "film-on-foil capacitors", a base-metal foil (nickel or copper) is coated with a high permittivity ferroelectric material, (Pb,La)(Zr,Ti)O3 (abbreviated as PLZT) via chemical solution deposition (CSD) technique. Ferroelectrics possess high permittivity, breakdown electric fields, and insulation resistance. They can withstand high temperatures such that high ripple currents can be tolerated at under-the-hood temperatures. Use of base-metals and solution-based deposition techniques reduce the cost. The stacked and embedded capacitors approaches significantly reduces component footprint, improves device performance, provides greater design flexibility, and offers an economic advantage for commercialization. This technology will achieve the high degree of packaging volumetric efficiency with less weight. Device reliability is improved because the number and size of interconnections are reduced. While this technology has primarily received attention for low voltage, high frequency decoupling capacitors, it can potentially be extended to the higher voltages of hybrid electric vehicle systems. The vision of embedded DC bus capacitors is compelling and offers US automotive companies a substantial technological advantage over their foreign counterparts. The bulky coke-can-like banks of capacitors can be replaced by lengths of capacitors tucked flat and neatly underneath the active components and bus structure. While embedding the film-on-foil capacitors into the PWB is the ultimate goal, the short-term practical approach is to target high voltage, high temperature, stacked capacitors for the inverter applications using film-on-foil dielectric layers. The short-term target will address the important issues, namely, weight, volume, and cost advantages of the film-on-foils compared to the conventional, bulky, wound polymer capacitors. Our R&D efforts focus on examining the issues that underpin the performance of film-on-foil capacitors, establishing fabrication protocols that are commercially robust and economically viable.

We have developed a core technology for fabricating CSD PLZT on Ni film-on-foil capacitors with $LaNiO_3$ (LNO) buffer layers. CSD solutions were synthesized at Argonne, and films were deposited by spin coating. Nickel substrates (25 mm × 25 mm, 0.5 mm thickness, 99.8% pure, ESPI Metals) were polished to 1-μm finish (≈0.4 mm final thickness) and ultrasonically cleaned in acetone and methanol prior to coating. Stock solutions of 0.3M $LaNiO_3$ (LNO) and 0.5M $Pb_{0.92}La_{0.08}Zr_{0.52}Ti_{0.48}O_3$ (PLZT) were prepared by modified sol-gel synthesis using 2-methoxyethanol as the solvent. The detailed procedure is reported elsewhere [1-4]. The LNO solution was spin-coated onto the substrate at 3000 rpm for 30 sec, pyrolyzed at 450°C for 5-10 min, and crystallized at 650°C for 2-5 min. This process was repeated five times to build the desired thickness with a final annealing at 650°C for 20 min. The PLZT stock solution was spin-coated onto the LNO-buffered substrate at 3000 rpm for 30 sec. Films were then pyrolyzed at 450°C for 10 min and crystallized at 650°C for 2-5 min, followed by a final annealing at 650°C for 20 min after repeating the coating steps to build up layers of sufficient thickness. By this process, we have fabricated PLZT films with thicknesses up to ≈3 μm. Platinum top electrodes were then deposited by electron beam evaporation using a shadow mask. These electrodes had diameters of 250 μm, 750 μm, and 12 mm and thickness of 100 nm. Films with top electrodes were annealed at 450 °C in air for 2 min for electrode conditioning. A Signatone QuieTemp® probe system with heatable vacuum chuck (Lucas Signatone Corp., Gilroy, CA) was used for electrical characterization. For the electrical measurements, the Pt/PLZT/LNO/Ni heterostructure was contacted by a Pt top electrode pad with one probe and the substrate (bottom electrode) with the other. A positive applied voltage corresponds to the configuration where the top electrode is at a higher potential than the bottom electrode. An HP 4192A impedance analyzer measured the capacitance and dissipation factor under applied bias field. A Radiant Technologies' Precision Premier II tester measured the hysteresis loops. The capacitor samples were immersed in Fluka silicone oil (Sigma-Aldrich) during high-field hysteresis loops and dielectric breakdown measurements. A Keithley 237 high-voltage source meter measured the current-voltage characteristics. The leakage current density was determined by fitting the current density relaxation data to the Curie-von Schweidler equation [5].

The PLZT films grown on LNO-buffered Ni foils were phase pure with no preferred crystallographic orientation as shown by X-ray diffraction, and no crack or delamination was observed from SEM [1]. Average grain size of ≈60 nm was determined from SEM and confirmed by AFM [3]. The use of LNO buffer allows the film-on-foils to be processed in air without the formation of a parasitic interfacial nickel oxide layer. The LNO also compensates for the roughness of the Ni foil and provides a smooth interface for the PLZT films, resulting in higher breakdown strengths. In addition, the LNO buffer helps to reduce the compressive strain in the PLZT films deposited on nickel substrates due to the thermal expansion coefficient mismatch between PLZT and metal foils [6]. We measured relative permittivity of 1300 and dielectric loss of ≈0.05 on PLZT film grown on LNO-buffered Ni substrate.

Figure 1 shows the time relaxation for the current density measured on 1.15-μm-thick PLZT/LNO/Ni sample at 25°C and 150°C with a constant bias potential of 10 V (corresponding to an applied electrical field ≈8.7×10^4 V/cm) across the top and bottom electrodes. The measurements were conducted by keeping the top Pt electrode positive and the bottom Ni electrode grounded. Both curves show strong initial time dependence, indicating depolarization process. The current density measured at 150°C is roughly a factor of two higher than that measured at 25°C. The decay in dielectric relaxation current obeys the Curie-von Schweidler law [5],

$$J = J_s + J_0 \cdot t^{-n} \qquad (1)$$

where J_s is the steady-state current density, J_0 is a fitting constant, *t* is the relaxation time in seconds, and *n* is the slope of the log-log plot. Fitting the data to Eq. 1, we found *n* values of 0.99 and 0.97 and

leakage current densities of 6.6×10^{-9} A/cm^2 and 1.4×10^{-8} A/cm^2 for the measurements at room temperature and 150°C, respectively.

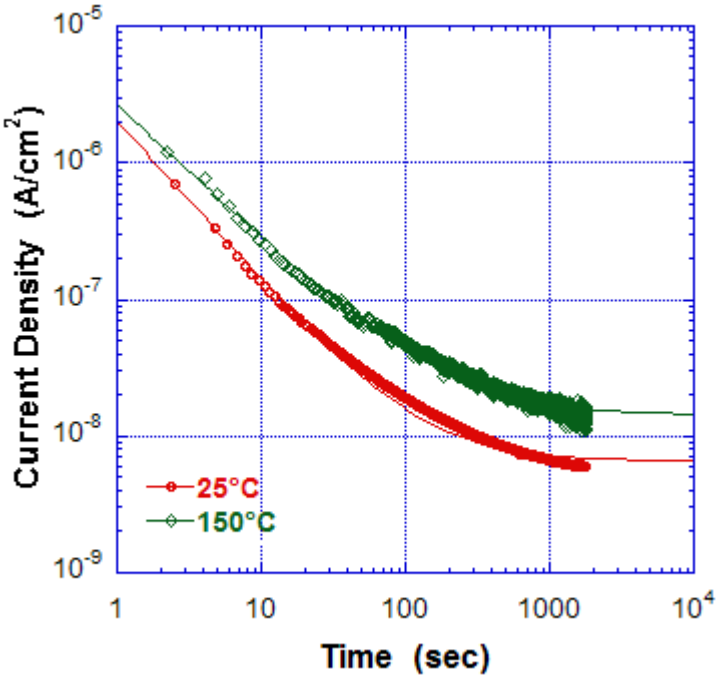

Figure 1. Time-relaxation current density measured on a PLZT/LNO/Ni sample under 8.7×10^4 V/cm electric field at room temperature and 150°C.

Weibull statistical analysis [7,8] were employed for assessment of reliability of film-on-foil capacitors under varying conditions of applied voltage and temperature, where time to failure was recorded under specific stress conditions. We utilized the following empirical relationship involving the mean time to failure (MTTF) [also know as mean time before failure (MTBF)] t, applied voltage V, and testing temperature T [9,10] for our data analysis,

$$t = C \cdot V^N \exp\left(\frac{E_a}{k_B \cdot T}\right) \qquad (2)$$

where, C is a constant, E_a is a pseudo-activation energy, N is the voltage acceleration factor, k_B is the Boltzmann constant, and T is the absolute temperature measured in K.

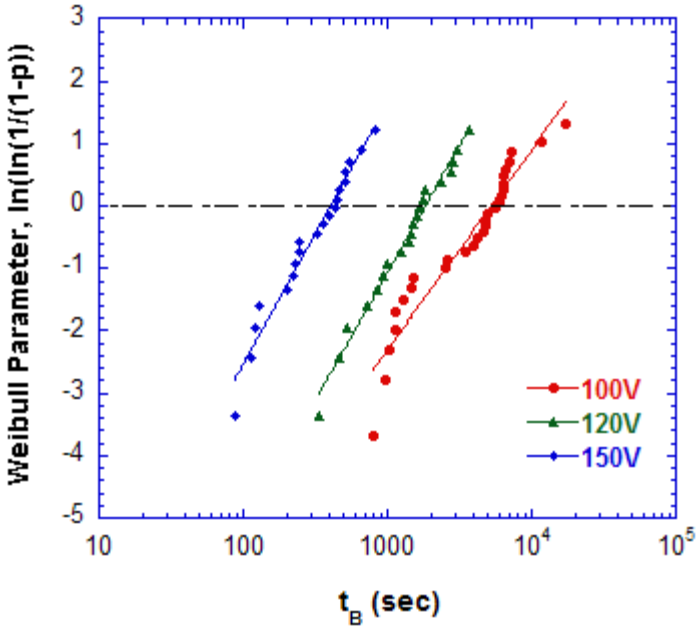

Figure 2. Weibull plot of time to breakdown for data measured at 100°C on Pt/PLZT/LNO/Ni film-on-foil capacitors with 1.15-µm PLZT layer.

Figure 2 shows the Weibull plot of time to breakdown data measured on 1.15-µm-thick PLZT/LNO/Ni film-on-foil capacitors under three different applied electric fields. The straight lines are least square fittings of experimental data to the 2-parameter Weibull function.

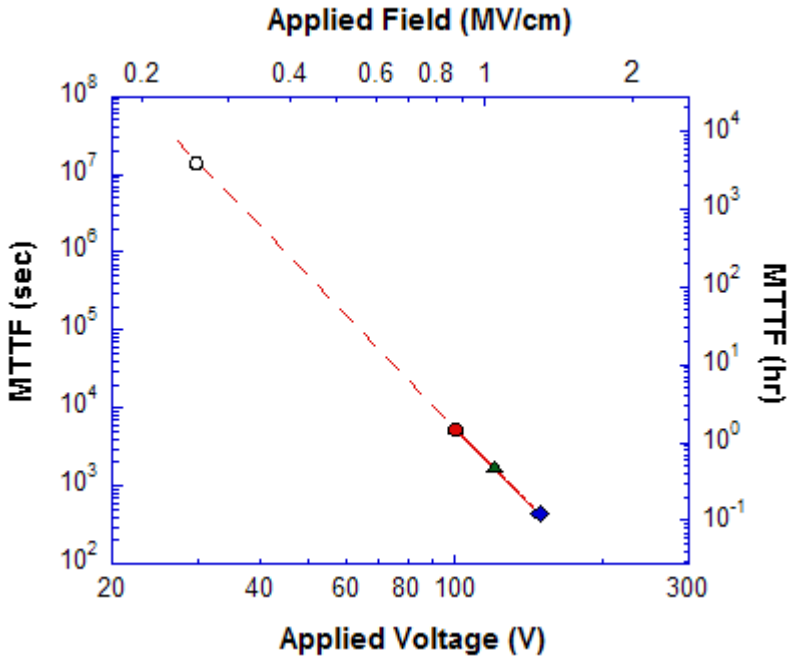

Figure 3. Mean time to failure as a function of applied voltage for the 1.15-µm-thick PLZT/LNO/Ni film-on-foil capacitors measured at 100°C.

MTTF values measured at 100°C on the 1.15-µm-thick PLZT/LNO/Ni film-on-foil capacitors are plotted in Fig. 3 as a function of applied field. Three different symbols correspond to those used in Figure 2 for data measured under different voltages. Solid straight line is the fitting to equation (2), and the dashed line is the extrapolation of solid line. A voltage acceleration factor N = -6.3 observed at 100°C for the PLZT film on nickel foil capacitors. This value is comparable to the value of N = -7.8 reported on $PbZr_{0.52}Ti_{0.48}O_3$ (PZT 52/48) grown on platinized silicon substrates [9]. The open dot shown in Figure 3 illustrated the fact that we can expect the capacitors to have a MTTF value greater than 3000 hrs when it is operated at 100°C with 30 V (corresponds to 2.6×10^5 kV/cm) electric field stress applied on the 1.15-µm-thick PLZT film on nickel foil.

Until last year we were characterizing the film-on-foils using 250-µm-diameter top electrodes. In FY09 we were able to improve the properties over larger areas of the PLZT films by controlling the processing conditions. Film-on-foils are characterized using 5-mm-diameter top electrodes (an increase in area of capacitor by a factor of about 400 times compared to what was produced until last year). Figure 4 shows the dielectric constant and dielectric loss vs. bias field on a 1.15-µm-thick PLZT film measured using a 5-mm-diameter top electrode. A dielectric constant of ≈1100 and dielectric loss ≈0.07 are measured using a 5-mm-diameter top electrode.

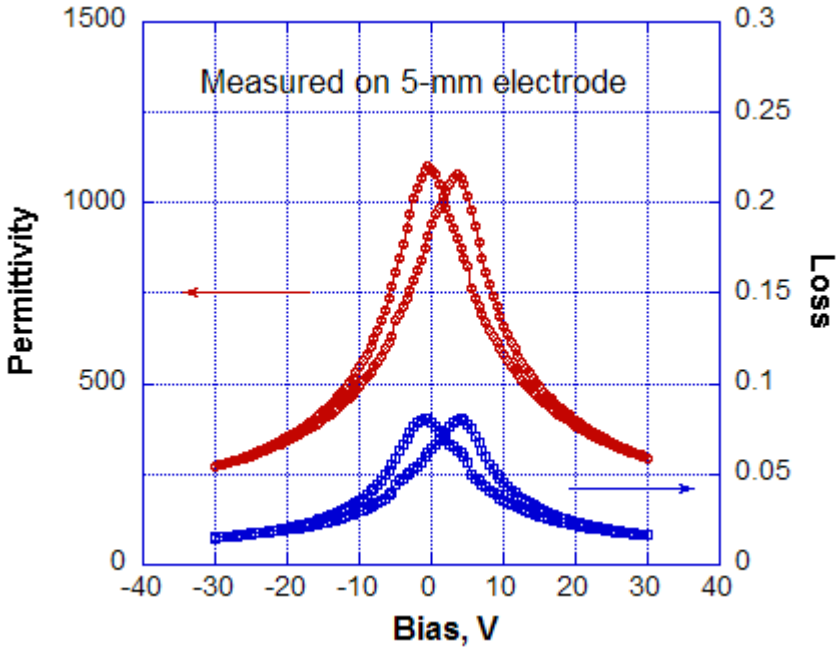

Figure 4. Relative permittivity and dielectric loss measured at room temperature as a function of applied bias field for a PLZT/LNO/Ni film-on-foil capacitor (measured on a 5-mm-diameter top electrode).

One of the PLZT films (1.15-µm-thick) was characterized using ≈12-mm-diameter (area about 1800 times compared to what was produced in FY09) and the measured dielectric constant and capacitance vs. bias field are shown in Figure 5. As seen in Fig. 5, we measured a capacitance of 0.9 µF on this film at zero bias. From the polarization-field loop at high fields, we measured a capacitance of ≈0.2 µF at 80 V.

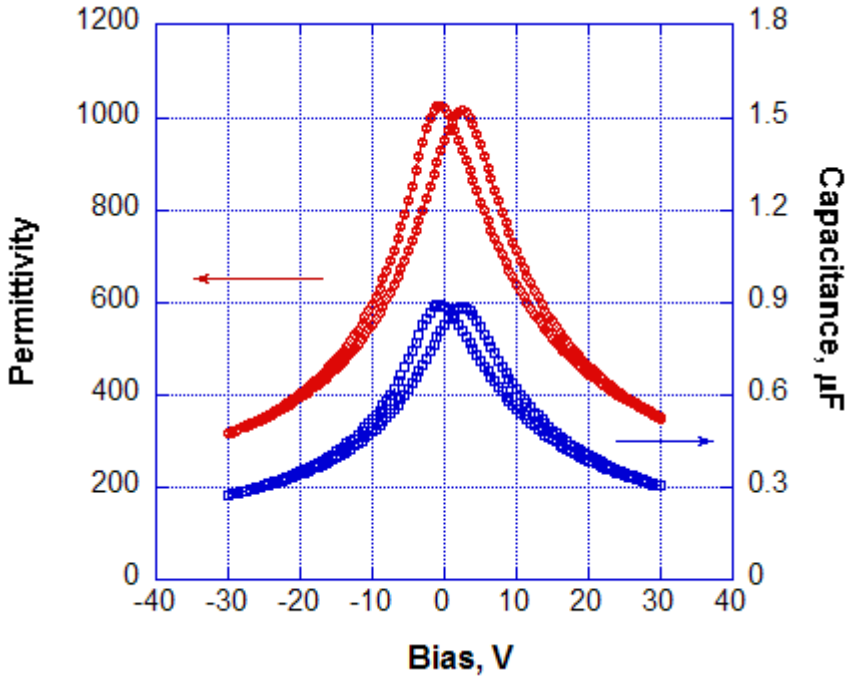

Figure 5. Relative permittivity and capacitance measured at room temperature as a function of applied bias field for a PLZT/LNO/Ni film-on-foil capacitor (measured on a 12-mm-diameter top electrode).

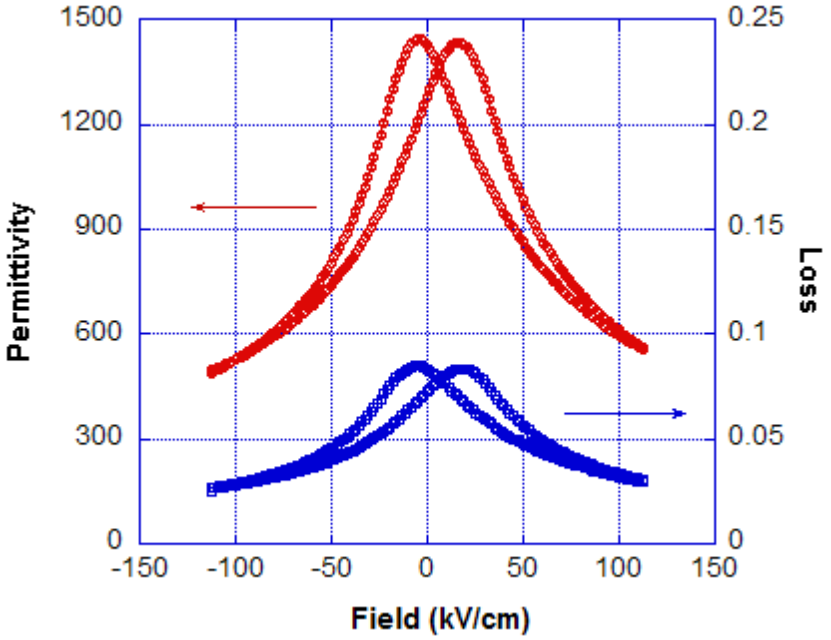

Figure 6. Relative permittivity and dielectric loss measured at room temperature as a function of applied bias field for a ≈3- μm-thick PLZT/LNO/Ni film-on-foil capacitor (measured on a 750-μm-diameter top electrode).

The dielectric films should withstand the operating voltage of 450 V for inverter applications and therefore, the films need to be thick enough to withstand the high voltages. Recently, we fabricated a ≈3-µm-thick PLZT film on LNO buffered Ni foil and characterized the film's properties using 750 µm diameter top electrodes. Figure 6 shows the dielectric constant and dielectric loss vs. bias field measured on a ≈3-µm-thick PLZT film using 750 µm diameter top electrodes. We measured a dielectric constant over 1300 at zero bias.

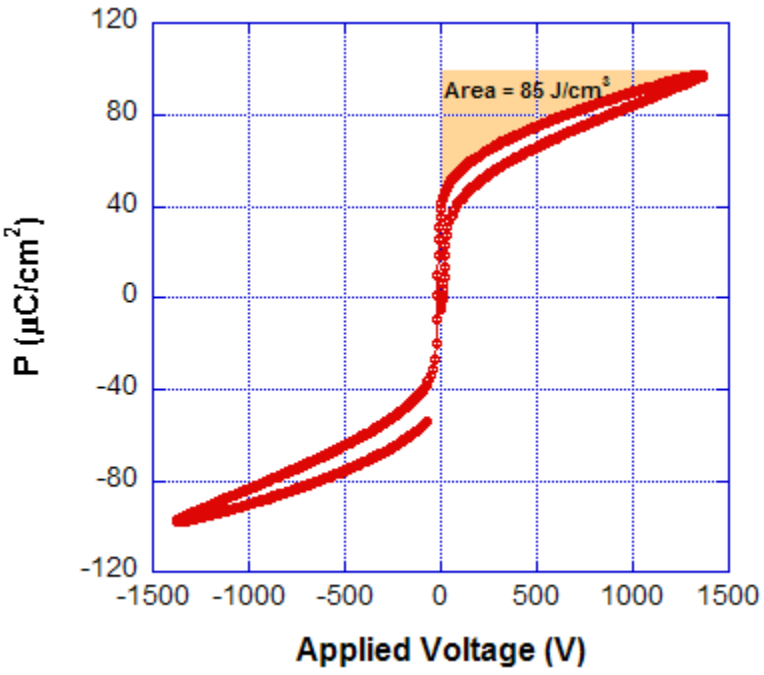

Figure 7. Polarization-field loop measured at room temperature on a ≈3- µm-thick PLZT/LNO/Ni film-on-foil capacitor (measured on a 750-µm-diameter top electrode).

Figure 7 shows the polarization-field loop measured with maximum applied voltage of 1400 V on a ≈3-µm-thick PLZT film using a field sweeping frequency of 1 KHz. By fitting and integration of the discharging portion of the P-E hysteresis loop curve, we measured an energy density of ≈85 J/cm^3 (at 1400 V) as indicated by the shaded area shown in Fig. 7. Estimated energy density at 600 V is ≈15 J/cm^3. From the P-E loop measurement, we calculated the dielectric constant of this film to be ≈200 at 300 V and ≈120 at 600V. These unique properties (high dielectric constant, outstanding breakdown strength, and high energy density) demonstrated that these film-on-foils can potentially be used for high-voltage power electronic systems in hybrid electric vehicles.

Conclusion

We have developed a core technology for fabricating high capacitance density PLZT film capacitors on base metal foils. PLZT film-on-foil capacitors have been fabricated with LNO buffer layers atop Ni foils, allowing the capacitors to be processed in air. We have fabricated a 12-mm diameter film-on-foil dielectric (≈1.15 µm-thick PLZT) with capacitance of 0.9 µF at zero bias. Significant improvements have been made in increasing capacitor area compared to previous years. A ≈3 µm-thick PLZT film to withstand high voltage (operating voltage of 450 V) has been fabricated and its P-E loop measurement was made with applied voltage as high as 1400 V. Highly accelerated lifetime tests were conducted at 100°C to determine the reliability of the film-on-foil dielectrics under field stress conditions. The

properties measured show that these film-on-foils have potential to meet the APEEM goals. The primary emphasis of FY10's effort is toward advancing the proven laboratory scale film-on-foil technology towards fabricating high-voltage capable thick dielectric films with uniform properties over larger areas suitable for high temperature inverters for applications in hybrid electric vehicles.

Publications

We have over 35 publications and presentations, and few selected publications are listed below.

1. B. Ma, M. Narayanan, S. Tong, U. Balachandran, *Fabrication and Characterization of Ferroelectric PLZT Film Capacitors on Metallic Substrates*, Journal of Materials Science (in press, 2009, available on line, doi: 10.1007/s10853-009-3910-0).
2. U. Balachandran, D. K. Kwon, M. Narayanan, B. Ma, *Development of PLZT Dielectrics on Base-Metal Foils for Embedded Capacitors*, Journal of the European Ceramic Society (in press, 2009, available on line, doi:10.1016/j.jeurceramsoc.2009.05.006).
3. B. Ma, D. K. Kwon, M. Narayanan, U. Balachandran, *Dielectric Properties and Energy Storage Capability of Antiferroelectric $Pb_{0.92}La_{0.08}Zr_{0.95}Ti_{0.05}O_3$ Film-on-Foil Capacitors*, Journal of Materials Research, **24**, 2993, 2009.
4. B. Ma, D. K. Kown, M. Narayanan, and U. Balachandran, *Chemical Solution Deposition of Ferroelectric Lead Lanthanum Zirconate Titanate Films on Base-Metal Foils*, J. Electroceram., **22**, 383, 2009.
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10. R. Munikoti and P. Dhar, IEEE *Transactions on Components, Hybrids, and Manufacturing Technology* **11**, 342-345, (1988).

Patents

D. K. Kaufman, S. Saha, *Ceramic capacitor exhibiting graceful failure by self-clearing method for fabricating self-clearing capacitor*, US Patent #7,009,141, August, 2006.

4.8 Glass Ceramic Dielectrics for DC Bus Capacitors

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Objectives

Commercial capacitors for hybrid electric vehicles (HEVs) and plug-in hybrid electric vehicles (PHEVs) do not meet US automaker's specifications for high temperature operation, cost and reliability. The objectives of this project are to develop high temperature capacitors that go beyond what is commercially available and to minimize the need for costly coolant systems within the HEVs and PHEVs. Ceramic capacitors have excellent high temperature performance and meet a majority of HEV and PHEV specifications for power electronic converters; however, low reliability is a primary impediment to their use in hybrid vehicles. The goal of this project is to produce reliable glass capacitors without compromising the energy density (related to capacitor volumetric efficiency). Specific goals include:

- Characterize the thickness dependence of dielectric breakdown of commercial flat panel display glass that is manufactured by Corning, Schott, and Nippon Electric Glass
- Collaborate with Argonne National Laboratory to understand coated conductor breakdown strength and reliability.
- Commercialize glass capacitor technology by collaborating with glass manufacturers and capacitor companies.

In addition, the project will leverage promising new glass materials that were previously developed for consumer electronics. This project provides an integrated development effort that involves materials, capacitor, and power electronic companies. Specific technical objectives include:

Approach

- Adapt low-cost production methods and materials, already developed for flat panel displays, to high temperature capacitors.
- Characterize glass materials at high temperature to project reliability.
- Develop benign failure modes in glass capacitors to avoid catastrophic failure.
- Manufacture prototype capacitors in collaboration with industrial partners.

Major Accomplishments

- Demonstrated that flat panel display glass can operate as a capacitor up to temperatures of 250 °C.
- Demonstrated thickness dependent dielectric breakdown and the statistics for making glass capacitors more reliable
- Submitted a patent disclosure "Self healing high energy glass capacitors".

Future Direction

- Scale-up glass capacitors to 10 µF 1,000 V levels - large-scale capacitors that are based on flat-panel display glass will require a multilayer construction. This project will develop robust terminations for multilayer glass capacitors.
- Penn State has been working with flat-panel display manufacturers to reduce the glass layer thickness. Currently 50 µm thick glass sheets are available and 10 µm thick sheets have been fabricated at the

laboratory scale. The final design for a high-temperature DC link capacitor will require glass layer thicknesses between 5 and 10 µm.

Technical Discussion

There is general agreement within the automotive and power electronic communities that revolutionary approaches, drawing on diverse disciplines, will be necessary to develop the next generation of power systems for electric vehicles. New active and passive components need to be manufactured which can operate at high temperature for long periods of time. In addition, component miniaturization is important to reduce the total volume of the power electronic circuitry on board an electric vehicle. A summary of the results of this study is shown in Figure 1.

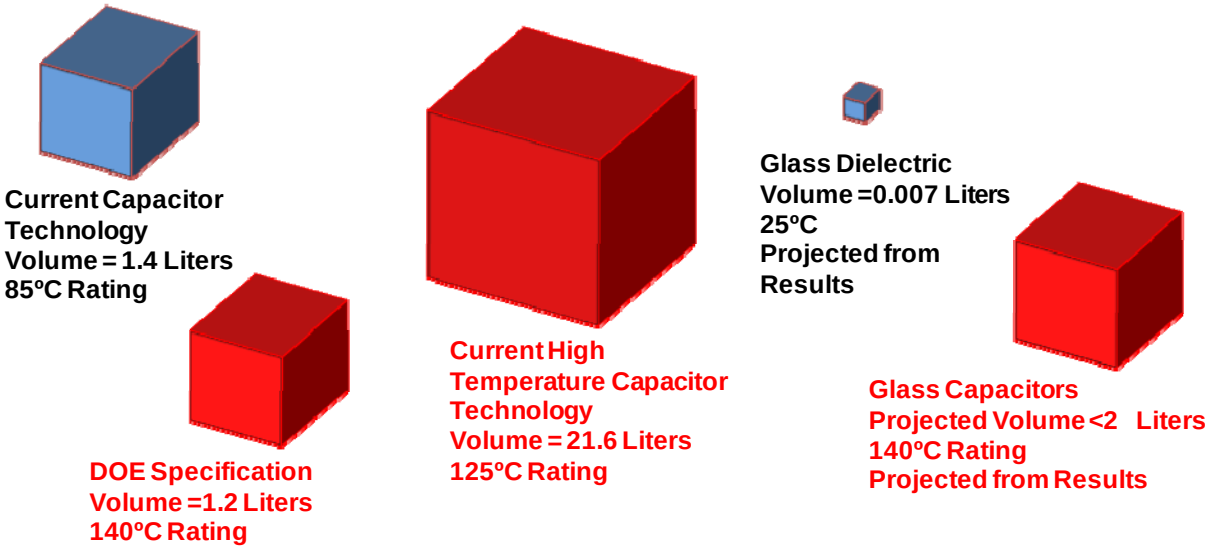

Figure 1. Volumetric comparison between DOE capacitor specifications, commercial capacitors and the projected capacitor volumes from the research at Penn State. All volumes shown are for a 1000 µF 1000 V capacitor.

The DOE specifications (Figure 1 lower left corner) were derived from discussions with the EE tech team and component manufacturers. Presently, high-temperature film capacitors (middle of Figure 1) have 18 times the volume of the DOE specification. The glass dielectrics explored in this study have the potential to operate above 140ºC and the volume is much smaller than commercial high temperature capacitors (Figure 1 right side).

Thin glass sheet production has grown substantially because of strong demand from the flat panel display industry and a $30 billion investment in the development of new glass fabrication methods [1]. Within the past year, Penn State has utilized an etching technique to reduce the commercially available glass thicknesses from 50 µm to 5 µm. The thickness reduction is a key factor in increasing the dielectric breakdown strength and the mechanisms associated with this improvement are under investgation. As shown in Figure 2, the mechanical properties of the etched glass sheet are impressive and the electrostatic energy density of 38 J/cm^3 is

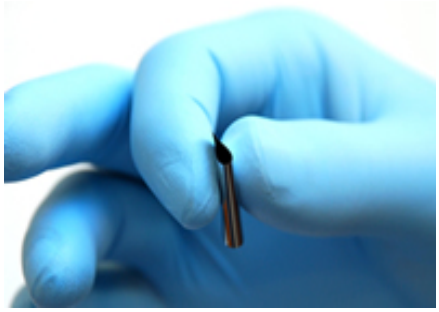

Figure 2. Demonstrating the mechanical flexibility and strength of chemically etched 10-µm thick glass sheet.

among the highest reported for any dielectric material. Another benefit is low dielectric loss (tan δ < 0.01, 1 kHz) up to 300 ºC [2].

A great variety of breakdown mechanisms exist in glass which is related to capacitor reliability. The dominant breakdown mechanism for a given sample is determined by many factors including dielectric and conducting characteristics of individual layers and of the interface. A schematic of a self healing breakdown event is shown in Figure 3.

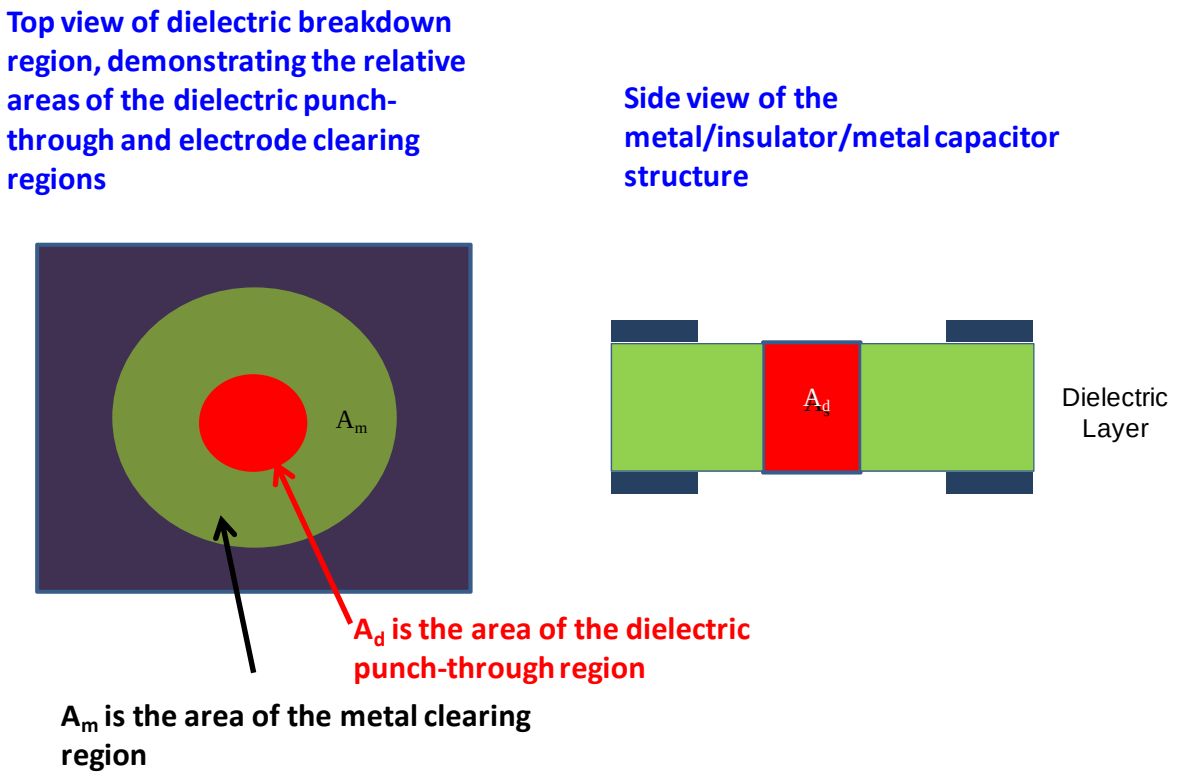

Figure 3. Anatomy of a dielectric breakdown event in a glass capacitor. The dark region is the metal conductor and the green region is the glass. As the glass fails, the electrical discharge transports through the red region (A_d) and heats the metal conductor up to the vaporization point. The green region (A_m) represents the metal that is removed from the glass surface.

Recently, we have observed graceful failure in thin glass sheets; however, not all of the breakdown events are benign (Figure 4). Detrimental cracking of the glass layer and inadequate conductor clearing are observed after a shorting dielectric breakdown. We anticipate that many of the benefits that are common in polmer capacitors (enhanced large-scale manufacturing and ease of graceful failure) will be achievable in a glass capacitor.

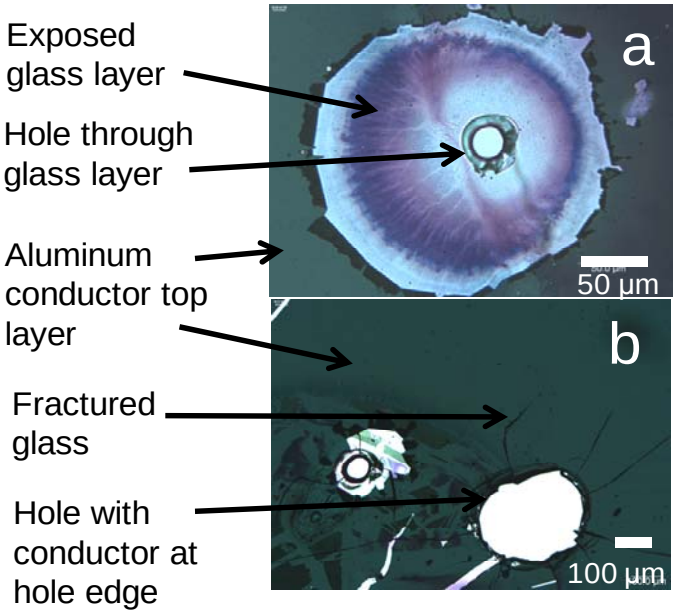

Figure 4: (a) Graceful and (b) catastrophic dielectric failure modes in a 15 µm thick glass layer with evaporated 10 nm thick aluminum electrodes. Fig. 4a shows a classic graceful failure mode with a significant clearing of the electrode away from the glass and very little damage to the glass. Note that the hole has a ring of glass that has melted during the breakdown event. Fig. 4b illustrates extended fracture due to thermal shock and the electrodes cover the entire glass layer except for the hole created by breakdown. Note a significant cracking in the lower left hole for Fig. 4b. The characteristic dielectric breakdown of the 10 µm thick glass layers is 10 MV/cm and the energy density exceeds 30 J/cm3 in these samples with aluminum electrodes that are 3 mm in diameter.

Scale-up efforts at Penn State have resulted in the construction of large area capacitors (Figure 5). The prototypes that are shown in Figure 5 were made by cutting larger glass sheets (45 cm x 35 cm) into 10 cm x 10 cm sheets. The glass sheets were supplied by Schott Glass company. Electrodes were applied to the glass sheets by a screen printing process in which silver ink was deposited on the glass surface and heat-treated to form a continuous metal conductor. The capacitors shown in the Figure 5 are single layer and we anticipate that multilayers be made in the next fiscal year. Protective outer glass layers were added to increase the mechanical stability of the structure. End terminations are currently a key concern with multilayer glass capacitor construction and we are investigating several types of conducting inks.

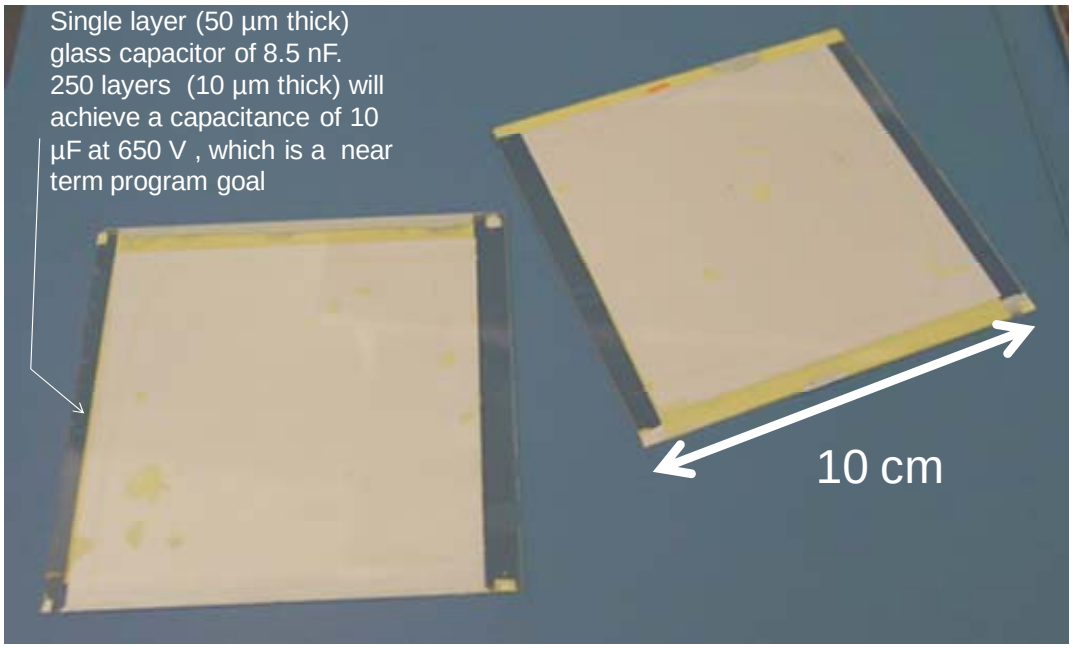

Figure 5. Prototype glass capacitors fabricated at Penn State University (Fabricated by Amanda Baker)

Conclusion

The outcome of this project is a cost effective manufacturing process for high temperature capacitors that will meet the US automaker specifications for HEV and PHEV applications. Penn State has collaborated with several industrial partners including large raw materials manufacturers (Corning Inc. and Schott Glass USA) and small capacitor manufacturers (TRS Technologies) to investigate reliable prototype capacitors from glass-ceramic materials.

Publications

1. C. A. Randall , H. Ogihara, S. S. N. Bharadwaja, M. T. Lanagan, S. Trolier-McKinstry, C. Stringer, Potential High Temperature, High Energy Density Dielectrics for Multilayer Ceramic Capacitors for Power Applications, 17th Annual IEEE Pulsed Power Conference, Washington DC, June 28 -July 2, 2009.
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Patents

1. Patent Submitted: M. Lanagan, N. Smith, H.K. Lee, C. Pantano, and R. Rangarajan "Self-healing high energy glass capacitors," Penn State invention 48718/36

4.9 High Temperature Thin Film Polymer Dielectric Based Capacitors for HEV Power Electronic Systems

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Objectives

DC bus capacitors are currently the largest and the lowest reliability component of fuel cell and electric hybrid vehicle inverters. Furthermore, current DC bus capacitors cannot tolerate temperatures greater than 120°C. Our project goal is to develop a replacement high energy densisty, high temperature dielectric for DC bus capacitors for use in hybrid electric vehicles (HEVs) and plug in hybrid electric vehicles (pHEVs). The improved capacitors will be based on inexpensivie novel high temperature polymer thin film dielectrics. Our technical goal is to enhance high temperature performance and volumetric efficiency of capacitors when compared to present dielectrics. Specific metrics include the development of polymer film dielectrics with dissiaption factors of 0.02 or less at 150 ºC. Synthesis, fabrication, and high temperature (100 to 150 ºC) characterization of these dielectric materials is an integral part of the material development program. In addition, work will focus on transitioning the material to industry to produce rolls of the novel high temperature polymer dielectric film will lead directly to the production of a prototype capacitor.

Approach

Sandia National Laboratory's (Sandia) capacitor R&D program addresses the technology gap in an innovative manner. We are developing high performance, high temperature, low cost capacitors that are based on novel Sandia developed polymer chemistry. Capacitors fabricated using this polymer technology will achieve a high degree of packaging volumetric efficiency with less weight while being able to operate at temperatures as high as 150 ºC. Our R&D efforts focus on 1) producing polymer film at Electronic Concepts, Inc. (ECI) in an appropriate quantity to fabricate prototype capacitors and 2) using the optimum polymer film stoichiometry as a starting point to improve the dielectric breakdown with the addition of appropriately modified nanoparticles.

Major Accomplishments

- Scaled up the polymer dielectric synthesis and produced a "spool" of cast high temperature dielectric polymer at ECI
- Identified the functional group within the polymer that was causing polymer solution instability
- Evaluated the inclusion of silica and titania nanoparticles with and without surface functionalization
- Identified, synthesized and characterized a higher temperature polymer system (>200˚C)

Future Direction

The R&D effort has demonstrated feasibility of using high temperature dielectrics for power electronics operating at high temperatures (150 ºC). Progress achieved thus far sets the stage to begin fabrication of prototype high temperature capacitors. These capacitor fabrication efforts will require the development of polymer casting conditions that allow the production of large rolls (>100 m length) of polymer dielectric films. We will continue to work with our industrial partner (ECI) to produce a desired amount of polymer dielectric film capable of prototype capacitor formation. Research in FY09 led to the discovery of the chemistry that was inhibiting the large scale film formation. Work in FY10 will focus on the removal of the crosslinkable double bonds in the backbone of the polymer to yield polymer casting solutions with greatly enhanced shelf life. We will further work with ECI to produce several prototype capacitors. At least six prototype capacitors will be evaluated and benchmark them against APEEM goals. In addition, we will produce at least six "stacked" capacitors at Sandia National Labs in the event that we are unable to produce six rolled prototype capacitors at ECI. These initial prototype capacitors (rolled or stacked) will be evaluated by ORNL as well as other research institutions. We will continue our effort in developing dielectric materials with improved performance focusing on the incorporation of nanoparticle fillers to increase the energy density further.

Technical Discussion

1.0. Polymer Film Production Leading to Capacitors

An industrial partner (ECI) was identified in January 2008 to begin the fabrication of large rolls (>100 m length) of polymer films. Initially a purchase order was placed to begin the production of polymer films. An initial amount of 1 kg of the identified polymer (**1**, Figure 1) was sent to ECI where several solvents and solvent combinations were evaluated in order to produce the required rolls of polymer film. The initial attempts to cast on a larger scale yielded only small amounts of polymer film. Work during FY09 continued to focus on development of the "pilot scale" process that would yield a large roll of polymer dielectric film. Again the work with ECI, began with Sandia synthesizing 1 kg of polymer **1** which was sent to ECI for large scale casting experiments.

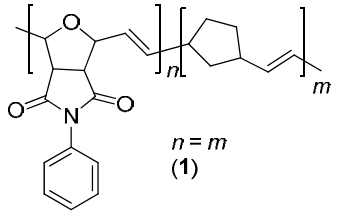

Figure 1. Structure of the high temperature polymer dielectric polymer

A switch to dichloroethane resulted in the fabrication of a larger length of polymer film than had been cast the previous year (Figure 2), however, the polymer solutions were not stable for long periods of time.

Figure 2. Spool of the high temperature polymer dielectric produced at ECI

A typical procedure to produce polymer film started with forming a solution of the polymer in dichloroethane and casting the polymer. Unused polymer solution would be stored in air usually over a weekend. When the polymer solution was examined at a later time point, it was observed that the polymer was precipitating out of solution and did not go back into solution upon heating or stirring. These results are consistent with the crosslinking of the double bonds in the backbone of polymer **1** as shown in Figure 3.

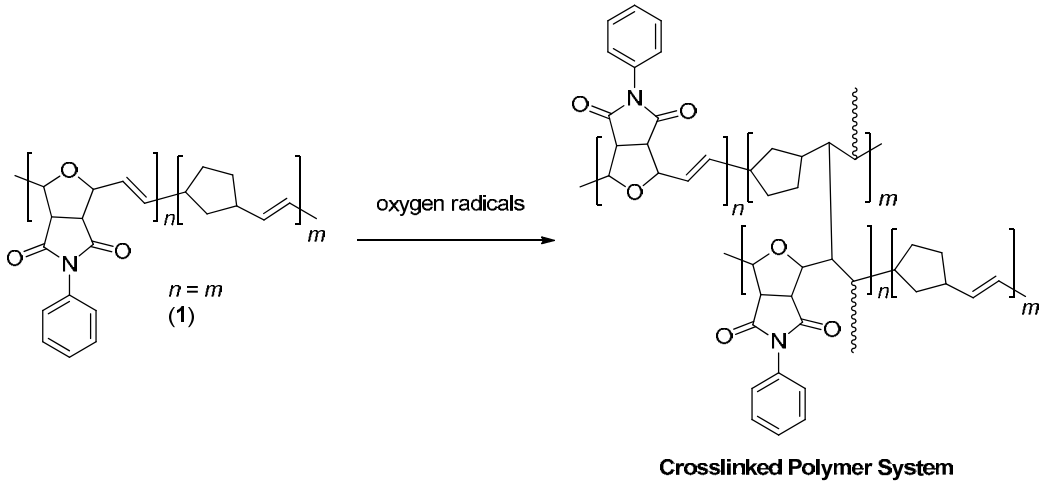

Figure 3. Crosslinking reaction that results in polymer precipitation from casting solutions

Removal of the reactive double bonds was then evaluated as a potential method of enhancing polymer solution lifetime, thus improving our ability to produce a large roll (>100 m) of polymer film. Initial reactions involving hydrogenation used *p*-toluenesulfonyl hydrazide as the hydrogen source. In practice less expensive hydrogen gas could be used in combination with a hydrogenation catalyst. Hydrogenation of a model polymer system (**2**) produced the desired hydrogenated polymer (**3**) is shown in Figure 4.

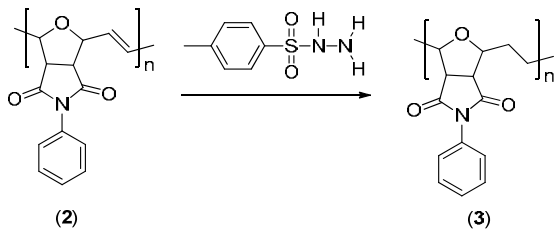

Figure 4. Hydrogenation of a model polymer dielectric

Electrical characterization polymers 2 and 3 were performed to determine the effect of the double bond on dissipation factor, dielectric constant, and breakdown strength. The dissipation factors were identical when measured at 1 kHz for both polymers 2 and 3 with values of 0.017. The dielectric constant of the hydrogenated polymer (2) decreased 20% when compared polymer 3. The breakdown strength (when analyzed using Weibull statistics) did however increase with the removal of the double bonds as shown in Figure 5. The net result of the change in dielectric constant and breakdown strength is an increase in polymer dielectric energy density.

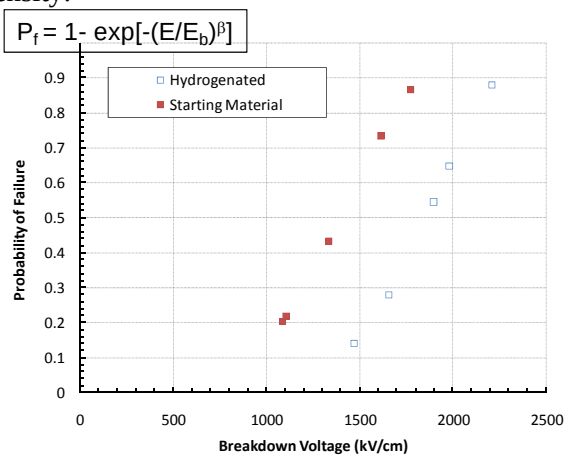

Figure 5. Dielectric breakdown of a model hydrogenated polymer dielectric compared to the starting polymer

2.0. Nanoparticle Filled Polymers for Increased Breakdown Strength

The energy density of polymer **1** was determined to be 0.21 J/cm^3, when measured using 30 pF capacitors as the test structures. In an effort to increase the energy density of the polymer we evaluated the use of very inexpensive nanoparticle fillers consisting of silica and titania. We evaluated the effect the nanoparticles had on breakdown strength by directly bending the nanoparticles into the polymer **1** and we also evaluated capping the nanoparticles using siloxane chemistry and then blending the nanoparticles into the polymer. Silica nanoparticles (20 nm) were functionalized according to Figure 6.

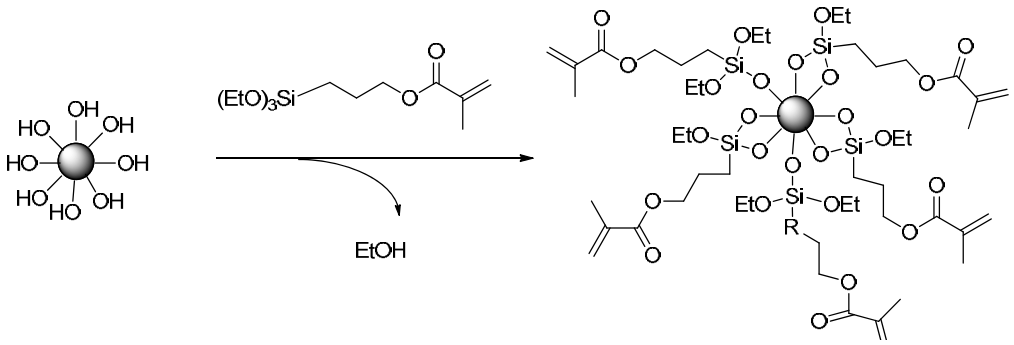

Figure 6. Functionalization of silica nanoparticles using siloxane chemistry

Thin polymer dielectric films were prepared using both the functionalized and unfunctionalized nanoparticle filled polymer composites. The films were metalized and breakdown strengths were measured and compared with non-nanoparticle filled polymer **1**. Figure 7 shows the breakdown strength comparison for the polymers and polymer composites evaluated using 8% nanoparticle filler.

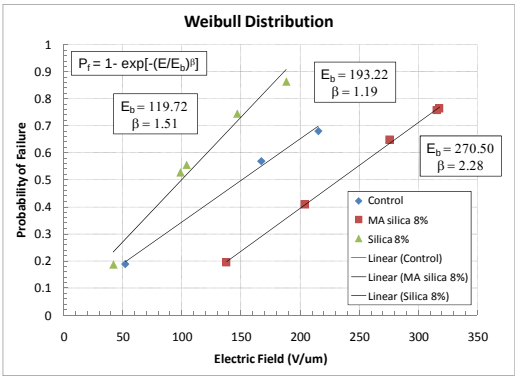

Figure 7. Dielectric breakdown of a nanoparticle filled polymer dielectrics

The methacrylate capped nanoparticles helped to facilitate blending and as a result increased the dielectric breakdown strength when compared to polymer 1 (control) by 77 V/µm. When the nanoparticles are not functionalized poor blending and dispersal of the nanoparticles occurs and the dielectric strength actually decreases by 75 V/µm. The increase or decrease in dielectric strength may pictorially be described by Figure 8.

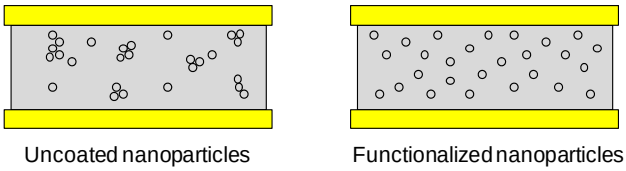

Figure 8. Dispersal of nanoparticles within the polymer dielectric is effected by the surface functionalization

The silica nanoparticles have polar hydroxyl surface functionalization and tend not to disperse within the polymer 1 matrix. The lack of dispersal results in localized electric fields which lead to lower breakdown strengths. If the nanoparticles are coated appropriately they disperse within the polymer matrix and increase the dielectric breakdown strength. The observation of increased breakdown strength using modified nanoparticles was also observed with titania particles (results not shown).

The nanoparticle loaded composites also exhibited graceful failure as is shown in Figure 9 with TiO_2 loaded polymer **1**. The data shown is for uncoated nanoparticles, however, the same graceful failure was observed for methacrylate capped titania and silica.

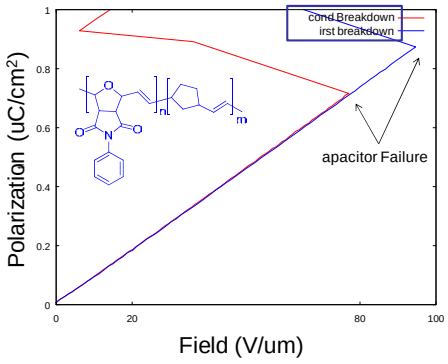

Figure 9. An example of graceful failure of nanoparticle loaded dielectrics

3.0. Alternative High Temperature Polymers

A new type of polymer system was also explored using diphenyl-polyphenylene vinylene (DP-PPV) precursor polymers which were synthesized according to figure 9. Hsieh and coworkers have previously reported the synthesis and electroluminescent properties of DP-PPV converted from a chloro precursor polymer.[1,2] Synthesis of intermediates **6, 7, 8, 9**, and the chloro-precursor polymer (4) are based on these reports.

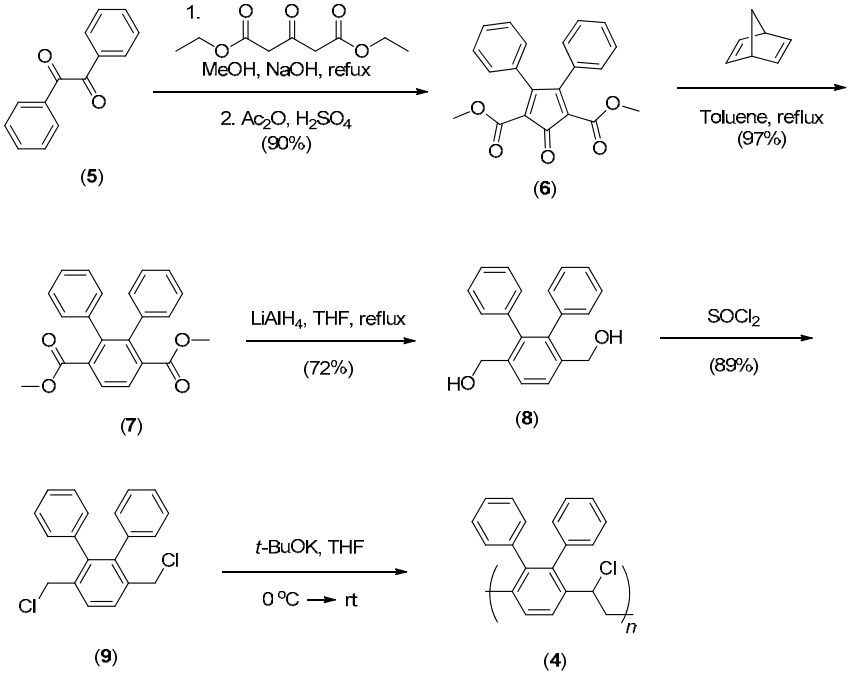

Figure 9. Alternative high temperature polymer dielectric

Thin films of the polymers were prepared using a drawdown machine casting onto a Teflon substrate. The thin polymer films (~20 µm thick) were metalized with Au electrodes and the electrical properties were measured as a function of frequency and then as a function of temperature. The electrical data is shown in Figure 10. Dielectric films fabricated using the chloro-polymer functioned to 200 °C.

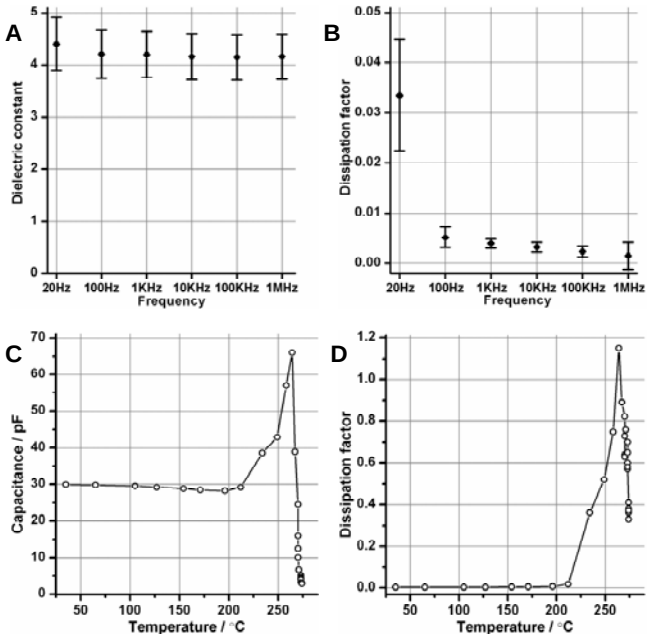

Figure 10. Electrical measurements of thin film capacitors made from the chloro-precursor polymer. (A) Dielectric constant and (B) dissipation factor at varying frequencies. (C) Capacitance and (D) dissipation factor as a function of temperature.

Conclusion

We have developed a novel polymeric material that has superior high temperature dielectric properties and are working with and industrial partner (ECI) to fabricate large rolls (> 100 m length) of polymer dielectric film leading to prototype capacitor fabrication. Through this industrial interaction we have identified the cause of decreased polymer solution lifetimes and are correcting the problem by removing the reactive double bonds without compromising the dielectric performance. Furthermore, we have identified nanoparticle functionalization chemistries that improve nanoparticle dispersal and as a result increase dielectric breakdown strength. We have also identified an alternative high temperature dielectric that performs up to 200 °C. These high temperature polymer film technologies will be used to fabricate high temperature DC bus capacitors with significantly reduced size and weight, and improved performance and reliability.

Publications

1. Dirk, S. M.; Sawyer, P. S.; Wheeler, J.; Stavig, M.; Tuttle, B., High Temperature *Polymer Dielectrics from the Ring Opening Metathesis Polymerization (ROMP)* Proc. - IEEE Int. Pulsed Power Conf., 2009.
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4.10 Bi-Directional DC-DC Converter for PHEV Applications

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Objectives

The objective of this project was to investigate the efficiency and cost advantages of a Bi-Directional DC-DC Converter (BDDC) with a Dual Battery Storage (DBS) system. The overall performance was to meet the following criteria:

1. To provide a vehicle system level study (in close collaboration with the drive system, charging system, energy system and vehicle mission and drive cycle requirements) to determine the optimum operating battery and dc-link voltage levels that maximize efficiency and minimize cost;
2. Design and develop a bi-directional dc/dc power-conversion system in support of PHEV program to meet the commercialization cost, weight, and volume;
3. To design, develop, and complete performance validations of the production-intent prototype high power density power 8 kW multi-phase bidirectional dc/dc boost converter.
4. To meet the following product-design targets:
   - ≥ 95% power-conversion efficiency at junction temperatures of 130-150 ^{o}C for Si and ≥ 180 ^{o}C for SiC for inlet coolant temperature of 105 ^{o}C;
   - current-loop bandwidth of ≥ 20 kHz via implementation of a novel load-sharing nonlinear hybrid controller that has demonstrated the fastest control performance for parallel dc/dc converters.

Approach

- Provide Vehicle system modeling for optimum voltage selection.
- Provide vehicle system level and dc-dc and motor drive modeling to determine energy efficiency of each component and perform switching frequency optimization.
- Provide modeling of the dc-dc converter with SIC power devices.
- Provide Modeling of the dc-dc converter with Silicon power devices.
- Provide modeling and magnetic design optimization considering various magnetic materials.
- Provide modeling for the battery system.
- Design, develop and fabricate dc-dc converter for performance evaluations.

Major Accomplishments

- Developed a vehicle level simulation modeling, based on Simulink with dual battery system and the dc-dc converter for characterizing vehicle drive cycles for various vehicle system configuration and drive cycles as well as different vehicle platforms (Economy, Compact, Sedan and SUV)
- Developed an FEA parametric model and analysis techniques to characterize the magnetic and thermal behavior of the dc-dc converter critical components.
- Developed a vehicle level power and energy management. Based on such analysis the converter dynamics had to be coordinated with the vehicle and implement a power and current slew rate control.
- Developed converter level modeling to determine the operation trade off and control system.

- The dynamic and static behavior of the Si and SiC converters were validated with fabricating a test unit and validating the losses and transient responses, including the converter system control. The modeling methodology enables optimization and switching frequency operation sensitivity studies.
- Established OEM customer and industry supplier relationships to study the potential of utilizing the dual battery system for PHEV application with the bi-directional dc-dc converter.
- Demonstrated High efficiency (meeting and exceeding the target > 95 %).
- Custom Silicon packaging with 1200V NPT fast IGBT and 1200V SIC diode with high inlet and ambient temp of 105 °C.
- Has been able to demonstrate high power density of 62.5 W/in^3, exceeding the program target of (20 – 50 W/in^3).
- Demonstrated the low cost (≤ $62.5 /kW) for quantities of 10k/year.
- The dual battery system provides 14% increase in range, while
- Reducing the weight by 13% and
- Reducing the cost by 5%

Future Direction

- 8kW, dc-dc converter design and modeling.
- FEA magnetic and thermal modeling
- FMEA and DFMA analysis.
- Design and develop the custom silicon power module utilizing IGBT and SIC diode.
- Design and develop the custom magnetic components for production.
- Fabricate and test the 8kW, bi-directional power converter.
- Work with supplier for critical components development and production.
- Continue to develop OEM's involvement to implement on a target vehicle platform for evaluations.

Technical Discussion

The primary objective for 2009 tasks was to design and develop the bi-directional dc-dc converter and also to complete the vehicle system modeling to include some dynamic to determine the overall vehicle energy and power management strategy. Figure 1, depicts the PHEV utilizing dual battery system. One battery is designed and optimized for power density and will operate at some given SOC (50%-70%), with small SOC variation. While the other battery chemistry and packaging is selected and optimized for energy density and will operate a wide range of SOC, it will typically start with 100% SOC, then t is discharged down to 5% SOC. The power battery can also be replaced with Ultra capacitor as well with similar system advantages. The system benefit associated with the dual battery overcomes the deficiencies of the bidirectional dc-dc converter.

While the power battery is delivery high rms power to the PHEV system the energy battery will be providing the average power to the vehicle almost acting as a range extender. The energy battery will be design to operate up to a couple of hours, therefore the discharge rate will be C/2 or lower. The energy battery technology can be selected to enhanced energy density to reduce cost and weight, knowing that it will only discharge at C/2 or lower. The energy battery cooling system can also be designed with such a low discharge rate.

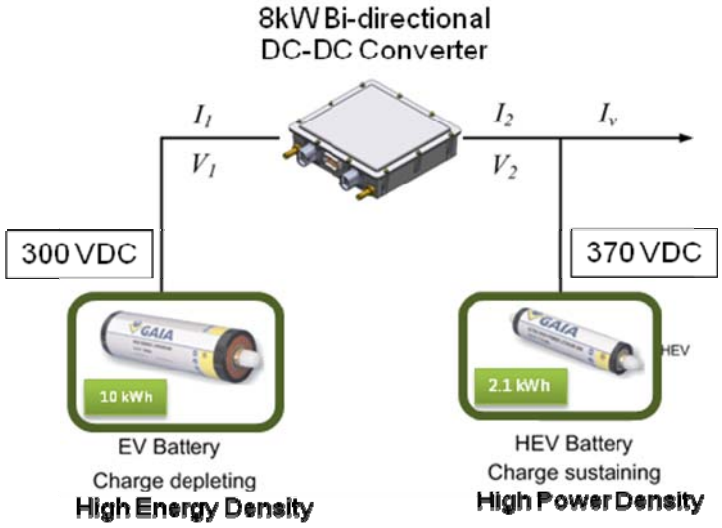

Figure 1. PHEV with dual battery system

Vehicle Control strategy and energy management.

For a PHEV operation, the battery is charged via the grid, then the vehicle operates in a charge depletion mode and uses the stored battery energy and when the battery reaches a pre-determined SOC level, then it is operated in charge sustaining mode. Depending on the battery technology and packaging, the battery should be able to deliver the required power at the charge sustaining SOC. Therefore some portion of the battery energy cannot be utilizes, due to power limitations. Typical charge sustaining operation is 20%-30% SOC level. During t such mode of operation the battery is subjected to EV discharge cycles (typically 80% DOD) and the power cycles of the hybrid operation especially at lower charge sustaining SOC. The battery cycle life is reduced and the battery design, chemistry, and packaging cost is increased.

When utilizing the dual battery the power battery is only subjected to the hybrid power cycles and the energy battery is subjected to the EV cycles only. Figure 2, shows the charge and discharge characteristic of the dual battery system, with/wo slew rate control. Ideally we want the energy battery to supply the average power and the power battery to deliver the rms with zero average power.

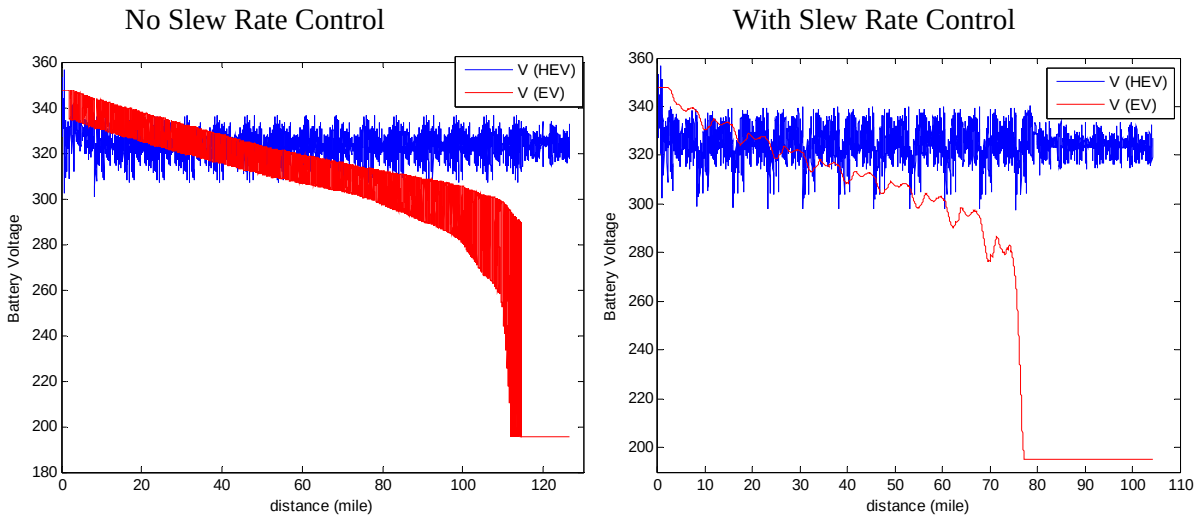

Figure 2. PHEV with dual battery control strategy

Fundamentally since we operate the energy battery at higher DOD, then we use the 10%-20% more of the stored battery energy. Meanwhile due to lower discharge requirements, the energy density can be optimized and can be increase by 20%-30%, as such reducing the weight of the battery and the cost of battery. The energy battery production cost is propositional to the material uses and if we have higher energy density (Whr/kg), then the cost will reduce proportionally. The dual system range increase, weight reduction and cost reduction is much higher compared to the deficiencies and the cost of the bi-directional dc-dc converter used.

Figure 3, shows the rms and average power for the power and energy battery when a proper vehicle energy management is used. These figures are all based on UDD Cycle.

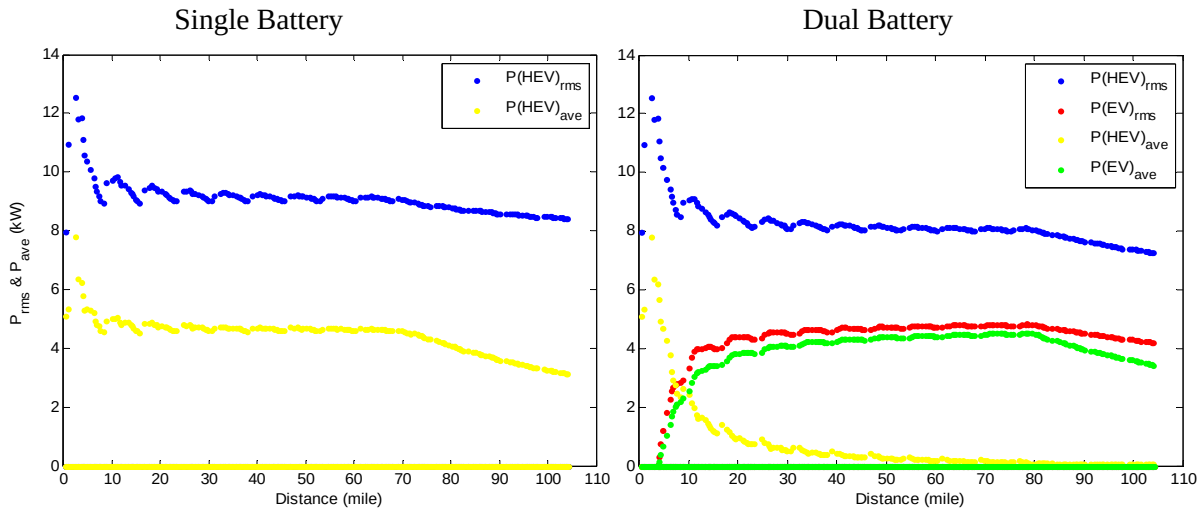

Figure 3. Battery rms and average power with optimum control strategy

The weight and cost reduction and the range increase for the dual battery system is shown in Figure 4.

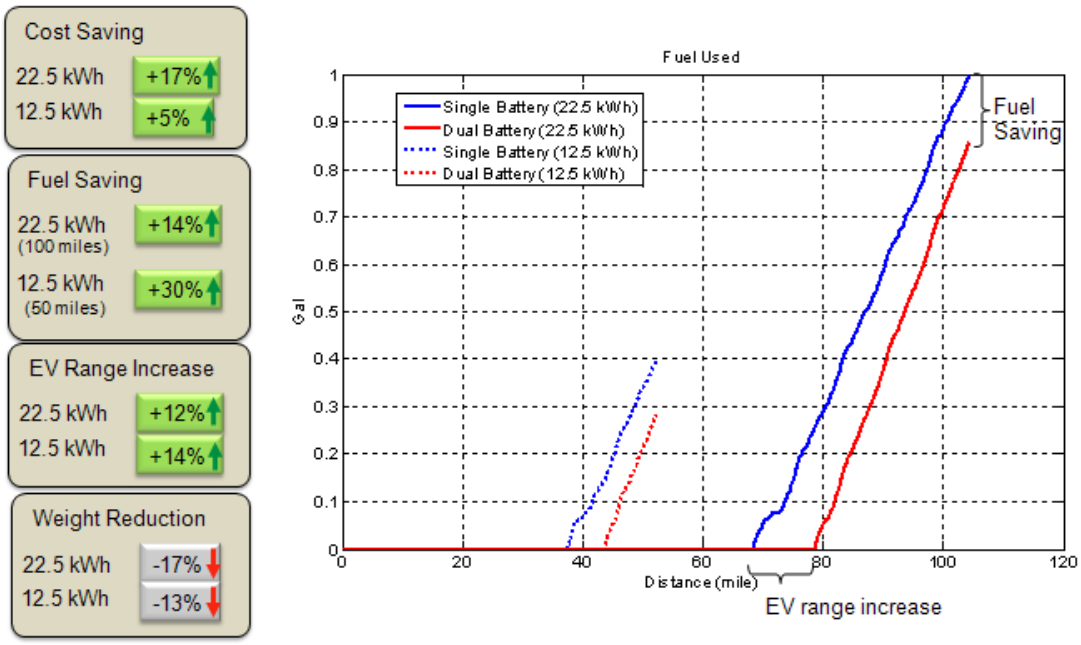

Figure 4. The cost and weight reduction and range extension of the dual battery system.

The dual battery system cost, weight and range analysis is presented in Table 1. For production of large capacity batteries such as the one used for PHEV, the cost is proportional to the material used and if the chemistry can provide higher energy density (Whr/kg), then the weight and cost is reduced almost inversely rotational to the battery energy density.

Table 1. PHEV cost and performance with dual battery and bidirectional dc-dc converter.

	Total battery Ahr	Pack Voltage	Total Capacity KwHr	%SOC used	dc-dc Eff.	Total usable capacity	Energy Density Whr/kg	Total Weight Kg	Cost (1) $/Kwhr ($/kg)	Total cost
Single pack	69	370	25.53	80%		20.4	85	300	$ 750	$ 19,148
Dual (EV Energy pack)	60	370	22.2	95%	97%	20.5	110	202	$ 580	$ 12,866
Dual (HEV Power pack)	6	370	2.22	35%		0.8	65	34	$ 981	$ 2,177
	66	370	**24.42**			21.2		236		$ 15,043
						Capacity Ratio		Weight Ratio		Cost Ratio
						104%		79%		79%
									Total Battery Saving $	$ 4,104
									Added additional BMS cost	$ 275
									Added dc-dc cost(8kW rated)	$ 552
									Total Vehicel System Saving $	$ 3,277
			EV range increase:			**12%**		**Cost Saving:**		**17%**
	Total battery Ahr	Pack Voltage	Total Capacity KwHr	DOD	dc-dc Eff.	Total usable capacity	Energy Density Whr/kg	Total Weight Kg	Cost (1) $/Kwhr ($/kg)	Total cost
Single pack	33	370	12.21	80%		9.8	85	144	$ 750	$ 9,158
Dual (EV Energy pack)	27	370	9.99	95%	97%	9.2	110	91	$ 580	$ 5,790
Dual (HEV Power pack)	6	370	2.22	35%		0.8	65	34	$ 981	$ 2,177
	33	370	12.21			10.0		125		$ 7,967
Additional Benefits:						Capacity Ratio		Weight Ratio		Cost Ratio
Lower cycle life cost.						102%		87%		87%
The enrgy battery is subjected to EV cycels (~1000), not EV+HEV									Total Battery Saving $	$ 1,191
PHEV and HEV can use common latforms with plug-n-play plug-in option.									Added additional BMS cost	$ 275
(1) The battery production cost is mainly propsotional to material/weight cost.									Added dc-dc cost(6kW rated)	$ 414
									Total Vehicel System Saving $	$ 502
			EV range increase:			**14%**		**Cost Saving:**		**5%**

Bidirectional dc-dc converter performance

The bidirectional dc-dc converter efficiency is shown in Figure 5 and the dynamic performance of the converter is shown in Figure 6.

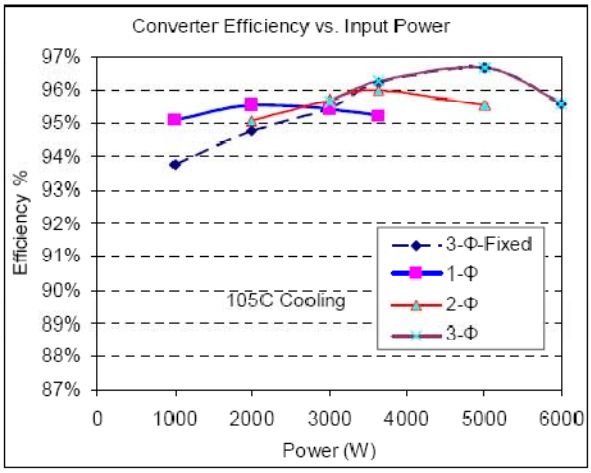

Figure 5. Bidirectional dc-dc converter efficiency

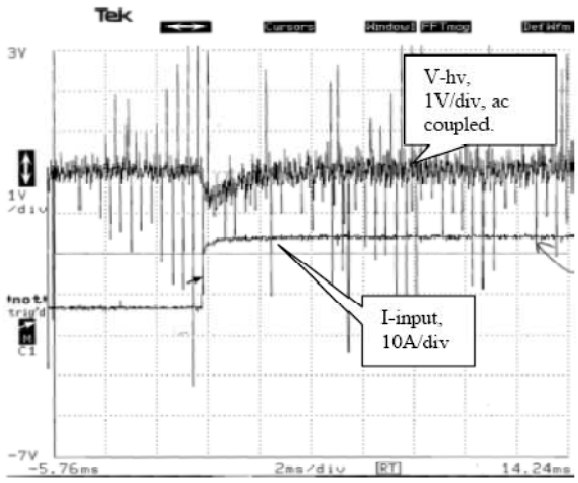

Figure 6. Bidirectional dc-dc converter response

Bidirectional dc-dc converter packaging.

The bidirectional dc-dc converter package is shown in Figure 7. The dc-dc converter performance exceeds the program targets.

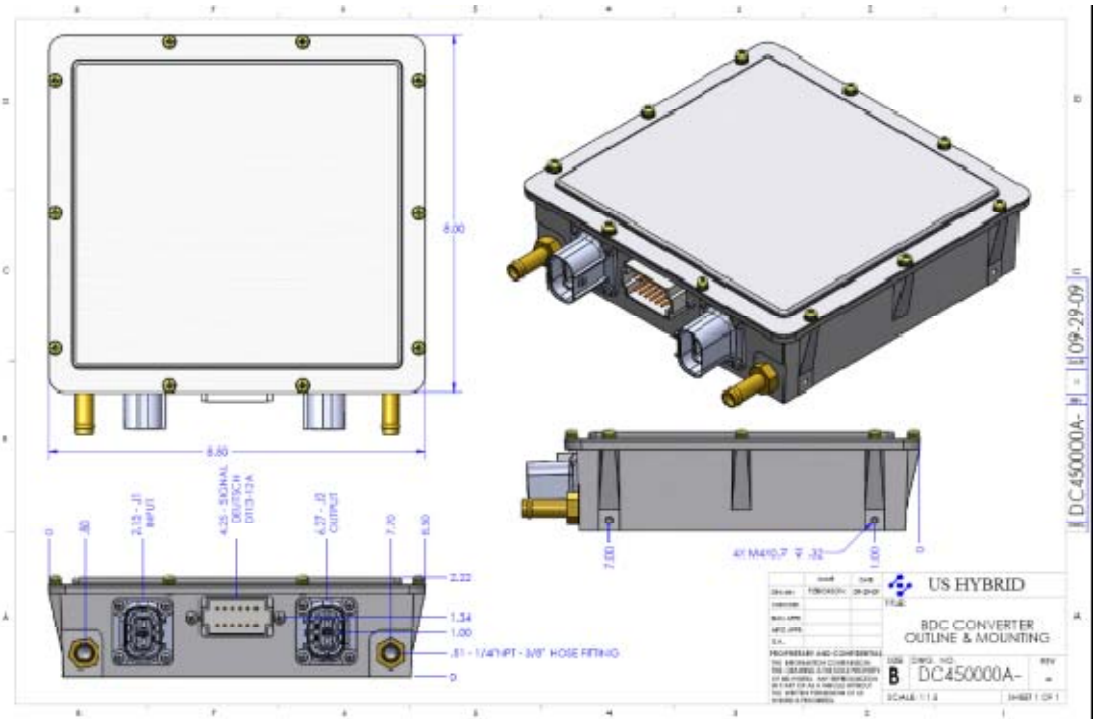

Figure 7. Bidirectional dc-dc converter packaging

Conclusions

The dual battery system for PHEV has proven to increase the range by 14%, reduce the weight by 13%, and the cost up to 17%. When using dual battery system the HEV and PHEV vehicle platforms can use more common parts and same vehicle platform and the customer has the option to choose the EV range

desired and the EV battery can be sized optimally for application requirement to reduce cost and enable the commercialization of PHEV.

The bidirectional dc-dc convert technology has met and exceeded the program requirements, following are a summary;

- Demonstrated High efficiency (meeting and exceeding the target > 95 %).
- Custom Silicon packaging with 1200V NPT fast IGBT and 1200V SIC diode with high inlet and
- ambient temp of 105 °C.
- Demonstrates high power density of 62.5 W/in3, (target 20 – 50 W/in3).
- Demonstrated the low cost (≤ $62.5 /kW) for quantities of 10k/year (target $75/kW).

Publications

Huang, Rongjun; Mazumder, Sudip K. Soft switching schemes for multiphase dc/dc converter with six-pulse modulated pulsating output Energy Conversion Congress and Exposition, 2009. ECCE. IEEE, Volume, Issue, 20-24 Sept. 2009 Page(s):853 - 860
Digital Object Identifier 10.1109/ECCE.2009.5316109

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Patents

1. In preparation and filling process

4.11 A Soft-Switching Inverter for High-Temperature Advanced Hybrid Electric Vehicle Traction Motor Drives

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Objectives

The proposed work is to develop an advanced soft-switching inverter that will eliminate the device switching loss and cut down the power loss so that the inverter can operate at high-temperature conditions while operating at high switching frequencies with small current ripple in low inductance based permanent magnet motors. The main objectives for the FY 2009 effort are

1. Characterize the soft-switching module and inverter performance at different temperatures.
2. Refine the design of the soft switching module and inverter to meet the cost target.
3. Integrate and package the soft switching module for manufacturing and in-vehicle testing.

Approach

The approaches to achieving the project goals include the following:

1. Measure soft-switching module conduction and switching losses.
2. Measure liquid-cooled soft-switching module thermal resistance.
3. Develop second generation version low-cost soft-switching module.
4. Measure inverter efficiency with inductive load and motor-dynamometer.
5. Measure inverter efficiency with calibrated calorimeter.
6. Improve design with failure mode effect analysis (FMEA).
7. Test electromagnetic interference (EMI) performance.
8. Analyze thermal performance at the module level and the chassis level.

Major Accomplishments

The key accomplishments for FY 2009 include the following:

1. Completed conduction and switching loss measurements for generation-1 modules.
2. Completed thermal resistance measurement of the liquid-cooled soft-switching module.
3. Completed efficiency measurement with inductive load and motor-dynamometer.
4. Tested inverter inside an enclosed chamber for more than 8 hours to ensure durability and reliability.
5. Demonstrated a peak efficiency exceeding 99% through calorimeter measurement.
6. Completed the second design iteration based on FMEA results.
7. Completed EMI evaluation for soft-switching inverter.
8. Three conference papers published in IEEE Applied Power Electronics Conference:

- High temperature device characterization for hybrid electric vehicle traction inverters
- Variable timing control for wide current range zero-voltage switching inverters
- An improved zero-voltage switching inverter using two coupled magnetics in one resonant pole

9. One conference paper accepted in IEEE Vehicular Power and Propulsion Conference:
   - High efficiency three-phase soft-switching inverter for electric vehicle drives
10. One journal paper accepted in IEEE Transactions on Power Electronics
   - An improved zero-voltage switching inverter using two coupled magnetics in one resonant pole

Future Direction

The future direction through FY 2010 includes the following:

1. Complete the inverter with Gen-2 soft-switching module
2. Develop Gen-3 soft-switching module
3. Demonstrate in-vehicle testing with soft-switching inverter

Technical Discussion

1. Soft-Switching Module Conduction Loss Measurement Results

Table 1 shows conduction loss of the main device Q_1-M_1 combination at different temperature conditions. Unlike a conventional IGBT device, which has a fixed voltage drop even at the current near zero, the hybrid switch voltage drop at low currents is proportional to current, and at high currents is dominated by the IGBT and increases as the current increases. The rate of increase, however, is much lower than a single IGBT only. It should also be noticed that when the temperature is above 75°C, the voltage drop at high currents tends to be lower. This is because the selected light-punch-through IGBT has a negative temperature coefficient. The current at which the IGBT dominates the conduction voltage drop is at 50 A, where the conduction voltage drop decreases as the temperature increases from 25 to 125 °C. At currents higher than 300 A, the resistive element of IGBT starts showing effect, and the negative temperature coefficient is no longer monotonic.

Table 10. Conduction loss measurement of Q_1-M_1 at different temperature conditions

Temperature (°C)	25	75	100	125
Current (A)	V_{cesat} (V)	V_{cesat} (V)	V_{cesat} (V)	V_{cesat} (V)
10	0.186	0.282	0.330	0.375
50	0.798	0.775	0.735	0.688
100	0.992	0.933	0.893	0.844
150	1.088	1.050	1.013	0.967
200	1.168	1.151	1.118	1.077
250	1.240	1.240	1.218	1.177
300	1.312	1.331	1.311	1.277
350	1.384	1.416	1.403	1.371
400	1.455	1.503	1.494	1.467

Figure 1 compares the conduction voltage drop between the novel hybrid module and a commercial one. As can be seen, at high temperature 125°C and high current 400 A, the

voltage drop of the hybrid module is 1.46 V compared to 1.67 V of the commercial one, which indicates a loss reduction of 14%.

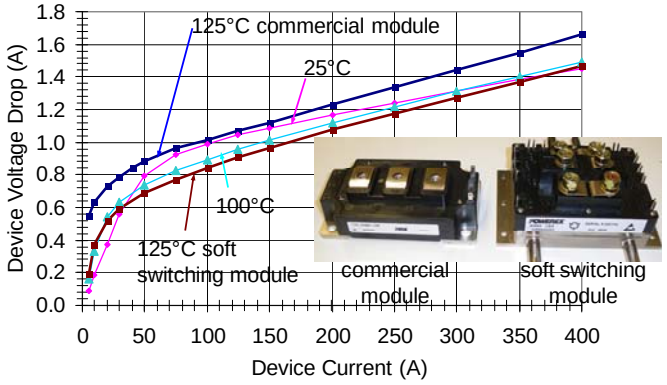


Figure 17. Conduction I-V curve comparison between designed module and commercial module.

2. Soft-Switching Module Switching Loss Measurement Results

In order to compare switching losses as a function of temperature, we performed tests at several different coolant temperatures. In each temperature condition, the switching loss was analyzed at the following current conditions: 50 A, 100 A, 150 A, 200 A, 250 A and 280 A. Figure 2 shows the switching-on waveforms with 0.1-μF resonant capacitor at 200-A load current under 25°C and 90°C conditions. For both temperatures, the bus voltage drops to zero first, and then the current rises up. There is no overlap between voltage and current for all load current and temperature cases. In addition, the bus voltage never swings back after reaching zero. So the switching-on energy is essentially zero for all test conditions.

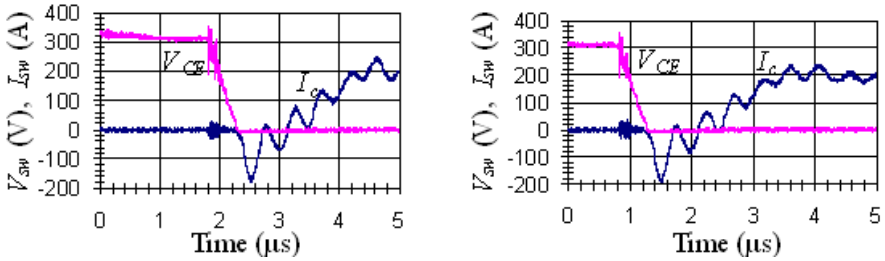


Figure 18. Switching-on waveforms with 0.1-μF resonant capacitance at: (a) 25°C and (b) 90°C.

Note that there is a significant ringing at the beginning of the falling edge of the device voltage. This is because the parasitic inductance inside the module rings with the resonant capacitors when the opposite side diode current is cut off and the diode goes through the reverse recovery process. The snappiness of the CoolMOS body diode worsens the parasitic ringing dramatically. This ringing did not occur in the scaled-down version because a larger resonant inductance was used and the slope of the reverse recovery was not as steep. The solutions to alleviating this parasitic ringing are: (1) further increase resonant inductance, (2) reduce the parasitic inductance in the module to nearly zero, and (3) use a lower voltage drop, but softer recovery diode that would prevent the CoolMOS body diode from conducting. The first method of increasing the resonant inductance has a limit because it will increase the resonant period and thus lengthen the short-pulse elimination period. The second method requires a new module layout that allows the resonant capacitor to sit directly over the chip, reducing the

parasitic inductance. It has certain degree of difficulty, but is possible to improve the situation. The third method is ultimately the best solution because it will also allow the main device freewheeling current to go through a diode with a larger die size to ensure proper cooling.

Figure 3 shows the detailed switching-off waveforms and energy with 0.1-μF resonant capacitor at 200-A load current under different temperatures. The switching-off energy increases as the temperature increases. At 25°C, the switching-off energy, E_{off} is 1.6 mJ, and it increases to 3.6 mJ at 90°C. The voltage and current waveforms look similar under the two temperature conditions. The turn-off voltage slew rate (d*v*/d*t*) is a function of the resonant capacitance. In this specific case, with 0.1-μF resonant capacitor, the measured d*v*/d*t* at 200 A current is about 1000 V/μs and is consistent with the theoretical derivation, which can be simply obtained from $I/(2C_r)$. A larger capacitor will further reduce d*v*/d*t* and switching-off energy, and vice versa. The change of temperature, however, will not affect d*v*/d*t*, but will impact the switching energy, as will be explained in the following discussions.

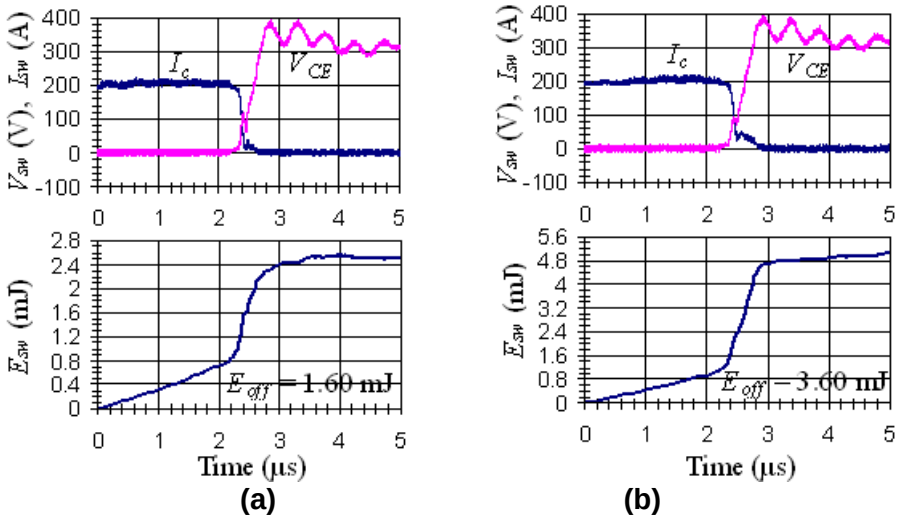


Figure 19. Switching-off waveforms with 0.1-μF resonant capacitance at different temperature conditions: (a) 25°C and (b) 90°C.

Figure 4 plots the switching energy as a function of device current and compares the results at 25°C, 50°C, and 90°C temperature conditions with 0.1-μF resonant capacitance. All the dots were directly from the measurement. The smooth curves were curve-fitted to the following format.

$$E_{on} = hI^k$$
$$E_{off} = mI^k \quad \textbf{(1)}$$

Since switching-on energy is zero for all temperature cases, *h* and *k* are all zero here. Switching-off energy increases with temperature rise. The m and k parameters are found as follows.

At 25°C, *h* = 0.000061, *k* = 1.9522
At 50°C, *h* = 0.000204, *k* = 1.777
At 90°C, *h* = 0.000777, *k* = 1.60

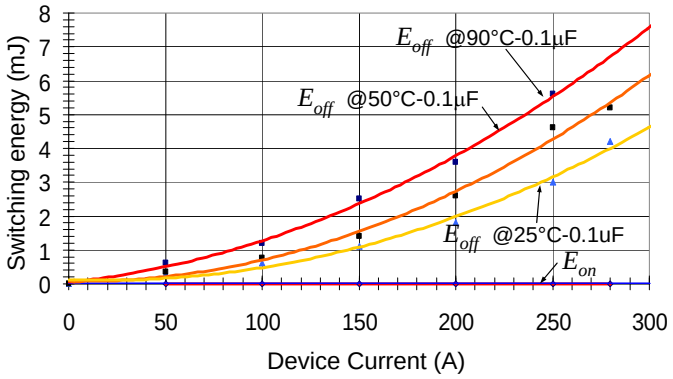


Figure 20. Switching energy with 0.1μF resonant capacitance at different temperatures.

3. Inverter Power Loss Measurement and Efficiency Prediction Results

Figure 5 shows the power loss as a function of the output kVA under different line frequencies and different temperatures: (a) 25°C and (b) 90°C. The figures clearly indicate that the higher line frequency, which represents higher motor speed, the lower power loss. The reason is the voltage level, and thus the power factor, is higher at a higher line frequency. To achieve the same kVA, the case with higher frequency requires less current or produces less power loss.

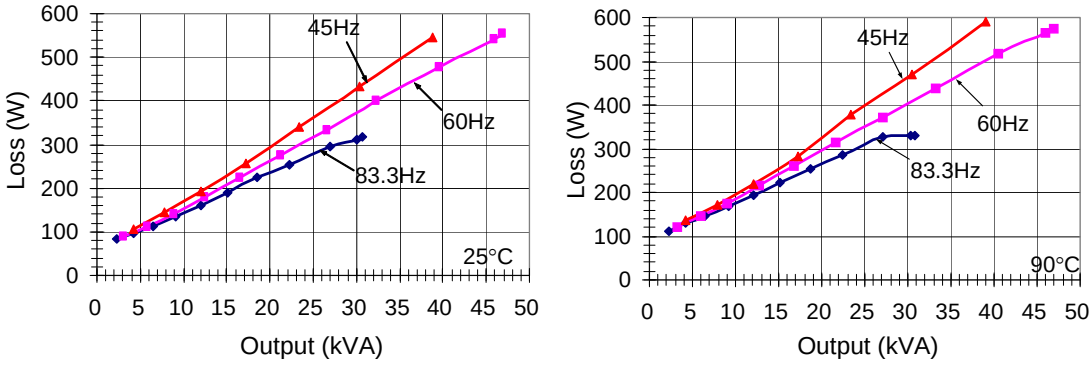


Figure 21. Power loss as a function of the output kVA under different line frequencies and different temperatures: (a) 25°C and (b) 90°C.

Figure 6 shows the power loss as a function of the output kVA under different temperatures and different line frequencies: (a) 45 Hz and (b) 83.3 Hz. The general trend is the higher temperature, the higher power loss. This indicates that the turn-off loss increases more than the conduction loss decreases. At higher frequency cases, when the modulation index saturates, the loss tends to flatten out, especially at high temperatures, and the loss is less impacted by the temperature. This is because the switching loss is no longer dominating.

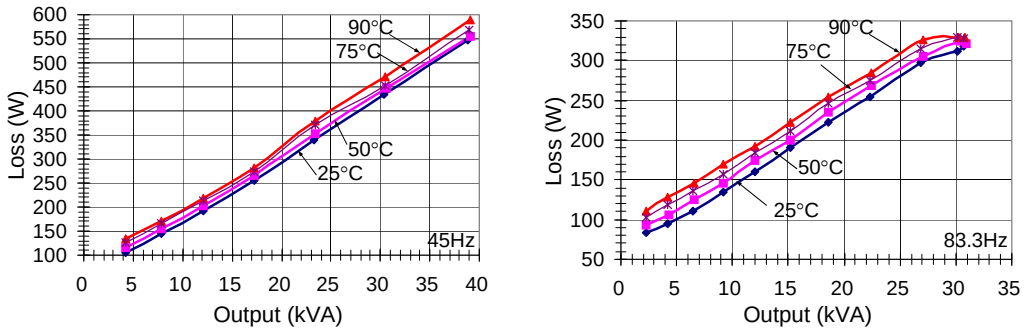


Figure 22. shows the power loss as a function of the output kVA under different temperatures and different line frequencies: (a) 45 Hz and (c) 83.3 Hz.

Figure 7 shows the projected efficiency based on the inductive load measured loss results at 83.3-Hz output line frequency at different temperatures. The power factor is assumed to be unity in this case. It is noted that at the light load condition, the efficiency decrease with increasing temperature is more obvious than that at the heavy load condition. The reason is that at light loads, the MOSFET shares more current, and with a positive temperature coefficient of the Rdson, the efficiency suffers. However, at heavy loads, the LPT IGBT shares more current, and with the negative temperature coefficient, the decrease in efficiency with temperature is not as severe. The peak efficiency approaches 99%.

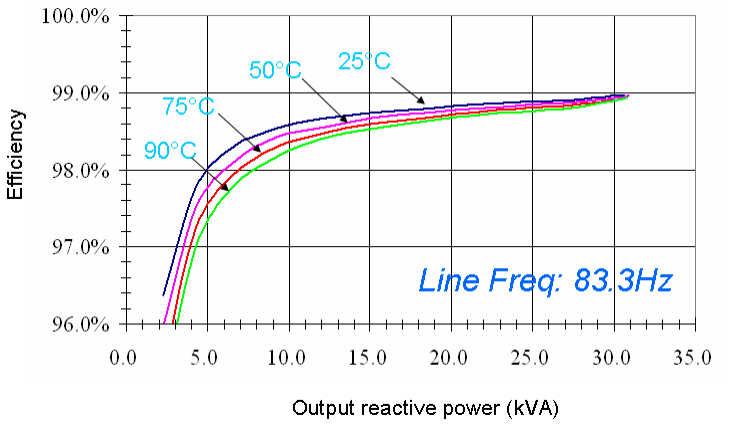


Figure 23. Efficiency measurement at 83.3-Hz line frequency and different temperatures.

To compare the efficiency as a function of frequency, the above results are rearranged to compare the projected efficiency at different frequencies under the same temperature condition. Figure 8 shows the projected efficiencies for different output line frequencies at 90°C. The power factor in this case is assumed to be 0.83, which is the same as what has been tested for the motor drive cases. As can be seen, at the same output power point, the efficiency is higher at a higher output line frequency. That can be translated into higher speed with higher efficiency, which was proven by later motor tests.

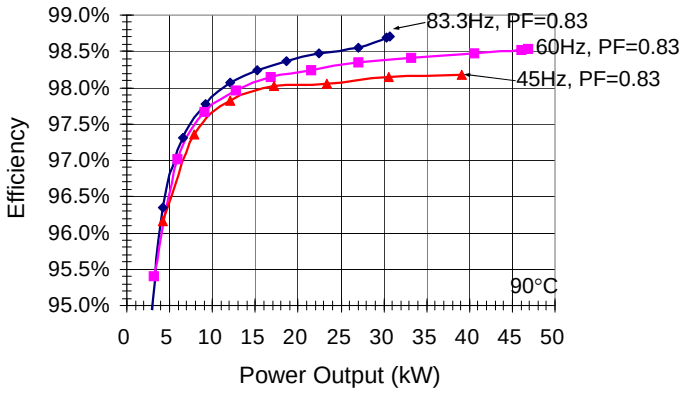


Figure 24. Efficiency comparison at 90°C and different line frequency conditions.

4. Inverter Efficiency Test under Motor Load

The motor test setup is the same as that of inductive load except that the load is a motor-dynamometer. We tested the motor at different speed conditions, 1000rpm, 1500rpm and 2000rpm with different output current values, 30A, 40A and 50A at different temperatures, 25°C, 50°C and 75°C. The dynamometer was adjusted to provide the load torque according to motor output current and speed conditions.

Table 2 shows the tested inverter efficiency at different speeds and different output currents at different temperatures reflected to power factor 0.83. Due to the limited power supply capacity in the lab, we can only test lower power regions. The high power test will be conducted in the next performance period at Azure Dynamics. As can be seen from Table 2, at lower output power, the low-temperature efficiency is slightly higher than the high-temperature one. At higher output power, the high-temperature efficiency catches up and may surpass low temperature one. At higher motor speed and thus higher output frequency, the inverter efficiency is higher than lower speed conditions.

Table 11. Efficiency measurement with motor test at different temperatures.

1000rpm (33.3Hz)	75°C		50°C		25°C	
30A	98.1%	9.8kVA	98.2%	9.8kVA	98.3%	9.7kVA
40A	98.2%	14.0kVA	98.3%	14.0kVA	98.4%	14.0kVA
50A	98.3%	18.3kVA	98.3%	18.3kVA	98.4%	18.3kVA

1500rpm (50Hz)	75°C		50°C		25°C	
30A	98.3%	12.1kVA	98.5%	12.1kVA	98.6%	12.2kVA
40A	98.6%	17.4kVA	98.6%	17.4kVA	98.7%	17.4kVA

2000rpm (66.6Hz)	75°C		50°C		25°C	
30A	98.8%	13.7kVA	98.9%	13.7kVA	98.9%	13.7kVA

Figure 9 shows the efficiency profile of the advanced soft-switching inverter under motor-dynamometer test at 25°C coolant condition. The motor was tested with different modulation indexes until the power supply reached its limit. For this plot, the measurements at 0.4 power factor were used to project the efficiency at 0.83 power factor. The measurement results show a consistent trend that the higher power factor, the higher efficiency and the higher speed, the higher efficiency. At higher speeds, the motor terminal voltage is also higher, and for the same

current, the loss is less. The efficiency profile shows the inverter efficiency is close to 99% even when the speed is still below its nominal 2500 rpm. This projected result is consistent with what has been tested using the calorimeter at 2800 rpm, at which the efficiency is 99.1%. Detailed results will be shown in the next quarterly report.

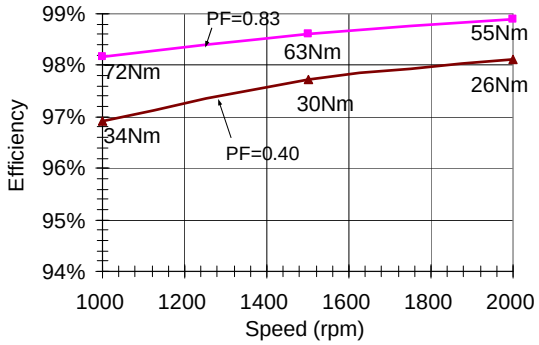


Figure 25. Efficiency profile of the advanced soft-switching inverter under motor-dynamometer test.

Table 3 shows the efficiency comparison between inductive load test and motor test. The efficiency with inductive load is projected from a power factor of 0.83. At the same output power, the motor test efficiency is higher than the pure inductive load test efficiency. The reason is during motor-dynamometer test, the current is mainly conducting through MOSFET and IGBT channels, while in inductive load test, the duty cycle of the anti-parallel diodes increases, and the efficiency suffers slightly. Previous inductive load tests show that at 83.3Hz (30.6kVA), the efficiency is 98.8%; and at 60Hz (46.8kVA), the efficiency is 98.6%. Therefore, the peak efficiency at higher motor load can be expected to exceed 99%.

The above measurement using our power meter becomes inaccurate when the power is further increased because the instrumentation is not well calibrated at these higher power levels. Table 4 lists the power meter readings at 30-minute intervals for the 27-kW, 1600-rpm machine output condition. Such a low-speed machine tends to draw larger current than the same power level case with a high-speed machine. In Table 4, the inverter efficiency reading at 4:00pm was exceeding 100%. This clearly indicates that power meter reading is inaccurate and should not be used for the efficiency index. Its voltage and current readings, however, can be used as the reference for the power level.

Table 12. Efficiency comparison between inductive load and motor test at different temperatures.

	75°C		50°C		25°C	
50Hz/motor	98.3%	12.1kVA	98.5%	12.1kVA	98.6%	12.2kVA
45Hz/inductor	97.9%	12.1kVA	98.0%	12.1kVA	98.1%	12.1kVA

	75°C		50°C		25°C	
66.6Hz/motor	98.8%	13.7kVA	98.9%	13.7kVA	98.9%	13.7kVA
60Hz/inductor	98.1%	13.7kVA	98.2%	13.7kVA	98.3%	13.7kVA

Table 13. Readings from power meter at 1600 rpm, 27 kW condition

Time	V_{dc} (V)	I_{dc} (A)	P_{inv} (kW)	I_a (A)	I_b (A)	I_c (A)	P_{inv} (kW)	η_{inv}
3:00pm	324	84.92	27.54	91.00	90.80	90.50	26.85	97.5%

3:30pm	325	83.55	27.12	91.00	90.00	90.00	26.55	97.9%
4:00pm	322	82.90	26.69	89.70	89.50	89.10	26.90	100.8%

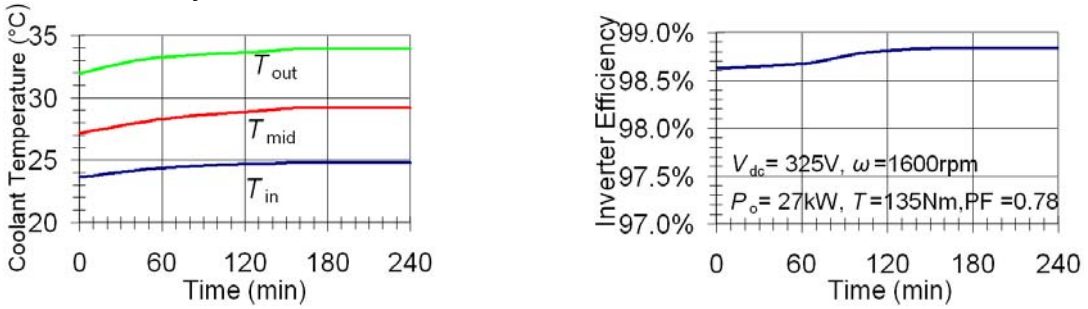
5. Inverter Efficiency Test with Calibrated Calorimeter.

To more accurately measure efficiency, a differential calorimeter has been constructed and calibrated. Figure 10 shows photographs of the differential calorimeter setup. Figure 10(a) shows the small reference chamber in foreground and the main chamber partially open in the back. Figure 10(b) shows the main chamber with the cover removed to see the coolant inlet and outlet. The DC bus and AC output cables passing through the chamber wall can also be seen. A stirring fan, seen at the top of the picture, is to ensure uniform temperature distribution inside the chamber.

(a) (b)

Figure 26. Photographs showing (a) differential-chamber based calorimeter with flow meter box in foreground and inverter chamber partially open in back; (b) main chamber cover removed for the view of coolant inlet and outlet.

The calorimeter test was performed for more than five hours to ensure that the thermal condition reached its steady state for each test point. Figure 11 shows the coolant temperatures and the measured inverter efficiency at 27 kW. Different speeds tend to have different power factor were tested, and the results were indicated in the figures ????. The test was conducted with an MG set with machine rated 90 kW and 1600 rpm. The test was conducted at a higher power output, 27 kW, which is about 50% of the peak power. The power factor is 0.78, and the steady-state efficiency is 98.8%.



(a) (b)

Figure 27: Calorimeter measurement at 27kW: (a) coolant temperatures, (b) inverter efficiency.

6. Improve Design with Failure Mode Effect Analysis

The Failure Mode Effects Analysis (FMEA) is a tool commonly used by the automotive industry but was developed from techniques started in the high reliability aerospace area. Its purpose is to identify potential problems and to insure that adequate consideration has been given to each. The possible consequences of a failure are identified and severity rankings are given to each issue. Our goal was to complete a quick FMEA on the power stage alone. A production design would have each piece of the overall system analyzed in detail, but in the interest of getting useful feedback while still in the design phase only the aspects of the inverter that would not be present in a conventional six-switch setup were analyzed. The following analysis shows the currents and voltages for a successful and two failed commutations. The failed commutations can be categorized in to two cases.

1. Q_{x1} opening after D_2 stops conduction, when the resonant current has reached its peak.
2. Q_{x1} opening before D_2 stops conduction, i.e. during the linear phase of the resonant current ramp-up.

Case 1 results in the worst-case peak current for D_{x5}, however the current decays quickly. Case 2 is different. The worst-case diode current is not as high as for case 1, however, the current decays very slowly (as the voltage across the coupled inductor is zero). This suggests that D_{x5} and D_{x6} cannot be 5-A diodes and possibly not even 50-A. Figure 12 shows the simulation diagram using MicroCap Ver. 9.

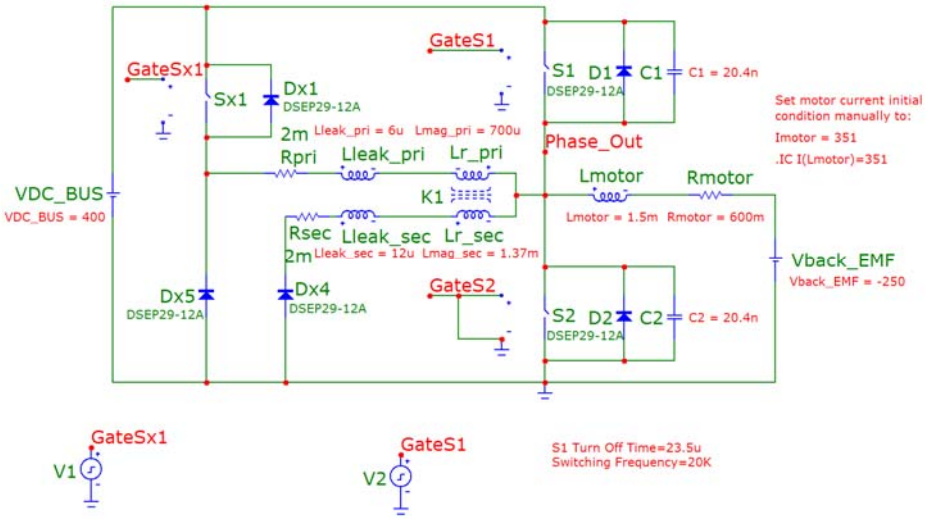


Figure 28. Simulation diagram using MicroCap.

Figure 13 shows the simulated resonant inductor voltage and current waveforms under normal operation. The top two traces are the gate signals for main (V_{GATES1}) and auxiliary ($V_{GATESX1}$) switches. The middle five traces are the motor line current (I_{LMOTOR}), the primary side resonant inductor current (I_{LEAK_PRI}), the secondary side resonant inductor current (I_{LLEAK_SEC}), the clamping diode current (I_{Dx5}), and the total resonant current (I_{LEAK_PRI}+I_{LLEAK_SEC}). The bottom two traces are output phase voltage (V_{PHASE_OUT}) and the voltage across the secondary side of the resonant inductor (V_{LLEAK_sec} + V_{LLEAK_sec}). Notice that the clamping diode current I_{Dx5} in the middle graph sees very little current during the normal commutation condition.

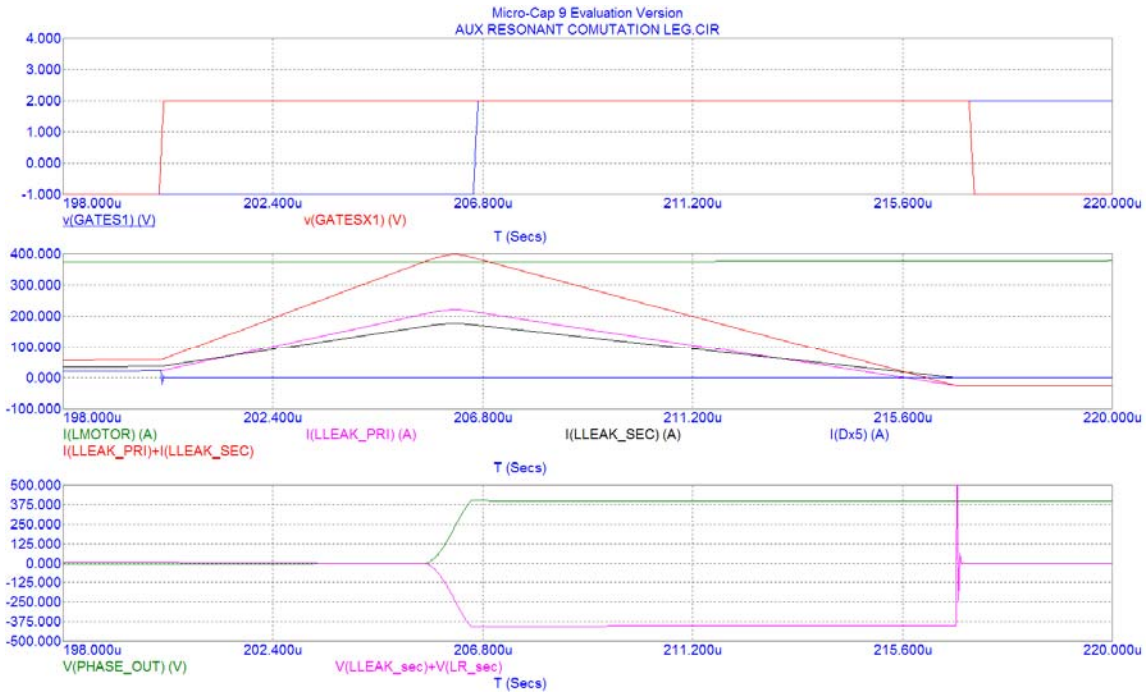


Figure 29. Resonant inductor voltage and current under normal operation.

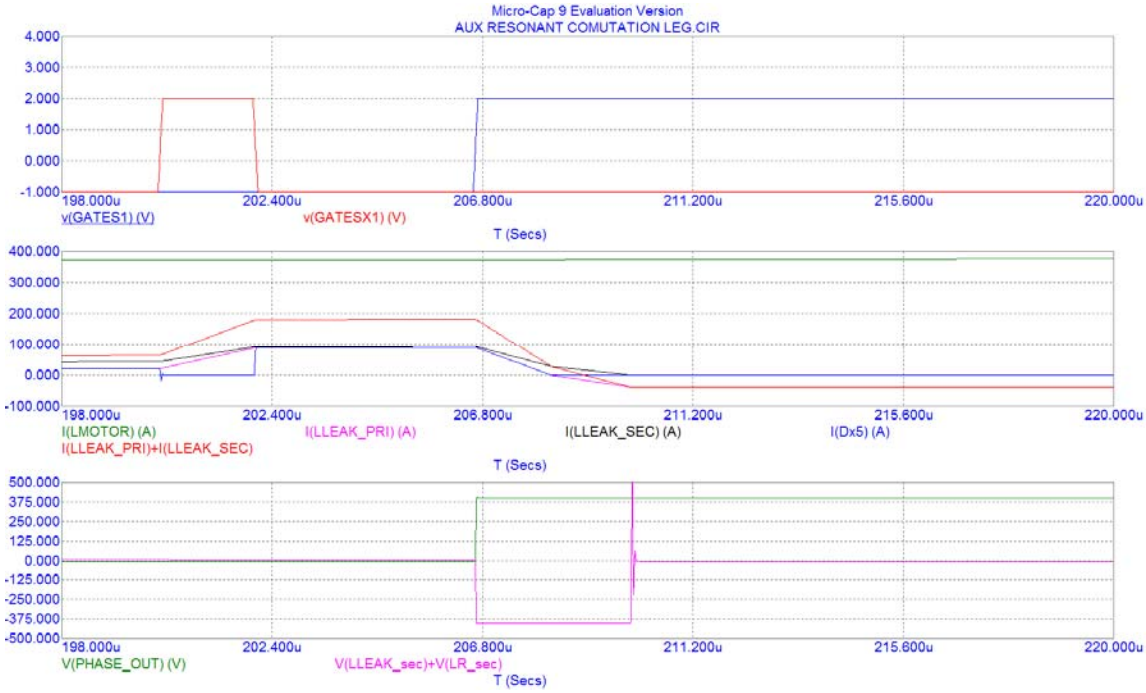


Figure 30. Simulated resonant inductor voltages and currents under communication failure.

Figure 14 shows the simulated results under the failure of communication between the inverter interface and DSP controller (Case 2 above). At time 202 μs, the auxiliary switch gate signal is interrupted due to loss of communication. In this case, the resonant current is interrupted, and the clamping diode current I_{Dx5} is equal to the primary resonant current until the main switch gate is turned on. A peak current of 90 A flows through the clamping diode for

about 3 μs. This suggests that a 5-A rated diode is inadequate to handle such a failure mode condition.

A communication failure can also cause the interruption of the main gate signal. Figure 15 shows the simulation result with loss of communication that interrupts the auxiliary and main gate signals. In this case, the clamping diode will conduct a high current for a long period, which is clearly exceeding its 5-A capability. Therefore, this FMEA study suggests that a much higher rated diode is required for the clamping diode.

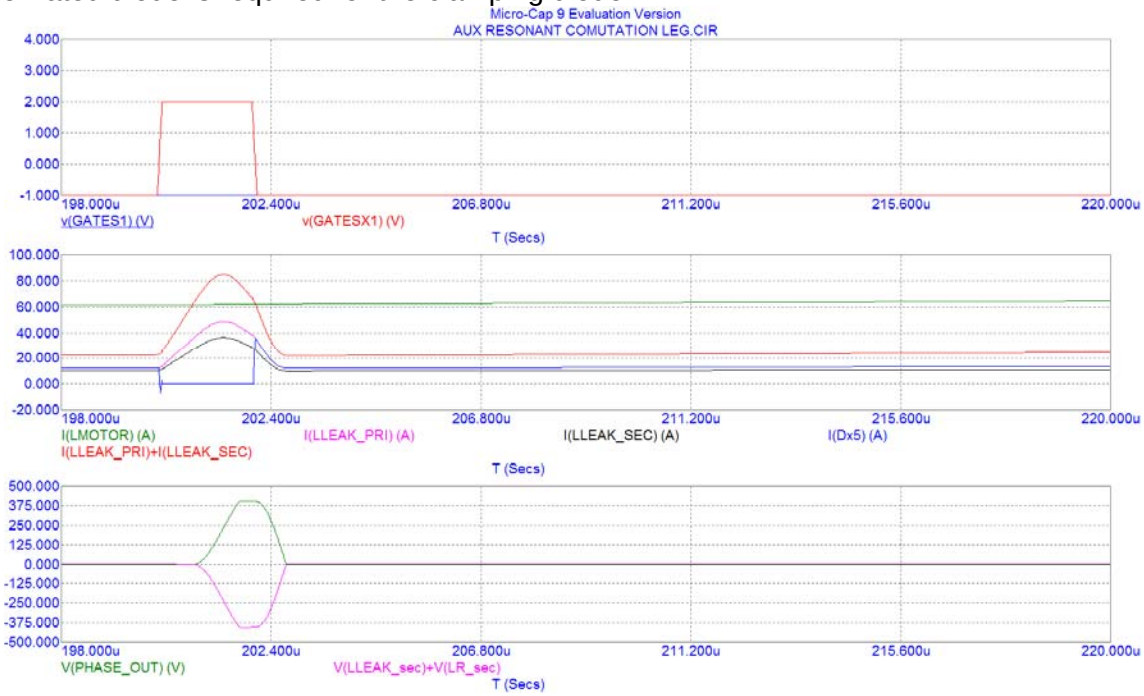


Figure 31. Simulation result with loss of communication that interrupts the auxiliary and main gate signals.

7. Test EMI Performance

Figure 16 shows the schematic diagram of EMI measurement setup that includes a set of line impedance separation networks (LISN), the inverter under test, and the load. The measurement instrument needs to have frequency-domain analysis capability. Both dc source side and ac load side EMI and differential-mode (DM) and common mode (CM) performances are measured to see the difference of EMI performance between hard-and soft-switching inverters. The source side current sensing comes from two LISN outputs, and the load side current sensing comes from a Rogowski probe that encloses all three cables that go into the load. The DM output EMI is not measured because it is the inherent load current that should not be different between hard- and soft-switching inverter.

Figure 17 compares DM noise at dc source side in the high-frequency region, from 0 to 50 MHz. The bottom traces of hard-switching and soft-switching results represent the measured EMI on the two differential lines, or I_{dc+} and I_{dc-}. By subtracting these two lines from each other, the total noise is the DM noise, which is shown in the top trace. Since the scale is much above the base switching frequency of 10 kHz, the soft-switching inverter is shown to be more effective at diode reverse recovery and parasitic related EMI noise reduction. By looking at the top traces of hard- and soft-switching inverter noises, the soft-switching inverter apparently lowers the EMI noise by 10 to 20 dB across the entire frequency range. The main noise reduction regions are in between 2 and 8 MHz and between 18 and 27 MHz, where 20-dB reduction by soft switching is clearly identifiable. There are two possible noises that tend to be pronounced in the hard-switching inverter: (1) diode reverse recovery related EMI noise and (2) layout and parasitic component related EMI noises. The dc link capacitor needs to have very low equivalent series resistance (ESR) and equivalent series inductance (ESL) to effectively suppress these high frequency noises.

In terms of which noise source is located in which region is still unknown, but the soft switching has demonstrated a significant EMI reduction advantage on the dc source side.

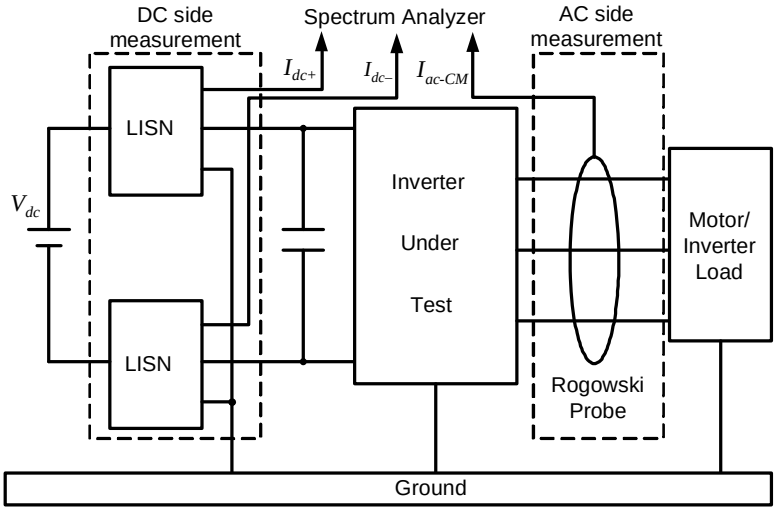


Figure 32. Schematic Diagram of EMI Measurement Setup.

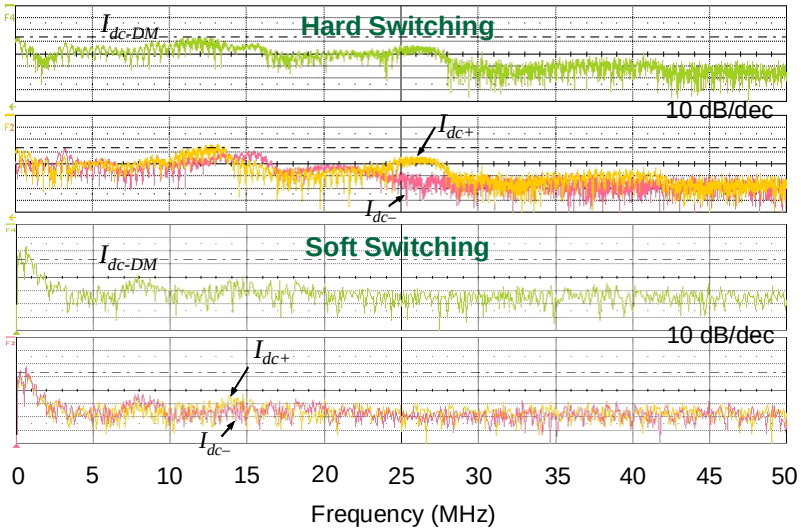


Figure 33. Measured High Frequency Range DM Noise at DC Side.

Figure 18 compares the CM noise at the dc source side in the high-frequency region. The bottom traces of the hard-switching and soft-switching results represent the measured EMI on the two differential lines, or I_{dc+} and I_{dc-}. By adding these two lines together, the total noise is the CM noise, which is shown by the top trace. Similar to the DM noise reduction, the main noise reduction regions are spread around certain frequencies. In this case, significant noise reduction is shown between 2 and 7 MHz, between 9 and 15 MHz, and between 17 and 28 MHz regions, where more than 10-dB reduction by soft switching is clearly identifiable. Again, in terms of which noise source is present in which region is still unknown, but soft switching has demonstrated significant CM EMI reduction advantage on the dc source side.

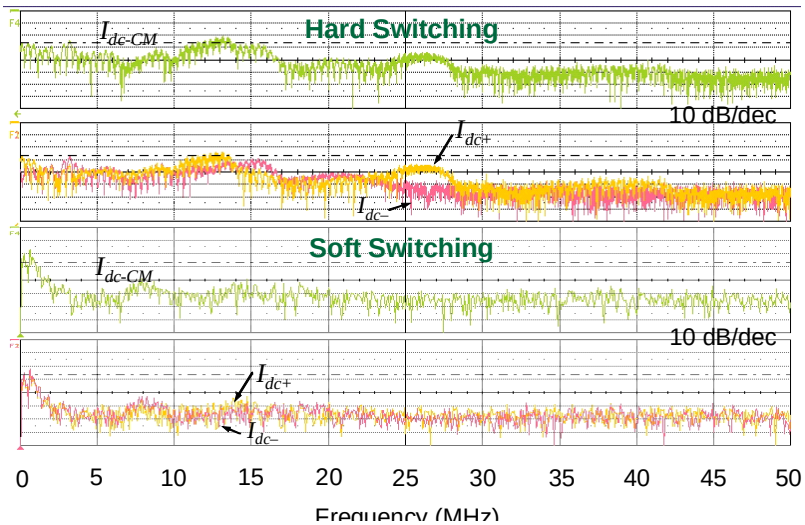


Figure 34: Measured High Frequency Range CM Noise at DC Side.

Figure 19 compares the ac load-side EMI performance of the hard- and soft-switching inverter in the high-frequency region. Since the low-frequency component is related to the load current, there is not a significant difference between hard and soft switching. At high frequencies, however, the soft-switching inverter demonstrates significant EMI noise reduction. The main noise reduction regions are between 2 and 7 MHz and 13 and 18 MHz, in which more than 10-dB reduction is realized.

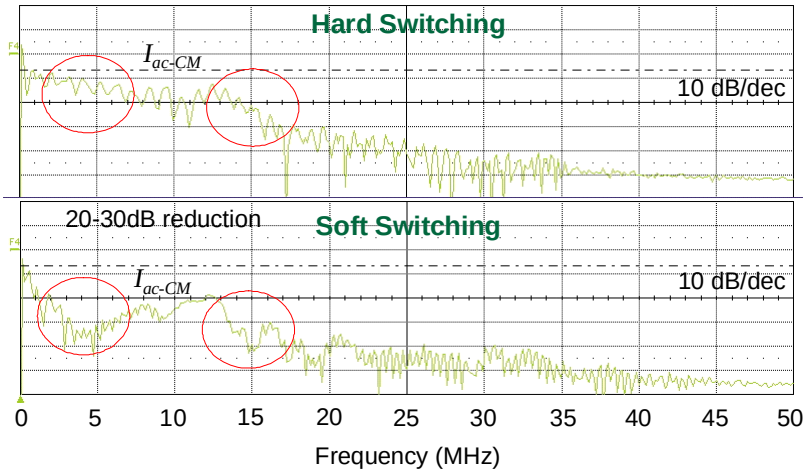


Figure 35: Measured High Frequency Range CM Noise at AC Side.

8. Summary

In this performance period, the first-generation, variable timing, soft-switching inverter based on a newly developed integrated liquid-cooled soft-switching module has been built and extensively tested. The module characteristics of conduction, switching, and thermal resistance were measured to predict efficiency and junction temperatures first. The efficiency of the three-phase soft-switching inverter was then measured with inductive load and motor-dynamometer. Peak efficiency of 99% was found with power meter measurement, but the accuracy of the power meter became doubtful at higher power outputs. Therefore, the inverter was then tested with a calibrated differential calorimeter for long-time (8 hours) operation. The calorimeter inlet and outlet temperature increases were then used to find the inverter loss for efficiency

calculation. The results of calorimeter tests show efficiencies between 98.5% and 99% for loads between 12 kW and 27 kW. As compared to the existing 55-kW hard-switching inverter, the efficiency improvement was between 1.5% and 2.5% depending on the torque and speed condition.

In addition to efficiency measurements, the team also performed extensive FMEA analyses and measured EMI for CISPR-25 compliance. The FMEA results suggest that the auxiliary diodes that are not carrying steady-state current need to be sized large enough to avoid catastrophic device failure during controller malfunction or loss of communication between the DSP controller and the power circuit board. The EMI measurement results show significant high frequency EMI reduction with the soft-switching inverter. Overall, the first-generation soft-switching inverter was successfully developed to demonstrate superior performance in efficiency and EMI. Future work will be in further reduction of parasitic components with new package designs and integration of auxiliary circuit components for cost reduction.

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5. Systems Research and Technology Development

5.1 Benchmarking of Competitive Technologies

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Objectives

- Determine the status of nondomestic hybrid electric vehicle (HEV) technologies through assessment of design, packaging, fabrication, and performance during comprehensive evaluations.
  - — Compare results with other HEV technologies.
  - — Distribute findings in open literature.
- Support FreedomCAR program planning and assist in guiding research efforts.
  - — Confirm validity of the program technology targets.
  - — Provide insight for program direction.
- Produce a technical basis that aids in modeling/designing.
- Foster collaborations with Electrical and Electronics Technical Team (EETT) and Vehicle Systems Analysis Technical Team (VSATT).
  - — Identify unique permanent magnet (PM) synchronous motor/inverter/converter/drive-train technologies.
  - — Ascertain what additional testing is needed to support research and development.

Approach

- Choose vehicle subsystem.
  - — Evaluate potential benchmarking value of various HEVs.
  - — Consult with original equipment manufacturers (OEMs) as to which system is most beneficial.
- Tear down power control unit (PCU) and electronically controlled continuously variable transmission (ECVT).
  - — Determine volume, weight, specific power, and power density.
  - — Assess design and packaging improvements.
- Prepare components for experimental evaluation.
  - — Develop interface and control algorithm.
  - — Design and fabricate hardware necessary to conduct tests.
  - — Instrument subsystems with measurement devices.
- Evaluate hybrid subsystems.
  - — Determine peak and continuous operation capabilities.
  - — Evaluate efficiencies of subsystems.
  - — Analyze thermal data to determine assorted characteristics.

Major Accomplishments

- Conducted end-of-life (EOL) assessments to find and explore any detrimental impacts sustained over the life of a 2004 Toyota Prius.
- Compared observations from EOL assessments to those made during original benchmarking of the 2004 Prius.
- Determined that subcomponents of the 2004 Toyota Prius sustained no substantially negative impacts.
- Selected the 2010 Toyota Prius (Generation 3) hybrid system to be benchmarked for the latter portion of FY 2009 and FY 2010.
- Conducted preliminary design/packaging studies of the 2010 Prius PCU and ECVT, wherein significant differences with respect to the 2004 Toyota Prius were noted.
- Assessed mass and volume of various PCU/ECVT components.
- Communicated effectively with EETT and VSATT to aid in discerning project direction, test plan, and test results.

Future Direction

- Discussions will be conducted with EETT and VSATT to determine the appropriate system to study in the latter part of FY 2010.
- Approaches similar to that of previous benchmarking studies will be taken while working to suit the universal need for standardized testing conditions.

Technical Discussion

Benchmarking efforts made in FY 2009 can be categorized under two main groupings. Most of the FY 2009 effort was devoted to conducting EOL assessments of the 2004 Toyota Prius. Secondary efforts were made in the latter portion of FY 2009 to initiate benchmarking assessments of the 2010 Toyota Prius (Generation 3)

End-of-Life Assessments

To ascertain the impacts of lifelong operation upon the subcomponents of the 2004 Toyota Prius, used vehicle components from a properly serviced vehicle were needed. Studies in which data are collected from various in-service company fleet vehicles are conducted by Idaho National Laboratory (INL) and Electric Transportation Applications (ETA). The vehicles are operated for 160,000 miles before they are removed from the fleet and are serviced per OEM recommendations. Therefore, collaboration was established through James Francfort at INL to obtain the 2004 Toyota Prius subcomponents and subsequent data from vehicles for which this evaluation process had been completed. The PCU and transaxle were obtained to conduct comprehensive assessments of the subcomponents, allowing observation of any degradation or signs suggestive of deviations from normal operation.

PCU components that were studied included the primary capacitor, power electronics (PEs), cold plate, thermal paste, and heat exchanger. Shown in Fig. 1 are the thermocouple locations used during capacitor tests, wherein “X” and “Y” thermocouples were placed on the casing of the capacitor above the main capacitor section of the module. Ripple current tests were conducted on the EOL module as well as on an unused module. (Fig. 2 shows the results of these tests.) As ripple current was applied to the capacitor, the temperature response was monitored over extended periods. The modules were located inside an environmental chamber as the ambient temperature was regulated to maintain consistency throughout the tests. At the beginning of the tests, 50 amps (A) root mean square (RMS) of sinusoidal current was applied to the capacitor for roughly 30 minutes. Thereafter, the current was increased by 50 A for each 30-minute interval, with a final RMS current of 200 A. The traces for the EOL module are shown in colors of cyan and red, which reflect the “X” and “Y” thermocouples, respectively. Note that data from two separate tests are combined on this graph, and the current was not adjusted at exactly 1,800-second

intervals. Nonetheless, it is observable that the unused module produces slightly more heat than the EOL module. An LCR meter was used to measure the modules' capacitances over a wide range of frequencies and at various temperatures. Results measured at room temperature are shown in Fig. 3, wherein the capacitance is nearly identical up to 5,000 Hz, and thereafter, the EOL module appears to have a greater capacitance. However, very small inductances can greatly impact capacitor measurements at high frequencies, and the discrepancies could be an artifact from slight differences in the test setup.

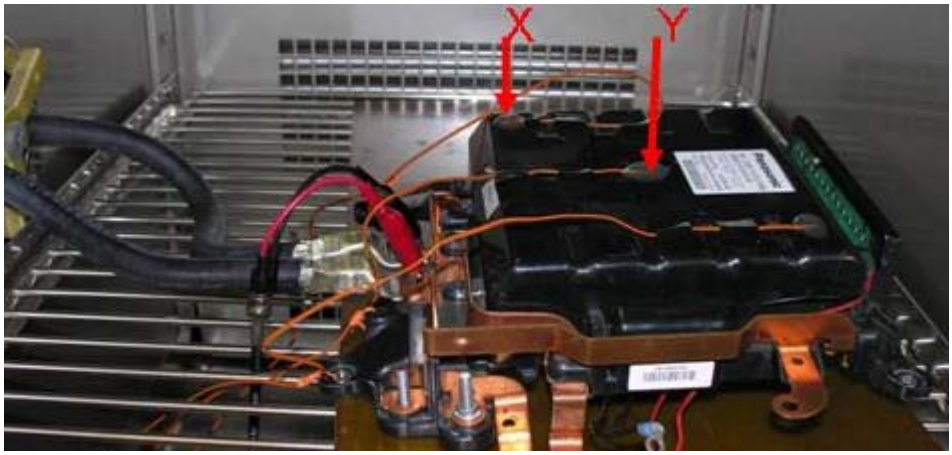

Fig. 1. Thermocouple locations on capacitor.

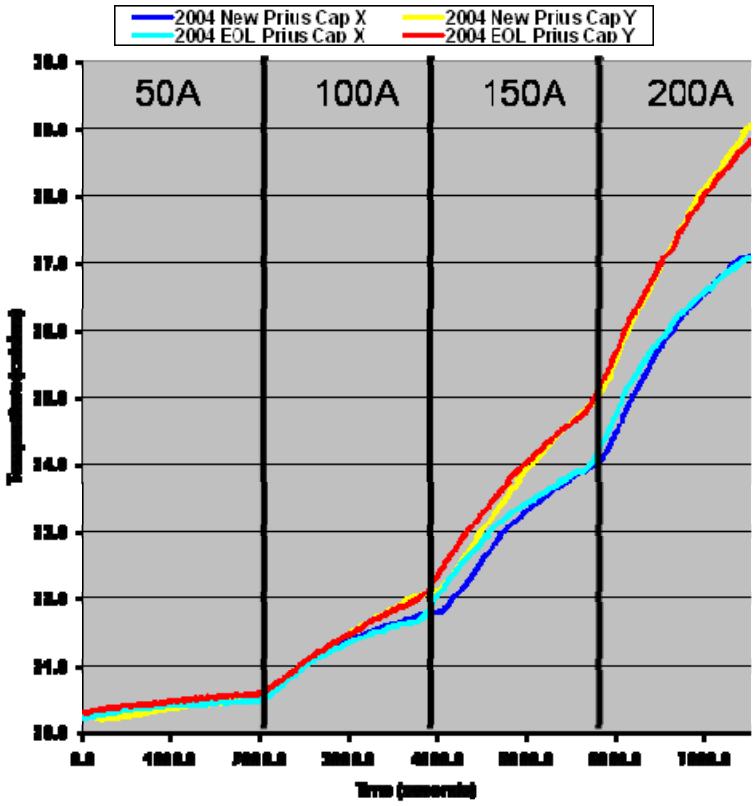

Fig. 2. Ripple current capacitor test results.

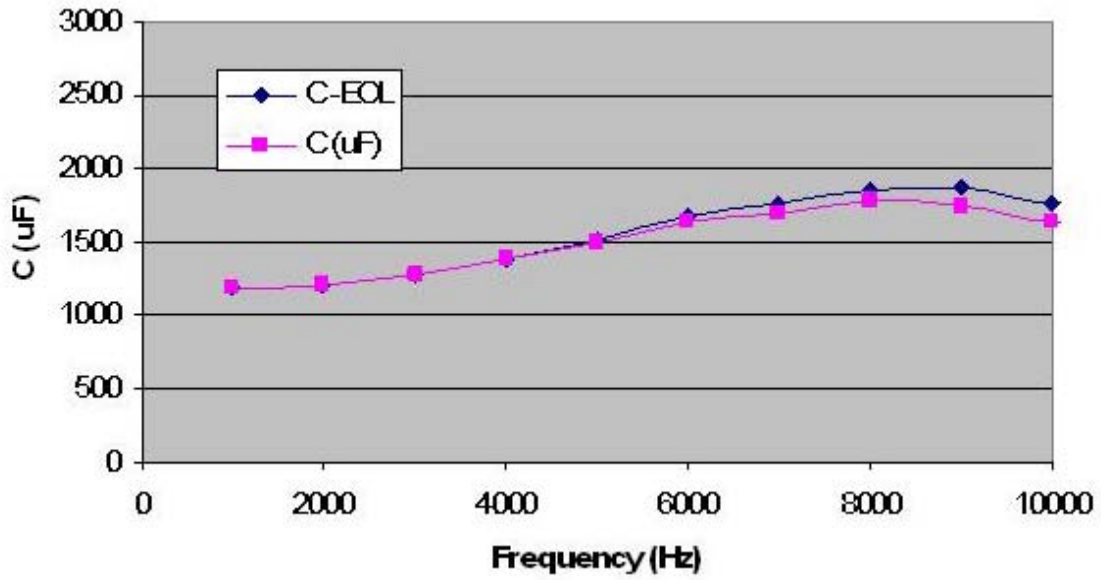

Fig. 3. Capacitance measurement comparisons.

Various aspects of the condition of the PEs and associated accessories were investigated within the EOL and unused Prius PEs modules. Although attempts were made to study impacts of vibration and thermal expansion upon solder interfaces, it is difficult to access the interfaces without altering them. For example, applying heat to remove the specimen would inadvertently reform the solder interfaces, and similar impacts would be incurred if the specimen were mechanically severed. Another trivial phenomenon is the impact of vibration and thermal expansion on wire bonds. Because the wire bonds are enclosed in silicone gel, it is difficult to obtain high resolution microscopic images of their structurally vulnerable locations, and removing the gel without applying stress to the wire bonds is difficult. Nonetheless, observations were made before and after gel removal, and there were no signs of abnormal behavior in the wire bonds or the surrounding gel. The overall efficiency of the inverter was monitored as it served as a drive to the EOL transaxle during characteristics tests conducted in the dynamometer test cell. The tests, described in greater detail later, showed significant consistency between the efficiencies of the EOL and unused Prius PEs. In comparing efficiencies at each test point, no greater than a 0.5% difference was observed between the two tests.

As shown in Fig. 4, a dial indicator was used to measure the amount of deformation across the interface of the cold plates. The separations between the three cold plates allow for the module to flex and/or expand when subjected to forces from thermal expansion or other perturbations. It is possible that over a lifetime of extended operation, the cold plates could become slightly warped due to prolonged subjection to the forces. If this happens, any voids not filled with thermal paste would result in compromised heat removal from the PEs devices. This phenomenon is difficult to measure while the cold plates are secured to the PCU housing with four bolts in each cold plate. However, the cold plate surface can be removed and compared with that of an unused PCU. Therefore, the bolts were removed and inspected, and there were no signs of stretching or abnormal threading. It was observed in both EOL and unused PEs modules that the centers of the cold plates tend to slightly bend toward the PEs devices. Thermal paste was removed from both units and inspected to ensure there were no degradations in heat transfer capability. As expected, energy-dispersive x-ray spectroscopy (EDS) analyses revealed no differences between the two specimens, and brief laboratory tests confirmed that the thermal conductivity of the substances matched. The EDS results showed that the paste had significant zinc content as well as silicon, aluminum, and oxygen content (see Fig. 5). Heat exchangers within the transaxle and PCU were inspected, and there were no noticeable signs of corrosion or abnormal artifacts (see Fig. 6).

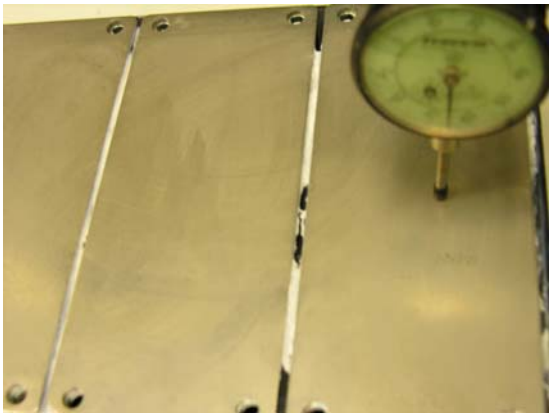

Fig. 4. Measurement of deformation of PEs module cold plate (upside down).

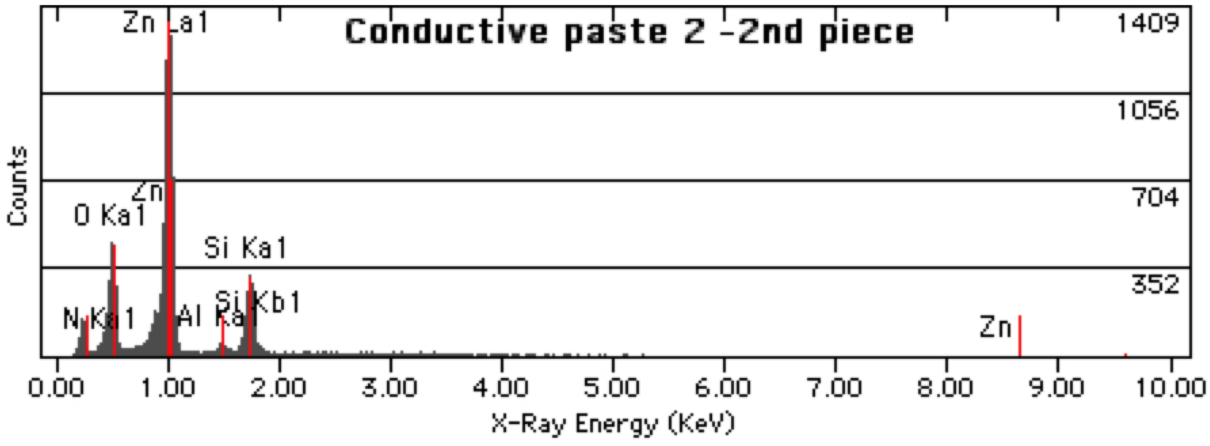

Fig. 5. EDS analysis of thermal paste.

Fig. 6. Heat exchangers for the transaxle (left) and PCU (right).

The transaxle was completely disassembled and inspected for degradations or signs of abnormal functionality (see Fig. 7, left, showing the motor windings, bearing, and rotor). There was a small remnant of oil with magnetic particles (metal shavings from gears) aligned in the shape of the "V" oriented magnets. The right portion of Fig. 7 indicates normal signs of wear on the differential gear obtained from gear meshing. The bearings were inspected, and they appeared to be in satisfactory condition considering the extent to which they were operated. Figure 8 shows both sides of the trochoid oil pump, which circulates oil for lubrication as well as heat removal. The pump rotates at a speed directly proportional to the rotational speed of the internal combustion engine. Therefore, the pump operates for a significant portion of any drive cycle. Nonetheless, there were no signs of excessive wear on the rotor of the pump or the pump housing.

The transmission oil is never normally changed over the entire life of the 2004 Prius, and therefore a significant amount of metal shavings were present in the oil obtained from the EOL Prius transaxle. Unfortunately, less than a quart of the used fluid was remaining in the EOL transaxle when it was received, and therefore no spinning loss tests could be conducted. However, viscosity measurements were made with a Mini Vis II Petrolab Grabner viscometer to compare the viscosity of the used fluid to that of unused fluid at various temperatures. As shown in Fig. 9, the viscosity of the used EOL fluid is about 37% lower than that of the unused for all tested temperatures. Nevertheless, it is evident that the impact of reduced viscosity will not be as substantial in the temperature range in which the motor usually operates, which is roughly 50°C and above.

Fig. 7. Motor rotor and windings (left) and differential gear (right).

Fig. 8. Trochoid oil pump.

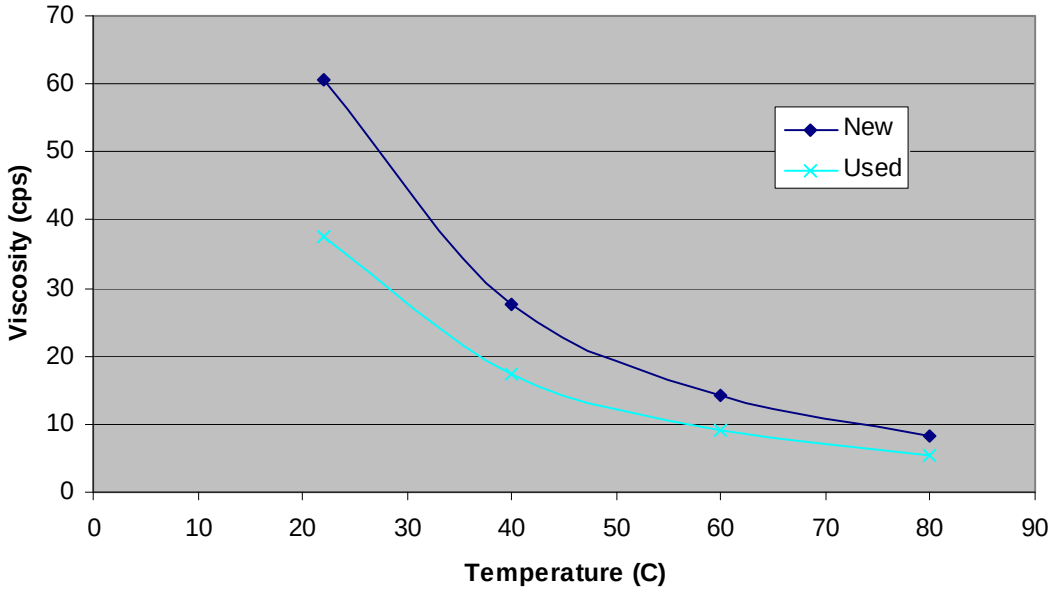

Fig. 9. Transmission oil viscosity versus temperature.

There are various potential degradations associated with the stator that are difficult to quantify, particularly when assessing the quality of the wiring insulation or paper inserts. Insulation on the conductors of the stator windings can be degraded as a result of the intense vibrations and torque pulsations of the motor. Insulation degradation can also occur as a result of voltage breakdown. This is also true for the insulation paper inserted between the conductors and the stator windings. Visual inspections were conducted in an attempt to discover any possible signs of insulation degradation, but no outstanding artifacts were observed. Additionally, current and voltage characteristics observed during dynamometer testing were consistent with previous benchmarking studies, and thus there was likely no substantial insulation degradation.

Further verification of the status of the winding conditions as well as the status of the PMs is gained through back-electromotive force, or back-EMF, and locked rotor torque measurements. The back-EMF measurements in Fig. 10 show that the induced voltage due to the rotating field of the rotor is essentially identical to what was found in previous benchmarking studies. This indicates that there was likely no degradation in the performance of the PMs and also indicates that the windings behave normally under moderate voltage conditions. Locked rotor torque measurements shown in Fig. 11 reveal significant agreement with that of previous studies. This confirms that the PMs sustained no detrimental impacts and verifies that the windings operate normally with high levels of current.

The used PCU and transaxle were installed into the dynamometer test cell in the same manner that these components were installed in previous benchmarking studies. It was of the utmost importance to ensure that the experimental conditions were as close as possible to the original tests. Therefore, the same controller hardware, control algorithm, coolant regulation system, data acquisition system, and measurement devices were used during these tests. Additionally, it was especially necessary to ensure that winding and inverter temperatures were consistent for each data point being compared. Because it is difficult to fully match all conditions of the original tests for all of the test points, about 20 torque and speed combinations were chosen throughout the entire operation range of the motor in which the test conditions were completely matched. Motor and inverter efficiencies were monitored, as were all ac and dc voltages, ac and dc currents, and temperatures throughout the system. It was observed that the motor efficiency varied no more than 1% and the inverter efficiency varied no more than 0.5% in reference to

the original data. Further investigations of the slight deviations did not reveal a specific trend in regards to any of the test conditions. For example, the efficiency difference between the EOL tests versus the original tests did not become increasingly negative with torque or speed. Therefore, these results provide reliable and informative feedback with regard to the condition of the subcomponents and overall characteristics after life-long operation.

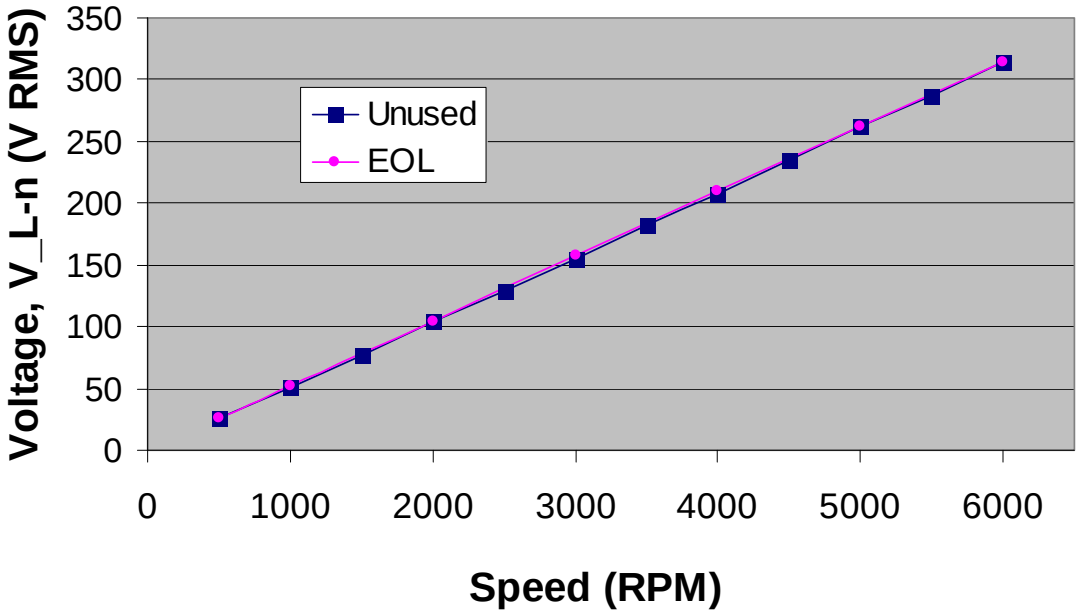

Fig. 10. Back-EMF voltage versus speed comparisons.

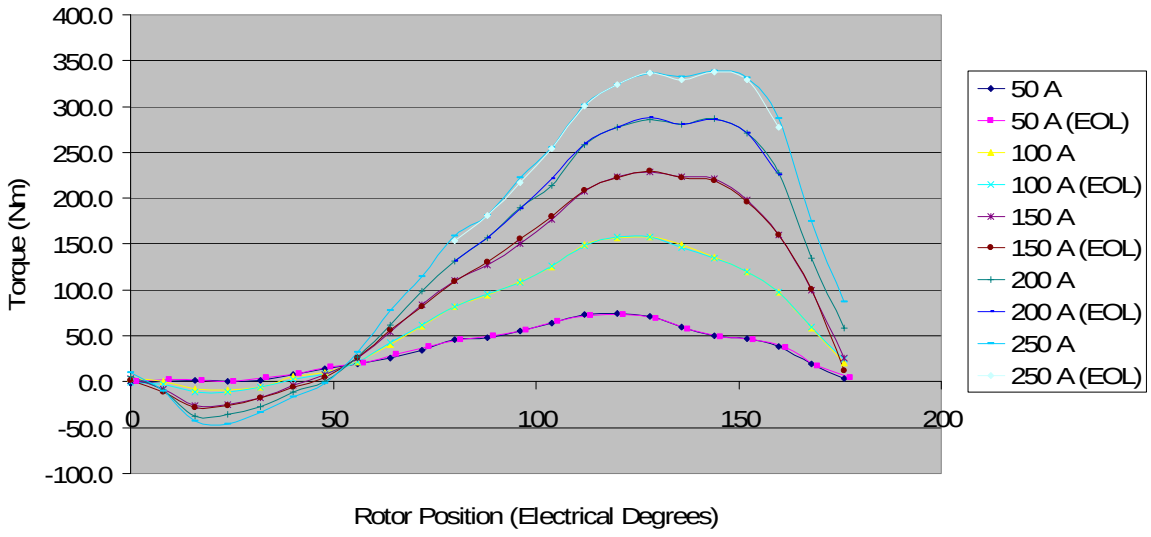

Fig. 11. Locked rotor torque versus position.

Benchmarking of the 2010 Toyota Prius

The subcomponents of the 2010 Toyota Prius were obtained to conduct preliminary benchmarking assessments on the PCU and transaxle, shown in Fig. 12 and Fig. 13, respectively. Published

specifications state that the motor power rating is 60 kW, a 10 kW improvement over the level of 50 kW in the 2004 Prius. The published maximum speed rating is 13,500 rpm, much higher than the former 6,000 rpm speed rating, whereas the torque rating is only 207 Nm versus the original 400 Nm. The published generator power rating increased by about 10 kW. The 2010 Prius operates with a dc link voltage of up to 650 V versus the 500 V level of the 2004 model. More detailed published specifications are provided in Table 1 along with comparisons with other hybrid systems

There are several outstanding findings from the preliminary teardown assessments from both the PCU and the transaxle. Upon disassembling the PCU, it was found that the PEs module was directly bonded to the cooling substrate instead of cooling plates being used as an interface between the PEs and heat exchanger. Also, instead of white thermal paste, a gray thermal paste was used between the opposite sides of the cooling substrate to provide cooling for the boost converter and 12 V accessory converter. Preliminary mass and volume assessments of the PCU are summarized in Table 2. Significant findings in the transaxle design include the observation of drastic conductor size reduction between the inverter and motor/generator. Even though the published power level has increased, the conductor size has decreased by nearly half as a result of moving to higher speed and voltage ratings. The 2010 generator design is much different in that it has a segmented winding configuration. Although the first generation Prius (produced up to 2003) included a generator with potted windings, the stator of the third generation Prius is segmented with only 12 stator teeth, as opposed to the conventional winding of the first generation Prius with 48 stator teeth. Detailed motor and generator parameters are provided in Tables 3 and 4, respectively.

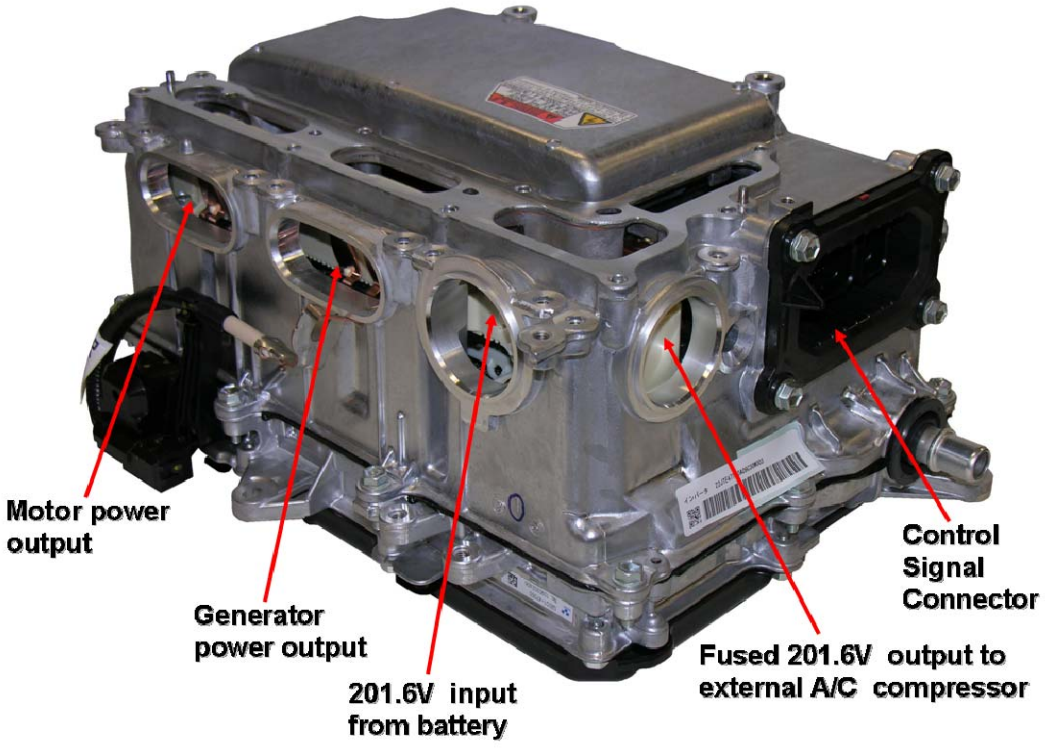

Fig. 12. 2010 Toyota Prius PCU.

Fig. 13. 2010 Toyota Prius transaxle/ECVT.

Table 1. 2010 Toyota Prius Published Information

Design Feature	2008 LS 600h	2007 Camry	2004 Prius	2010 Prius
Motor peak power rating	165 kW @5,250 rpm (disputed)	105 kW @4,500 rpm (disputed to be 70 kW)	50 kW @1,200–1,540 rpm	60 kW
Motor peak torque rating	300 Nm	270 Nm	400 Nm	207 Nm
Rotational speed rating	10,230 rpm	14,000 rpm	6,000 rpm	13,500 rpm
Generator specifications	Not published	Not published	33 kW	42 kW
Number of rotor poles	8	8	8	8
Bidirectional dc-dc converter output voltage	~288–650 Vdc	250–650 Vdc	200–500 Vdc	200–650 Vdc
Inverter/converter cooling	Water/glycol loop	Water/glycol loop	Water/glycol loop	Water/glycol loop
Hybrid transmission	Same as Camry, yet Ravigneaux high and low gear used for speed reduction	Planetary gears used for speed reduction and power split	A single planetary gear used for power split	Planetary gears used for speed reduction and power split
Fan-cooled high voltage Ni-MH battery	288 V, 6.5 Ah, 36.5 kW	244.8 V, 6.5 Ah, 30 kW	201.6 V, 6.5 Ah, 20 kW	201.6 V 27 kW

Table 2. 2010 Toyota Prius PCU Preliminary Mass and Volume Assessments

Item	Mass (kg)	Volume (L)
Inverter/converter as received from original equipment manufacturers	13.0	~18.6
PEs, controller/driver boards, cooling infrastructure	2.7	2.9
PEs, cooling infrastructure housing	1.9	3.6
Boost inductor, 12 V converter, and housing	5.9	5.8
Large capacitor	1.8	1.3
Connectors/sense wires/resistor	0.7	1.1

Table 3. 2010 Toyota Prius Motor Parameters

Parameter	2008 LS 600h	2007 Camry	2004 Prius	2010 Prius	Comments
Lamination dimensions					
Stator outer diameter (OD) (cm)	20	26.4	26.9	26.4	
Stator inner diameter (ID) (cm)	13.086	16.19	16.19	16.24	
Stator stack length (cm)	13.54	6.07	8.4	5.08	
Rotor OD (cm)	12.91	16.05	16.05	16.04	
Rotor stack length (cm)	13.59	6.2	8.36	5.0165	
Air gap (mm)	0.89	0.73025	0.73025	1.0033	
Lamination thickness (mm)	0.28	0.31	0.33		
Mass of assemblies					
Rotor mass (kg)	11.93	9.03	10.2	6.7	Includes rotor shaft.
Stator mass (kg)	18.75	18	25.9	15.99	
Stator wiring					
Number of stator slots	48	48	48	48	
Casing					
Motor casing mass (kg)	14	9.5	8.9	15	Resolver, pump, etc

Table 4. 2010 Toyota Prius Generator Parameters

Parameter	2008 LS 600h	2007 Camry	2004 Prius	2010 Prius	Comments
Lamination dimensions					
Stator OD (mm)	263.9	Same as LS	236.2	246.0	
Stator ID (mm)	162.1	Same as LS	142.6	152.7	
Stator stack length (cm)	7.07	3.58	3.05	2.7	
Rotor OD (mm)	160.5	Same as LS	140.72	151.3	
Mass of assemblies					
Rotor mass (kg)	9.7	5.19	4.01	3.93	Including rotor shaft
Stator mass (kg)	20.5	12.09	9.16	8.58	

Conclusion

- 2004 Prius EOL studies revealed only slight discrepancies.
  - Measured motor efficiency changed no more than 1% from original tests.
  - Measured inverter efficiency changed no more than 0.5% from original tests.
  - Behavior of capacitors shows only miniscule differences.
  - No damage to stator windings was found.
  - Transmission oil, which impacts rotational losses, was found to have 40% lower viscosity for all temperatures.
  - Slight wear due to gear meshing observed.
  - No degradation of PM capabilities over vehicle lifetime.

- Preliminary 2010 Toyota Prius benchmarking results were as follows.
  - Motor speed rating has increased from 6,000 rpm to 13,500 rpm.
  - Maximum boosted dc voltage has increased from 500 V to 650 V.
  - Size of motor/generator power leads has been drastically reduced.
  - PEs module is bonded directly to the water-cooled heat exchanger.
  - Preliminary mass and volume assessments indicate significant reduction in motor size.

Publications

None.

References

None.

Patents

None.

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