Role of Substrate Choice on LED Packaging

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LED Substrate Choices

Substrate	Advantages	Disadvantages
Sapphire	Globally dominant, Relatively low cost	Difficult to scale size
SiC	Lattice match closer than sapphire, Unique device structures possible	Not widely available at low cost
GaN	Lattice matched, Reduced droop	Cost, large diameters not available
Silicon	Takes advantage of low-cost semiconductor manufacturing infrastructure	Epi growth difficult to master

LED Chip Architectures Using Various Substrates

LED Substrate	Surface Emitters	Volume Emitters
Sapphire	Philips TFFC	Nichia PSS
SiC	CREE EZ	CREE SC[3]
GaN	X	Soraa GaN-on-GaN
Silicon*	Toshiba LETERES	X

New

Surface emitters:

High surface brightness, typically use conformal phosphors

Volume emitters:

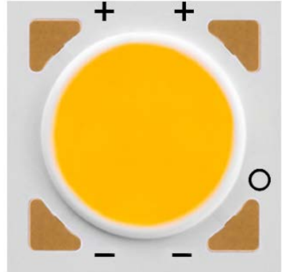
Typically use dispensed phosphors

* Can be a drop-in replacement

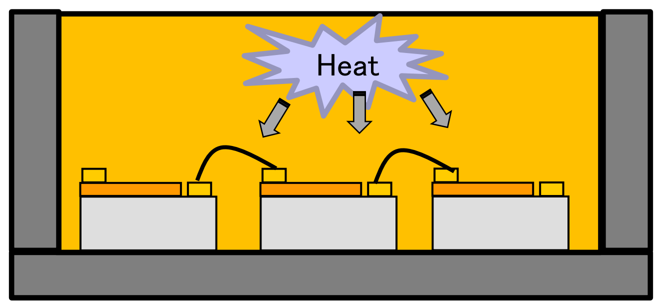
Packaging for High Current-Density LED Operation

Goal: Operate die at high current density to reduce chip cost

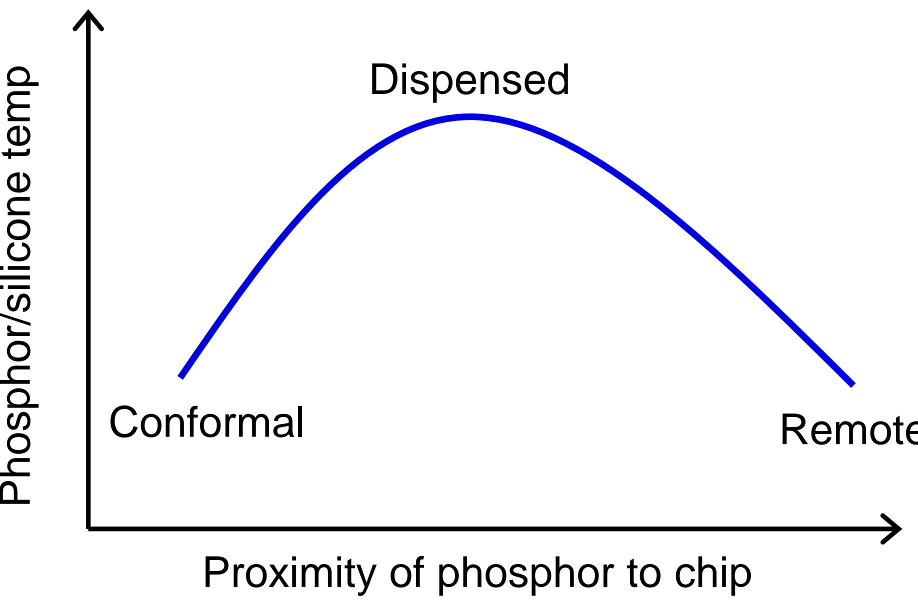
Problem: phosphor/silicone temperature must be controlled



COB example:



The LED chips are heatsinks!



The phosphor solution depends on the substrate!

Packaging for High Current Density LED Operation

Goal: Reduce chip cost by driving LEDs hard

Substrate	Phosphor Technology		
	Conformal	Dispensed	Remote
Surface emitter (Si, Al_2O_3, SiC)	✓	✓	✓
Volume emitter (GaN, Al_2O_3, SiC)	?	✓	✓

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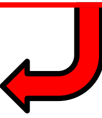
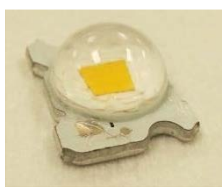


Phosphor/silicone remain cool – no limit on chip size

Example:



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Phosphor/silicone remain cool – also, no limit on chip size

Example:

Generally use many small die to avoid overheating phosphor– added assembly complexity

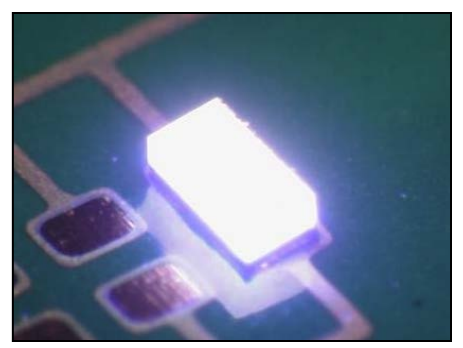
Examples:
Typical COBs, GaN-on-GaN

"Packaging" Solutions Possible for GaN-on-Si

❑ *LED Integration*

Large wafers enable single-chip solutions for most common lighting applications

❑ *Package-less solution*



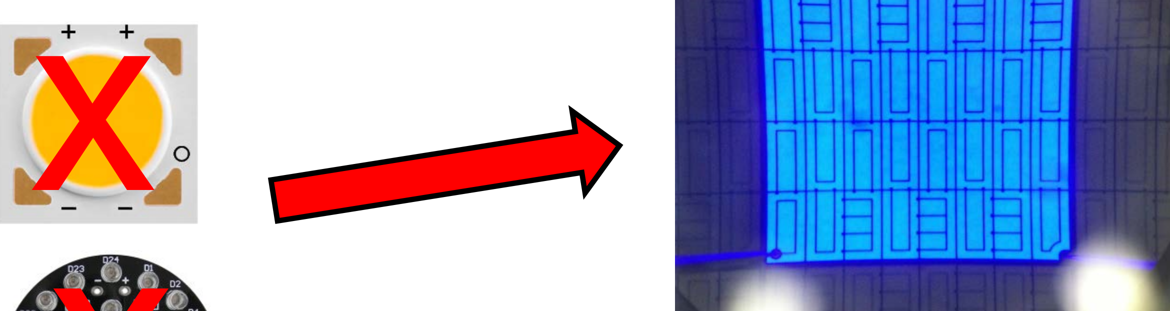
"Chip-scale package"

"Chip-on-application"

Ideal for distributed light sources

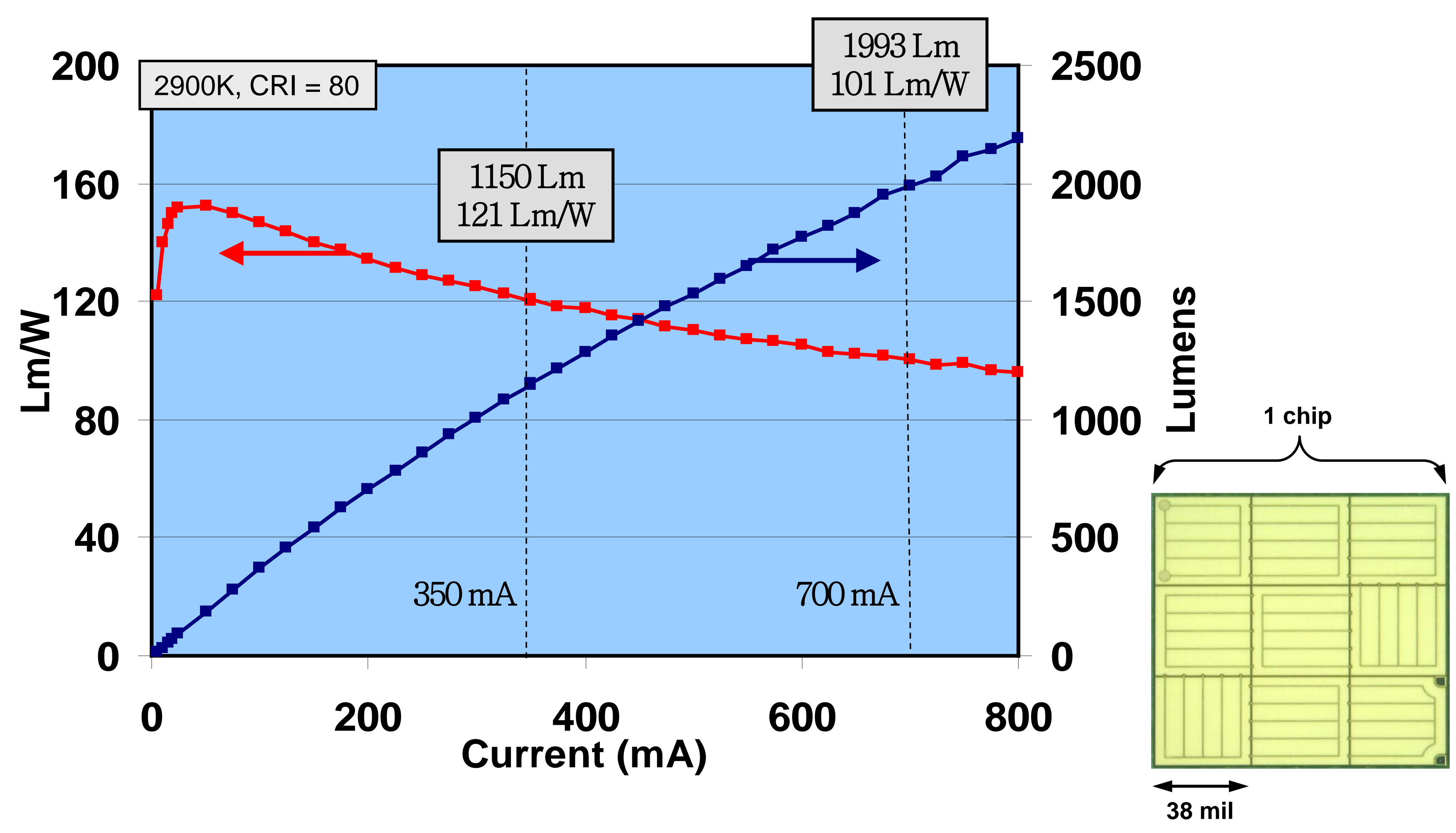
GaN-on-Si Enables More Integrated Solutions

- Single-chip LED light source with >>1000 Lm
- On-wafer integration of LEDs & phosphor
- Voltage and current determined by series/parallel connections between LEDs
- Single die placement, minimum wire bonds, even for high lumen sources
- Minimum source size, highest possible lumen density, and reduced package cost



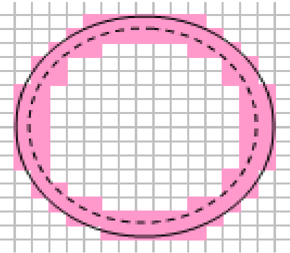
Example: 3mm x 3mm
32 junction GaN-on-Si LED

Example: Single Chip A19 Source



Why GaN-on-Si for Integrated LEDs

- **Big chips require large wafers!**
- **Semiconductor industry processing enables very high yields**



2” wafer with 3mm die
> 40% edge exclusion loss

Chip-Scale Package Based on GaN-on-Si

LED chips on Sapphire

Conventional Package — *Individual Assembly Process*

Singulation → Mounting → Wire Bonding (Au Wire) → Phosphor Dispense (Phosphor)

All Wafer Level Fabrication

Toshiba Concept → Cu Electrodes → Substrate Removal (Si sub.) → Phosphor Layer Formation → Singulation

Phospher w/ silicone
blue LED (GaN)
Cu

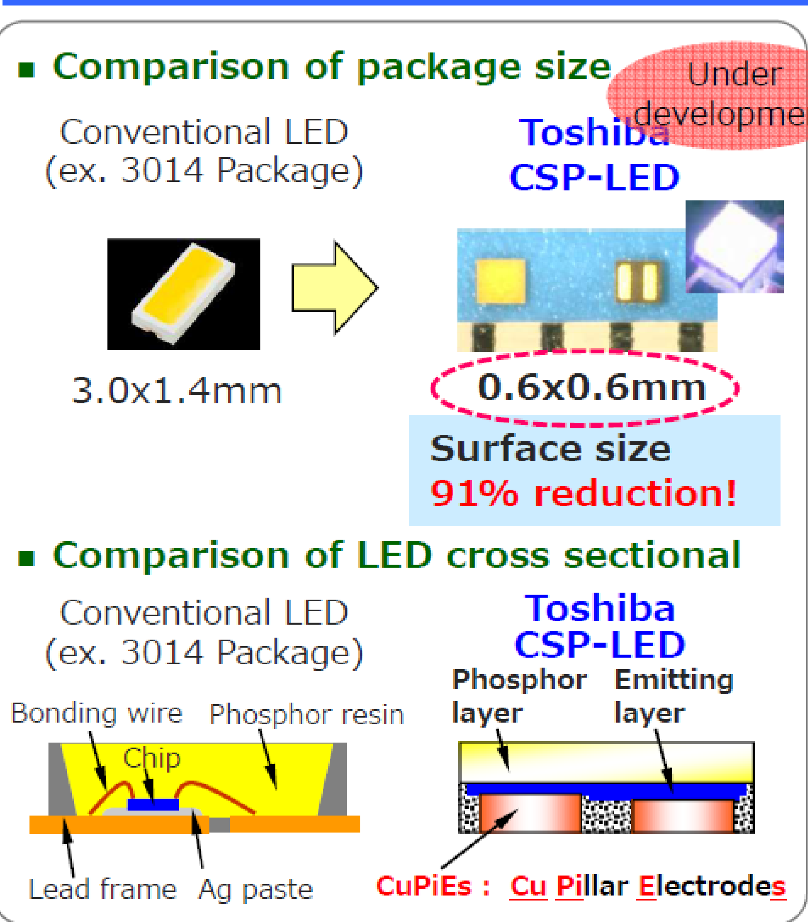
Concept

1. *High thermal dissipation using Copper Pillers*
2. *Extremely small package leads to design flexibility*
3. *All wafer level fabrication material/process cost reduction*

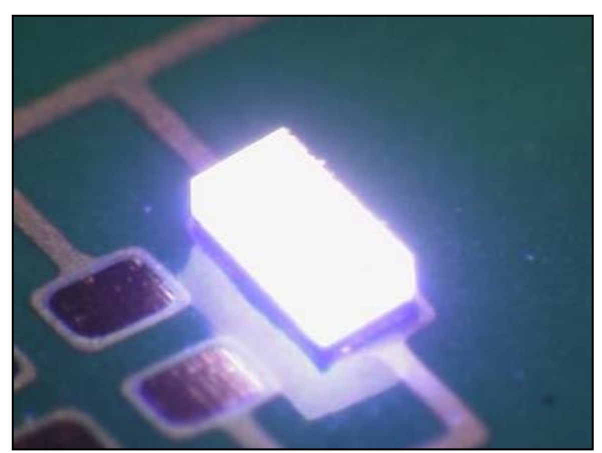
Concept and features of CSP-LEDs

CSP-LED brings new design and added values for lighting system.

W/W No1! Smallest package in Quarter ~ Half Watt LEDs



- ***Chip-Scale-Package LED***
  - *Small and thin package.*
  - *Point light → Small lens design(lower cost)*
  - *New concept "strip" or tiny lighting system.*
- ***Low thermal resistance***
  - *Cu-pillar electrodes.*
- ***Original wafer level process***
  - *Wafer warping control, Phosphor thickness precise control and bonding wire less design.*



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Conclusion

- LED substrate choice has downstream consequences for packaging
- New LED substrates, Si and GaN offer unique opportunities for SSL
- GaN-on-Si enables integrated, single-die sources and advanced chip-scale package architectures