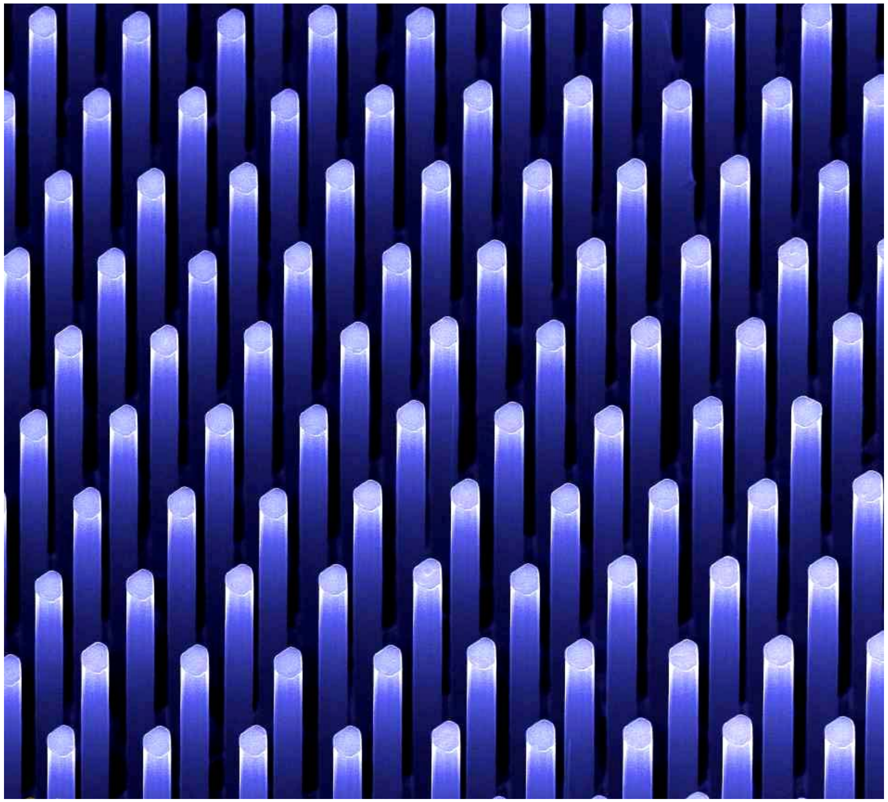

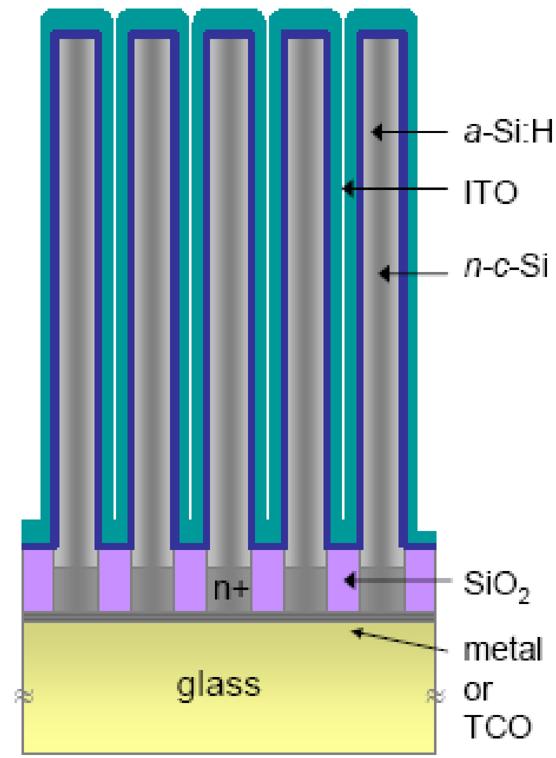

High Aspect Ratio Semiconductor Heterojunction Solar Cells

Future Generation Photovoltaics

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26th May 2010

This presentation does not contain any proprietary, confidential or otherwise restricted information.

Timeline

- Project start date: 2/1/08
- Project end date: 7/31/11
- Percent complete: 50%

Budget

- Total project funding
  - DOE share: $900,000
  - Contractor share: $225,000
- Funding received in FY09: $450,000
- Funding for FY10: $225,827

Barriers

- The project is aimed at developing low cost crystalline silicon solar cells on glass using a high aspect wire array structure designed to maximize light absorption and carrier collection.

Faculty Participants

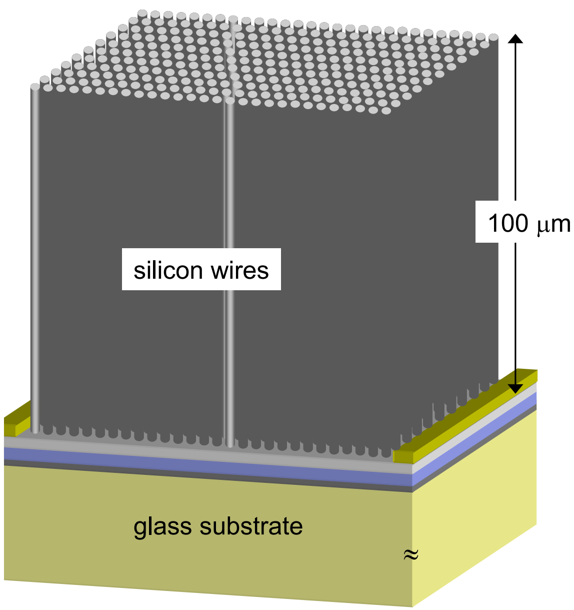
- Elizabeth Dickey (MatSE)
- Theresa Mayer (EE)
- Tom Mallouk (Chem)
- Joan Redwing (MatSE)
- Chris Wronski (EE)

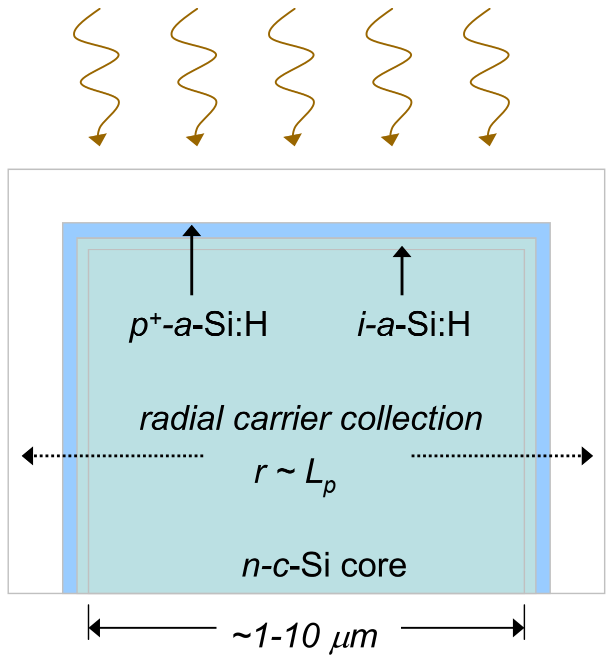
Challenges, Barriers or Problems

- Device design
  - To achieve optimum efficiency, wire radius should match the carrier diffusion length
    - Dependent on doping and trap density in Si wires
      - Not well understood for VLS-grown Si wires
- Recombination
  - Low V_{OC} of previously reported Si nanowire solar cells attributed to recombination in bulk (due to catalyst impurities) or at surface (due to high surface area)
    - Methods to reduce bulk traps and surface states are needed
- Cost
  - Low cost fabrication methods are essential to realize full potential of this approach

Radial Junction Nanorod Solar Cell

- Decouples directions of light absorption and carrier collection
- Offers potential for increased collection efficiency in materials with short minority carrier diffusion lengths (*L*)





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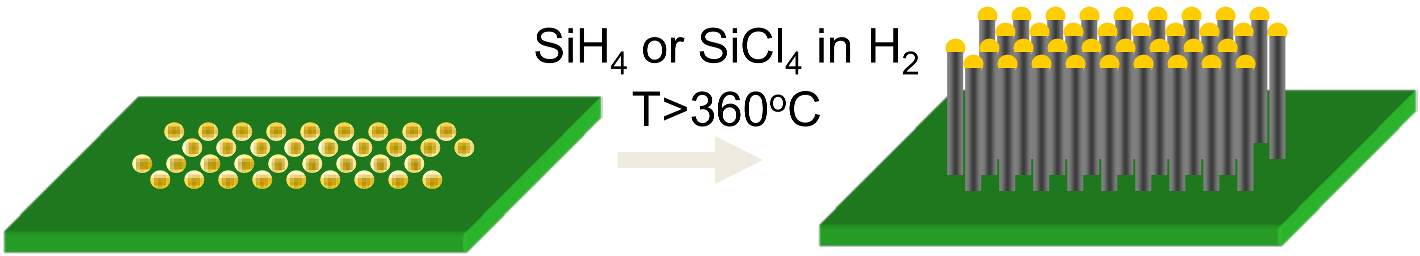
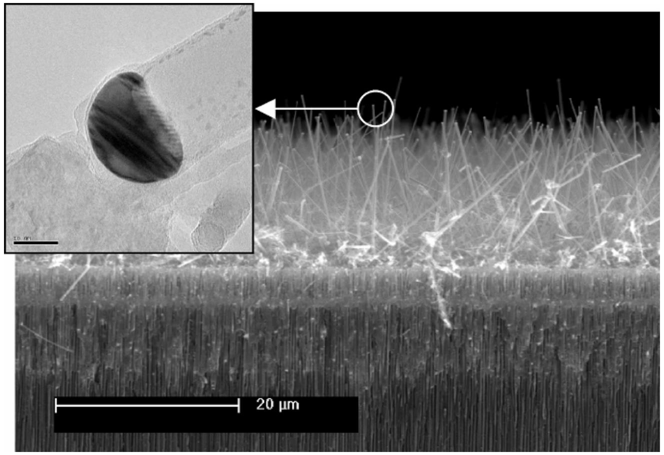
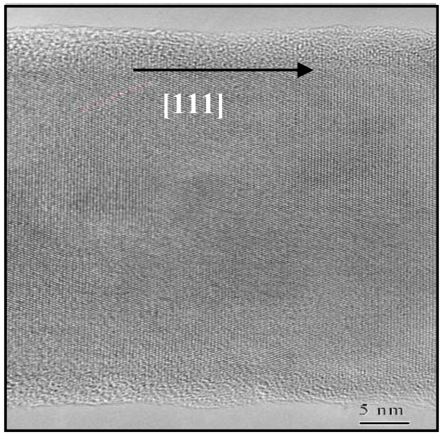
Vapor-Liquid-Solid (VLS) Growth of Si Wires

- Enables growth of single crystal Si wires on non-crystalline substrates.
- Wire diameter controlled by size of metal catalyst particle.



Si nanowires grown by VLS on anodized alumina templates



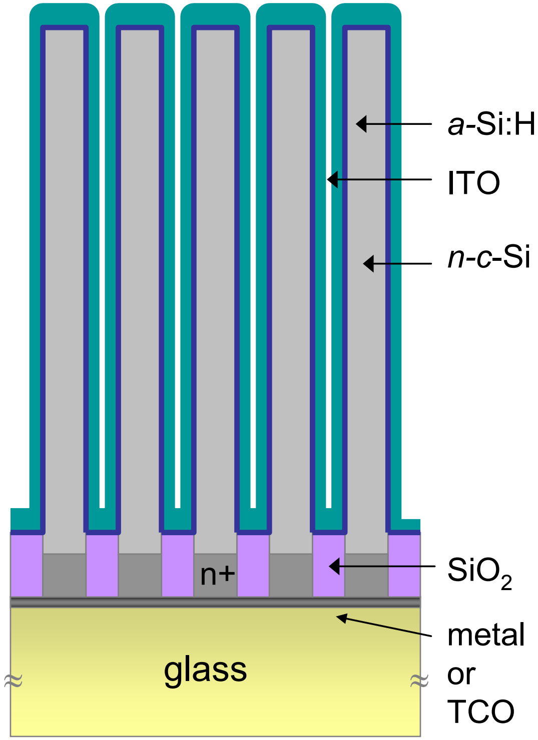


T.E. Bogart, S. Dey, K.K. Lew, S.E. Mohney and J.M. Redwing, Adv. Mater. 17 (2005) 114.

High Aspect Ratio Silicon Heterojunction Solar Cell

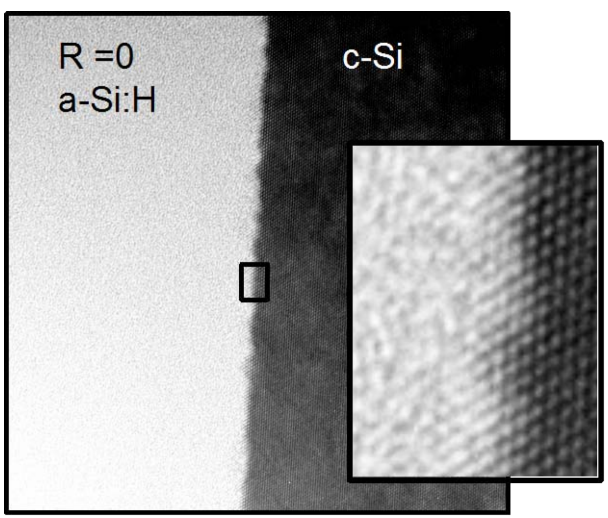
- High density array of crystalline Si wires formed on glass by vapor-liquid-solid growth at reduced temperature and high growth rate.

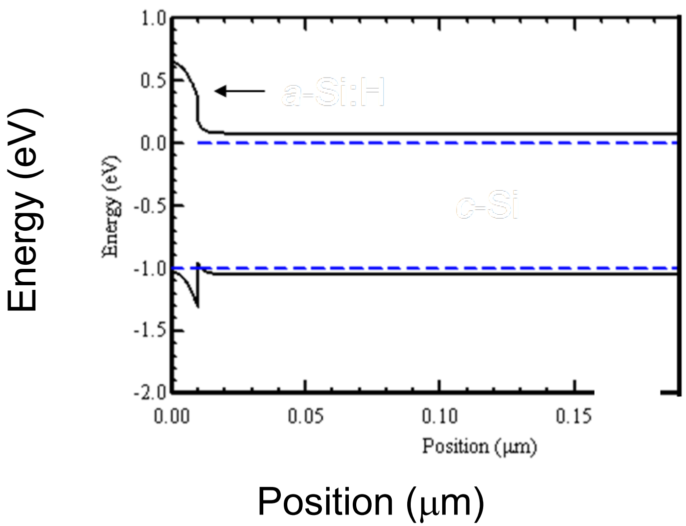
- Amorphous hydrogenated silicon (a-Si:H) used to passivate surface of wires.



Amorphous Hydrogenated Si Coating

- Similar to "heterojunction with intrinsic thin layer" (HIT) solar cells
- Ultra-thin (~10 nm) intrinsic a-Si:H and p-type a-Si:H contact layer
  - Effectively passivates crystalline Si surface
    - Low interface recombination and dark current, high V_{OC}
    - 20.7% efficiency reported for optimized HIT cell





Project Period Goals (March 2009 to April 2010)

1. Device design and modeling
   - Evaluate effect of carrier diffusion length on performance of Si pillar array solar cells

2. Si wire array fabrication
   - Demonstrate controlled p-type doping
   - Investigate alternative catalysts for VLS growth
   - Demonstrate initial transfer of patterning and wire growth process to glass

3. Semiconductor-liquid junction studies
   - Evaluate effect of catalysts and surface cleaning on photoelectrochemical properties of Si wire arrays

Project Period Goals (March 2009 to April 2010) Cont'd.

4. Radial junction fabrication
   - Improve uniformity of a-Si coating on Si pillars and wires

5. Radial junction characterization
   - Demonstrate a radial p-n junction Si wire array solar cell using VLS-grown Si wires
   - Fabricate a HARSH cell using a-Si:H shell layer

- 18 Month Go/No-Go Milestone (January 2010):
  - Demonstration of high aspect ratio Si wire array liquid junction cells and radial junction solar cells on Si substrates and measurement of their photoelectrochemical and photovoltaic characteristics.

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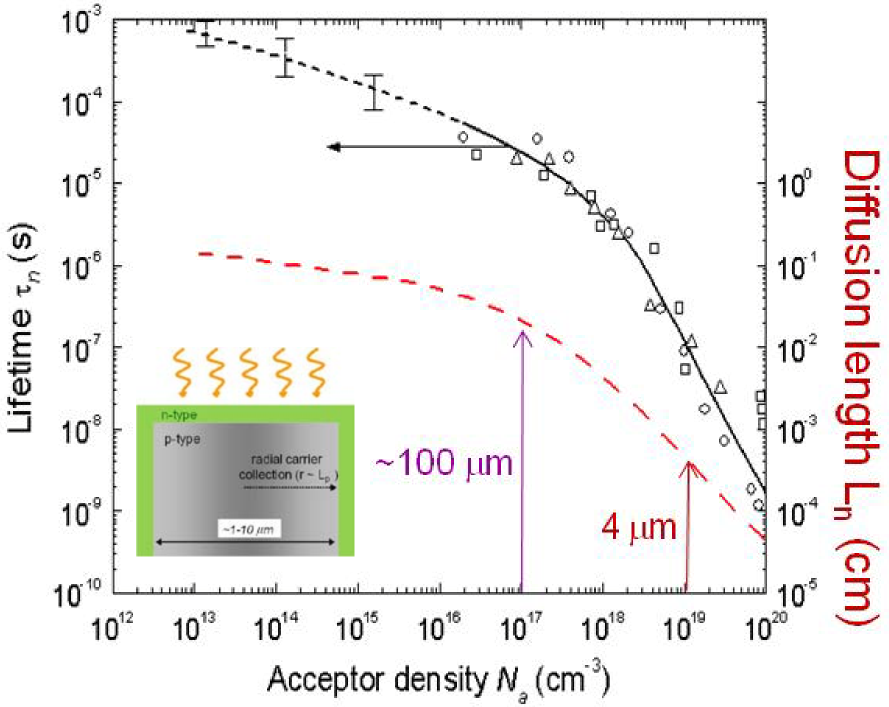
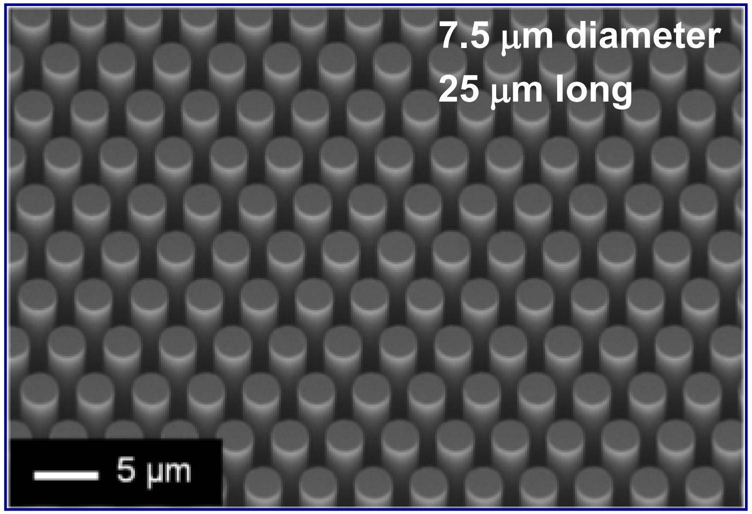
Evaluating the radial junction – DRIE Si pillar array cells

- Used highly doped silicon with short carrier diffusion length to compare performance of Si pillar arrays vs. planar devices.

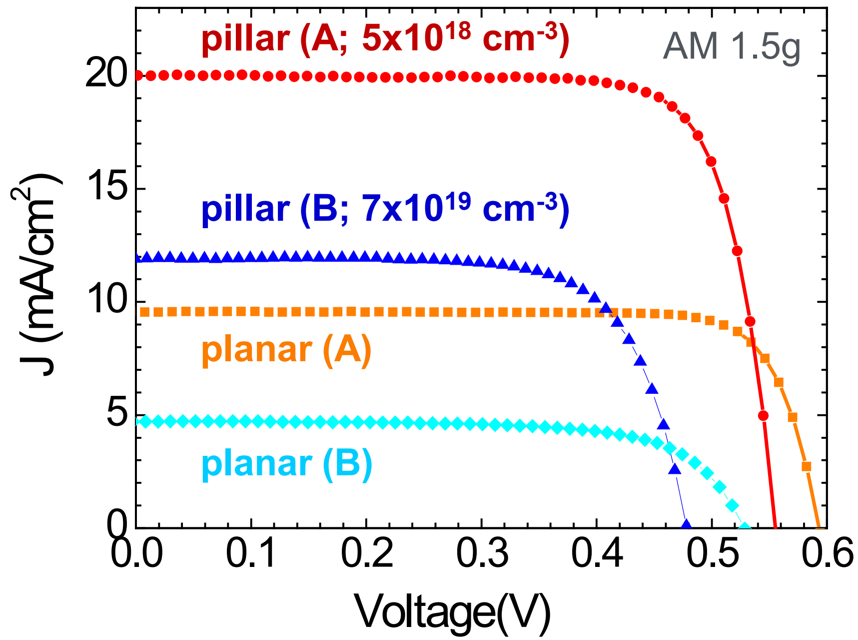


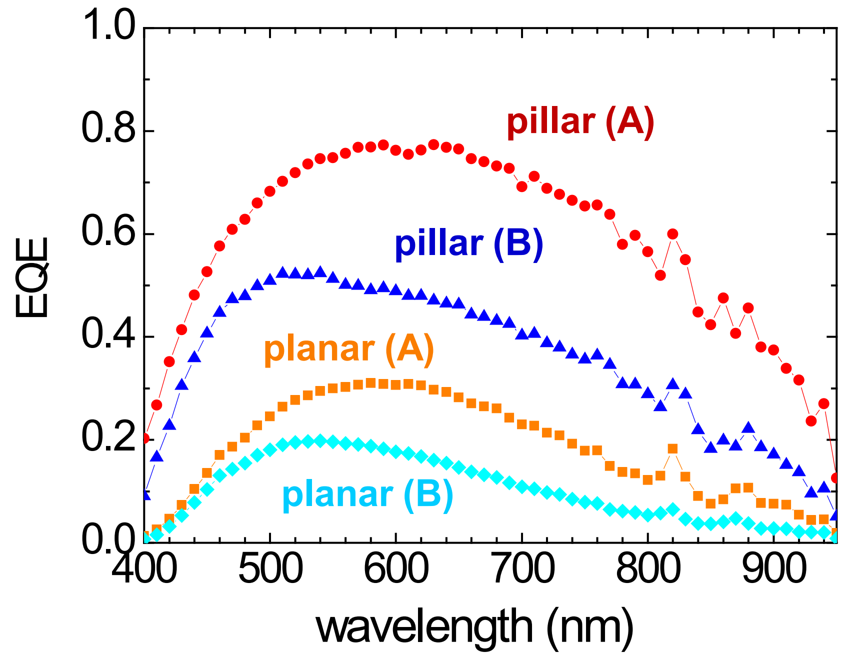
Tyagi, M. S. and R. Van Overstraeten, Solid State Electron. 26, 6 (1983) 577-598



- Deep reactive ion etching (DRIE) and *n*-type dopant diffusion were used to fabricate n^+–p^+ *c*-Si pillar arrays.
- Two p-type Si substrates:
  - **Sample A: p=5x10^{18} cm^3,**
  - **Sample B: p=7x10^{19} cm^{-3}**

Si Pillar Array Cells – Light I-V and Spectral Response

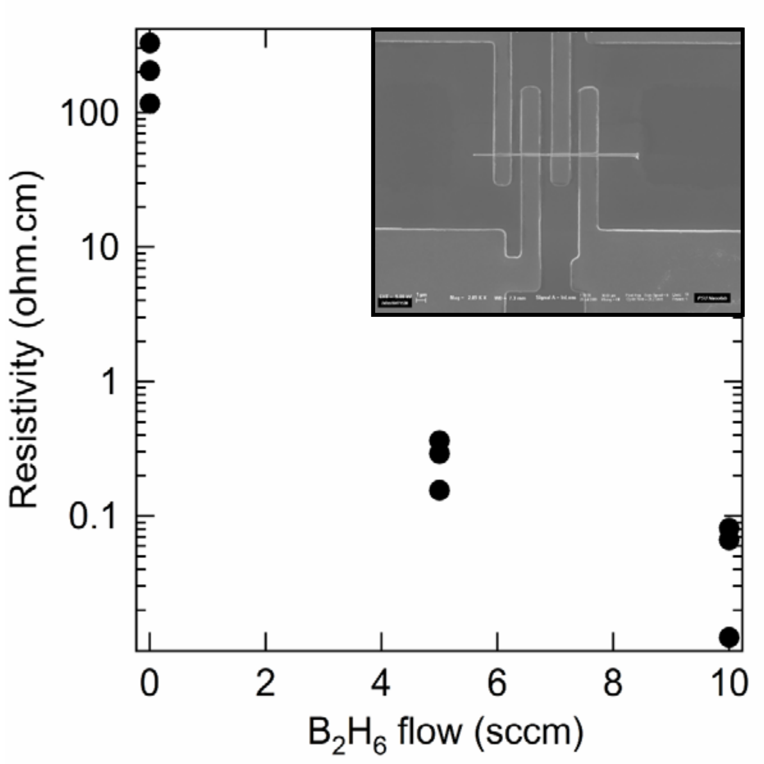




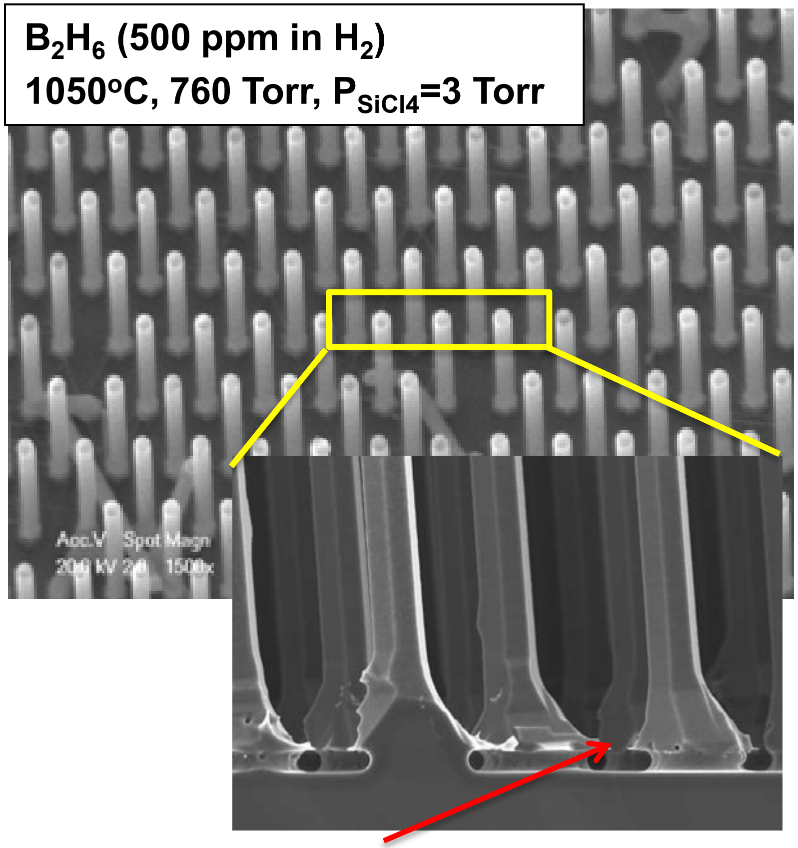
Device	Jsc (mA/cm²)	Voc (V)	FF (%)	Efficiency (%)
A (planar)	9.6	0.59	80.8	4.6
A (pillar)	20.0	0.56	78.1	8.7
B (planar)	4.7	0.53	71.5	1.7
B (pillar)	11.7	0.48	71.4	3.7

- Confirms that the radial junction geometry is effective at improving solar cell efficiency for materials with short minority carrier diffusion lengths.

In-Situ Boron Doping of VLS-grown Si Wires



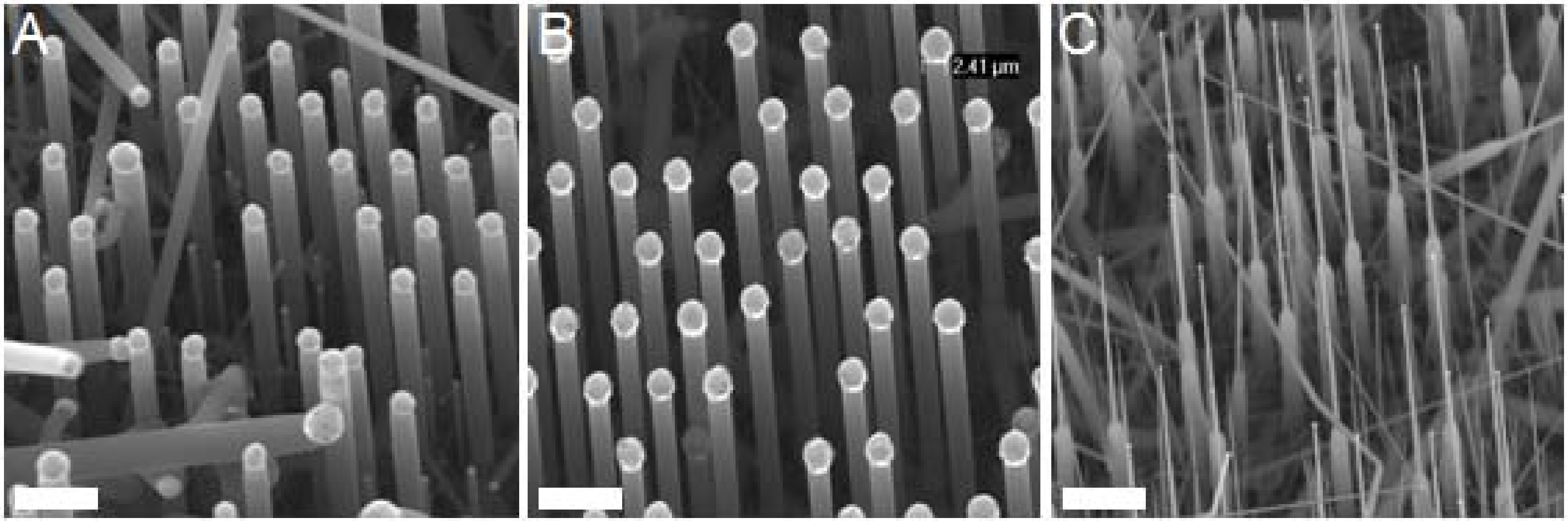
Four-point measurements of single wires show decreasing resistivity with addition of B_2H_6 during VLS growth.



B_2H_6 also results in formation of Si base layer which is problematic for devices – other dopant sources are being investigated.

Alternative Catalysts for VLS Growth – $SiCl_4$ Source

- Interest in replacing gold as catalyst due to concerns over deep level states and cost
- Results demonstrate that copper and nickel are also effective catalysts for growth with $SiCl_4$

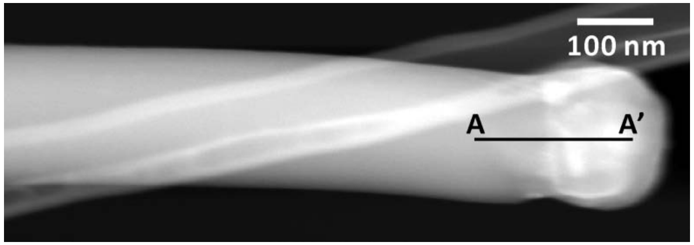


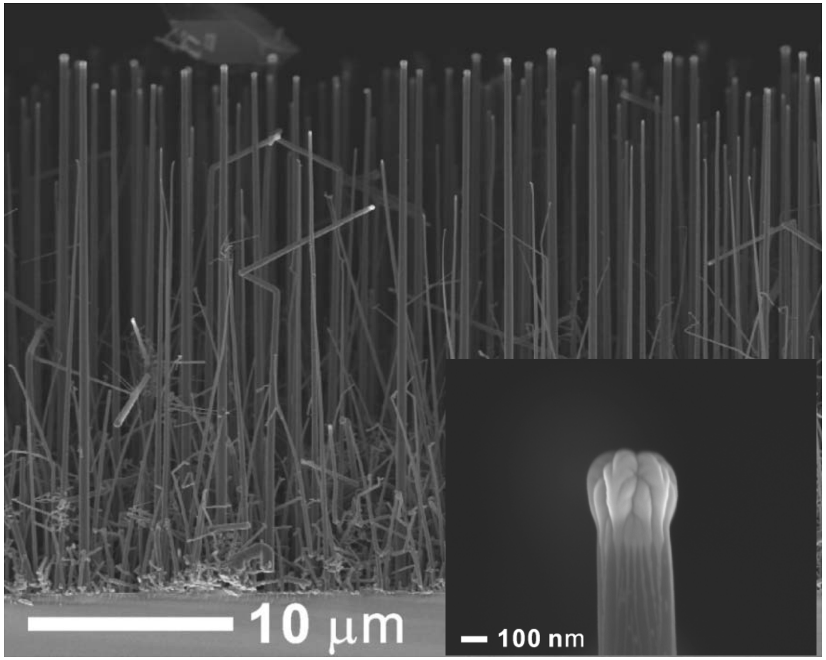
Silicon wires grown with a) copper b) nickel and c) silver.

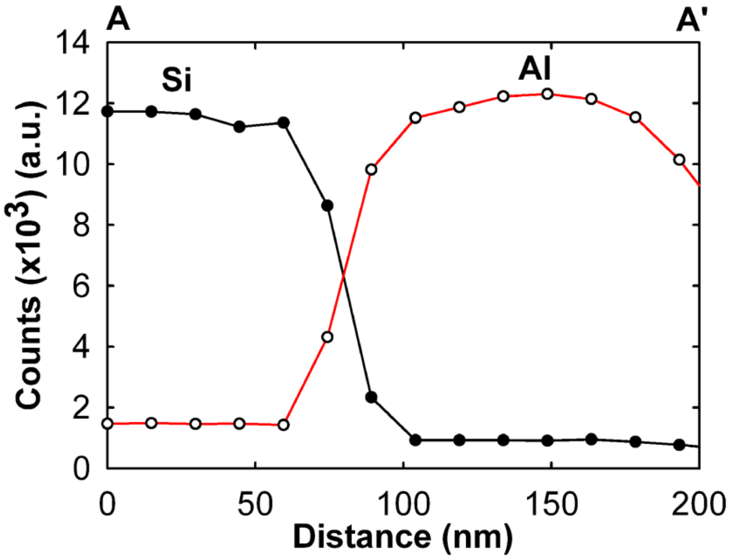
1050°C, 760 Torr, P_{SiCl4}=3 Torr, (111)Si substrates

Aluminum-Catalyzed Si Wire Growth – SiH_4 Source

- SiH_4, T=500-650°C, P=100-600 Torr
- Epitaxial Si NWs obtained at high growth rates (up to 10 μm/min)







- Wires exhibit p-type conductivity
  - ρ = 0.01±0.004Ω-cm
  - p≅ $1x10^{19}$ cm^{-3} (bulk Si mobility)

- *Collaboration with Illuminex Corp. (DOE STTR)*

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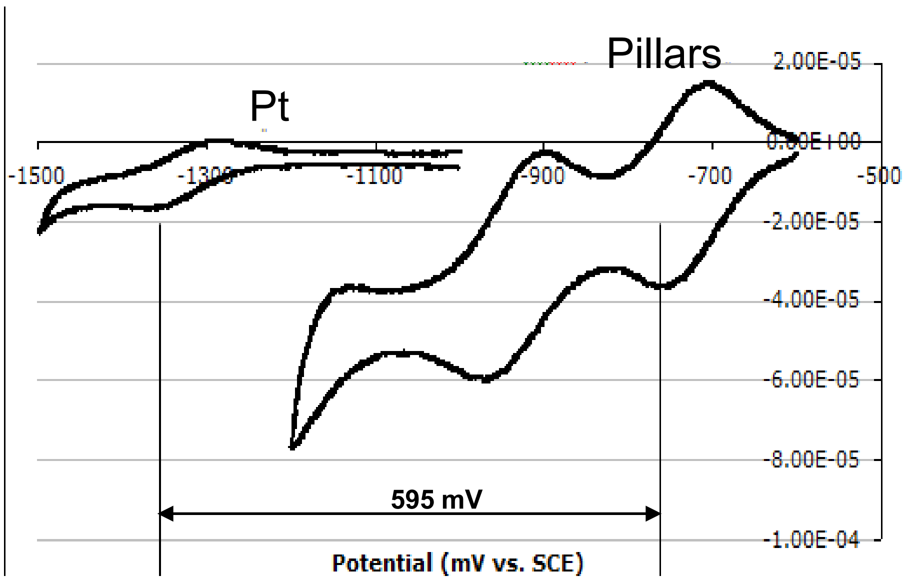
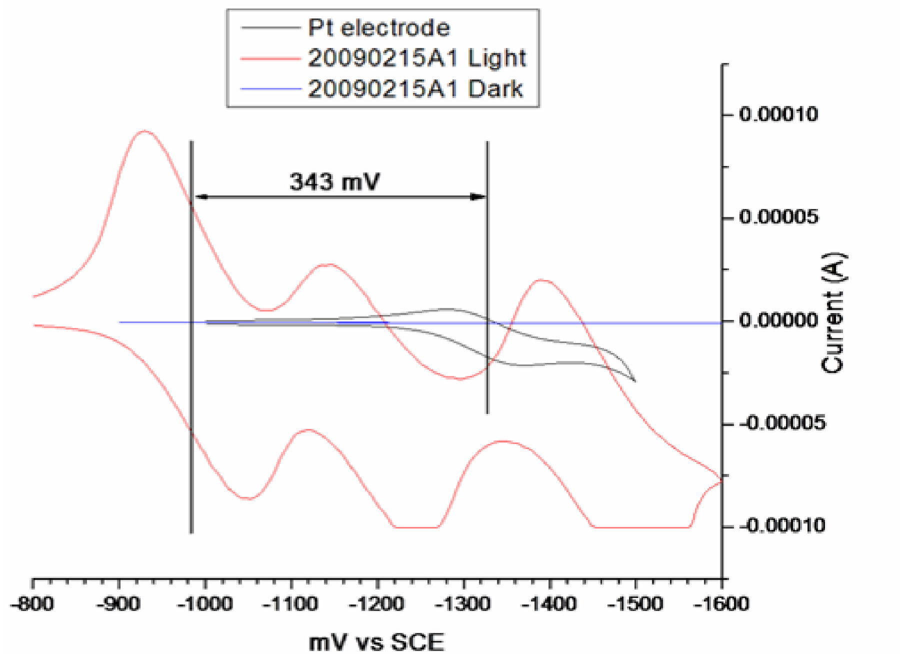
Liquid Junction Analysis of Si Pillar/Wire Arrays



32 μm diameter by 25 μm long DRIE silicon pillar arrays.

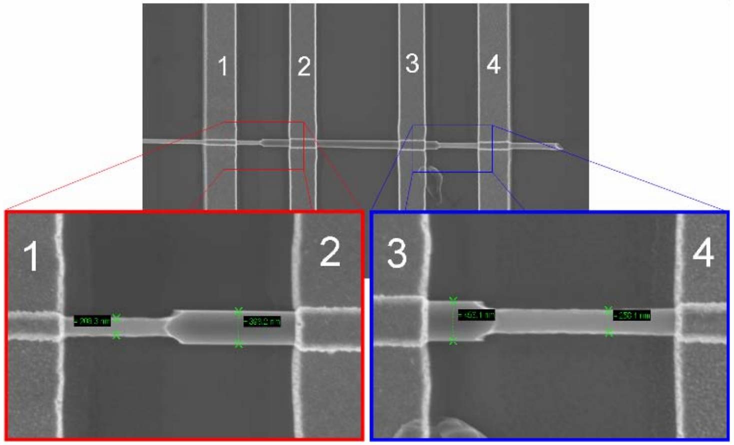


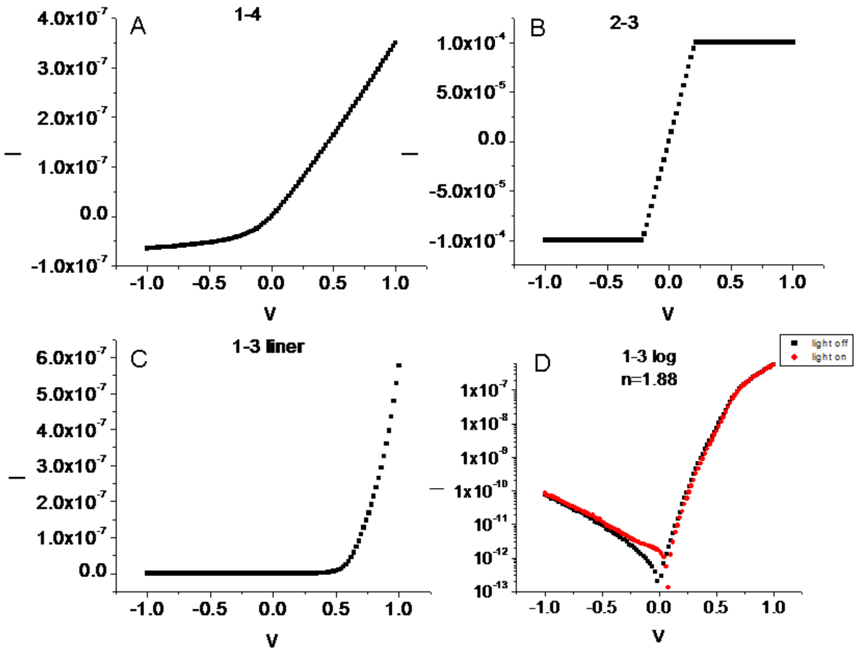
2 μm diameter by 80 μm long Au-catalyzed silicon wire arrays.

Photoelectrochemical measurements of the DRIE etched Si pillars show a V_{oc} value of 595 mV, while the Au and Cu catalyzed Si wires have lower V_{OC} due to possible surface states.

Single Wire Radial Junction Devices

- Electrical testing of single wire devices is used to evaluate the radial p-n junction without the additional series and shunt resistances possible in the wire arrays.
- Selective etching is used to remove the outer n-type shell for electrical contact to the p-type wire core.





I-V curves obtained for:

A) The p-type wire core (contacts 1-4)
B) The n-type shell (contacts 2-3)
C) The p-n junction (contacts 1-3), linear scale
D) The p-n junction (contacts 1-3), log scale

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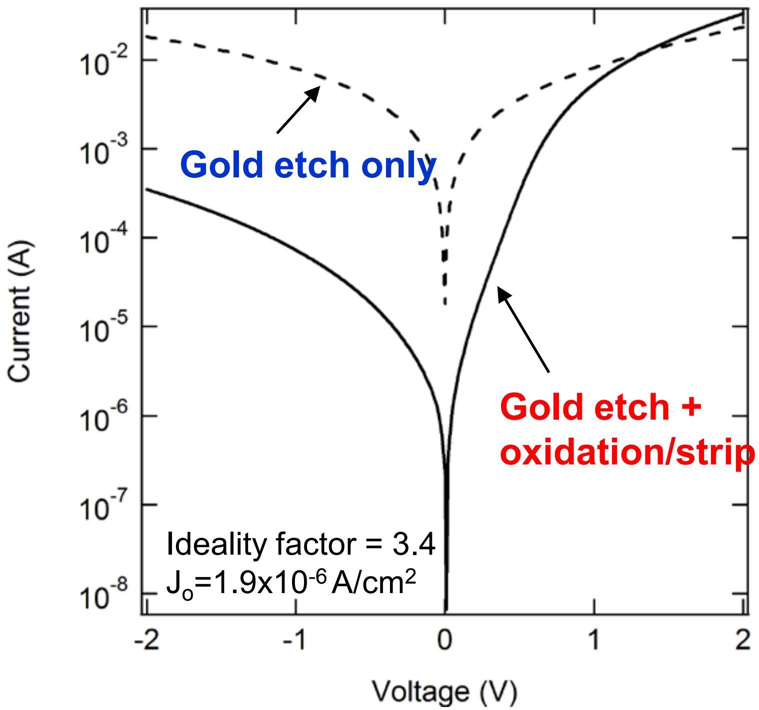
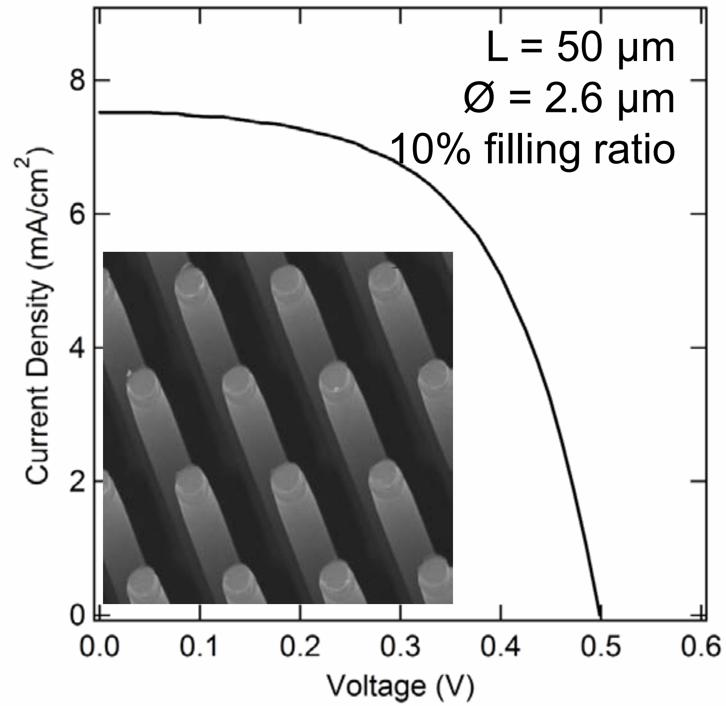
VLS-grown Si Wire Array Solar Cell

- Radial junction formed by $POCl_3$ dopant diffusion to an expected junction depth of ~200 nm into p^- Si wires grown by gold-catalyzed VLS on p^+ Si ($p \sim 10^{19}$ cm^{-3}) substrates
- Surface cleaning required to remove residual gold





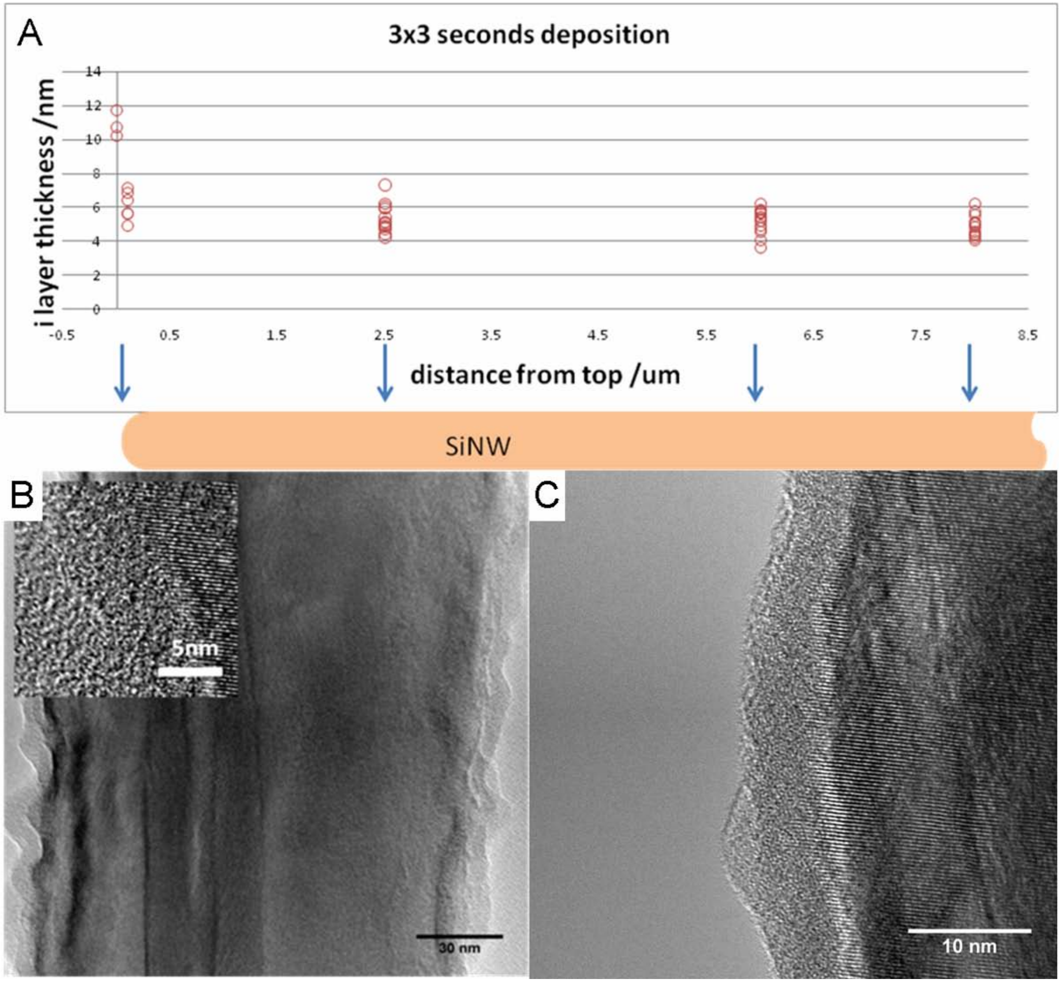
Wire Dia.	V_{oc} (V)	J_{SC} (mA/cm²)	Fill Factor	Efficiency
2.6 µm	0.50	7.6	57%	2.3%

Amorphous Si Coating of Si Wires by PECVD

A. Thickness of the intrinsic a-Si:H layer along the silicon nanowire to the required thickness for the HIT cell structure (deposited for 3 x 3 seconds)

B. TEM images of the intrinsic a-Si:H layer on a silicon nanowire grown by $SiCl_4$.

C. Close up image of the intrinsic a-Si:H layer on the silicon nanowire.



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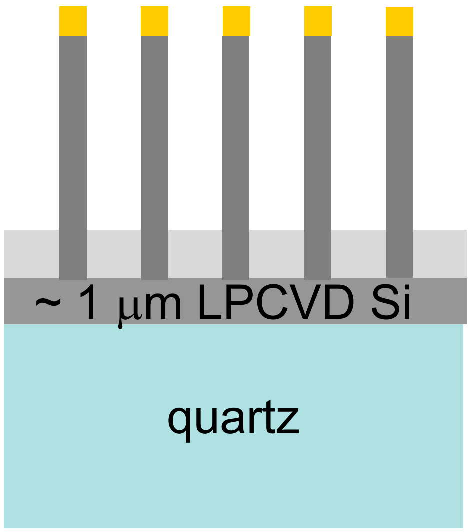
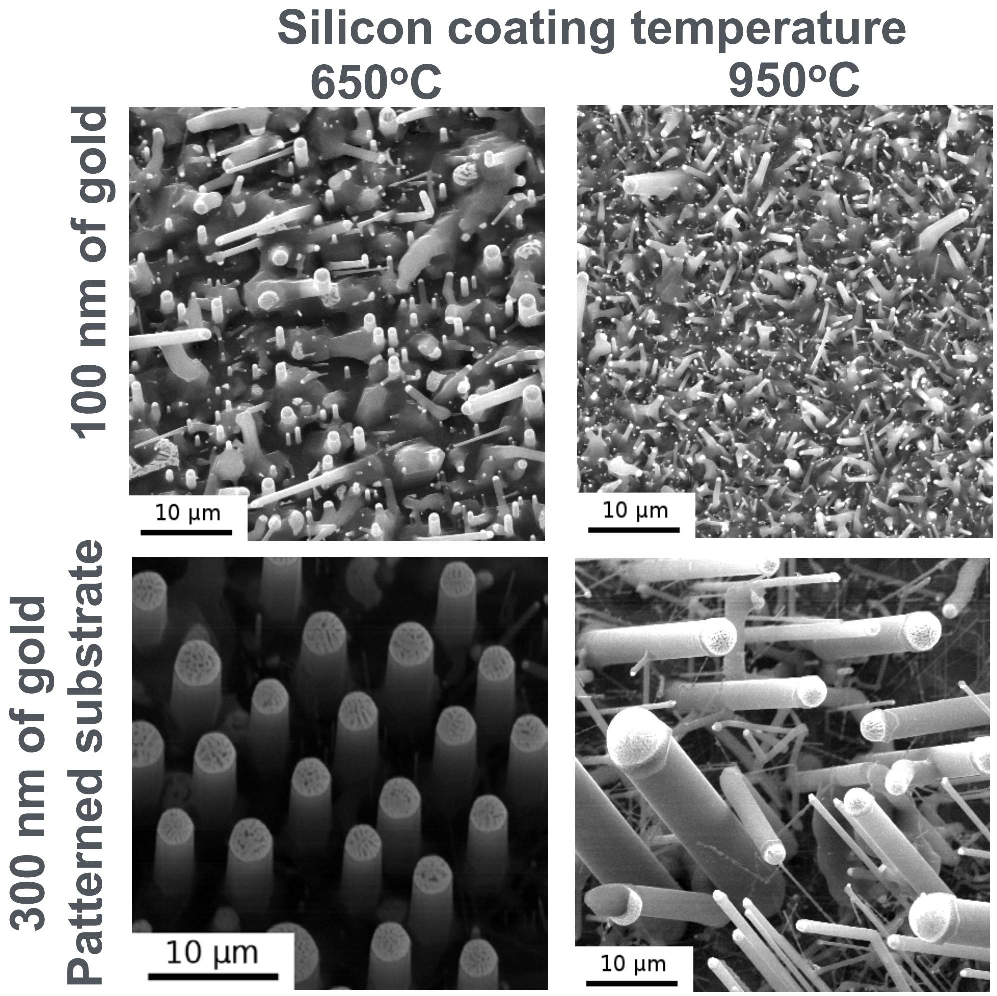
VLS Growth of Si Wire Arrays on Quartz





- Vertically-oriented Si wires obtained with 650°C LPCVD Si template on quartz

Budget Status and Potential for Expansion

- Total project funding:
  - DOE share: $900,000
  - Penn State cost match: $225,000
    - Cost match includes stipend and tuition for one graduate student for 3 years and user fees for analytical and nanofabrication equipment.
- Project timeline status:
  - A 6 month no-cost extension (8/1/09 to 1/31/10) was requested at the end of period 1 due to delays getting initial funding increment in place. Period 2 tasks are now on track with no changes anticipated.
- Tasks that could be expanded with additional funding:
  - We would like to investigate the use of metal-induced crystallization to form oriented (111) Si layers on glass which can be used as templates for Si wire array growth.

Future Plans (FY 2011 and beyond)

- Optimize the design of the Si pillar/wire arrays and investigate the use of light scattering approaches to enhance light absorption and increase the efficiency of the devices.

- Develop suitable silicon-on-glass templates for the vertical growth of Si wire arrays by VLS.

- Demonstrate a radial p-n junction Si wire array solar cell on quartz/glass using LPCVD or a-Si shell layers.

- Demonstrate an amorphous hydrogenated Si /crystalline Si radial junction Si pillar/wire array solar cell.

Mandatory Summary Slide

- Demonstrated increased efficiency in radial p-n junction Si pillar array solar cells fabricated using highly doped Si due to a larger optical thickness for light absorption and a shorter carrier collection length compared to comparable planar cells.

- Demonstrated that VLS growth can be used to fabricate high aspect ratio Si wire arrays at high growth rates (1-10 μm/min) using metal catalysts such as Cu and Ni (with $SiCl_4$) and Al (with SiH_4).
  - Effective cleaning methods are required to remove residual metal from the wire surface prior to device fabrication.

- Amorphous Si coating and reduced temperature VLS growth on glass under development as lower cost fabrication pathway.

Publications and Patent Applications

- “Fabrication and electrical properties of Si nanowires synthesized by Al-catalyzed vapor-liquid-solid growth,” Y. Ke, X. Weng, J.M. Redwing, C.M. Eichfeld, T.R. Swisher, S.E. Mohney and Y.M. Habib, *Nano Letters* **9**, 4494, 2009.

- “Enhanced conversion efficiencies for pillar array solar cells fabricated from crystalline silicon with short minority carrier diffusion lengths,” H.P. Yoon, Y.A. Yuwen, C.E. Kendrick, G.D. Barber, N.J. Podraza, J.M. Redwing, T.E. Mallouk, C.R. Wronski and T.S. Mayer, accepted for publication in *Applied Physics Letters* (04-30-2010).