Highly Integrated Power Module (Keystone Project #1)

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Oak Ridge National Laboratory

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Overview

Timeline

- Start – FY19
- End – FY24
- 53% complete

Barriers

- Availability and the limited field reliability data of wide band-gap (WBG) power devices
- Meeting DOE ELT 2025 High Voltage Power Electronics Targets
  - Power Density: 100kW/L
  - Cost: $2.7/kW
  - Peak Efficiency: > 97%
  - Reliability: 300,000-mile lifetime or 15 years

Budget

- Total project funding
  - DOE share – 100%
- Funding for FY21: $765K

Partners

- NREL, SNL, Virginia Tech, University of Arkansas
- Momentive, Indiana IC, and DuPont
- ORNL team members: Emre Gurpinar, Shajjad Chowdhury, Lincoln Xue and Burak Ozpineci

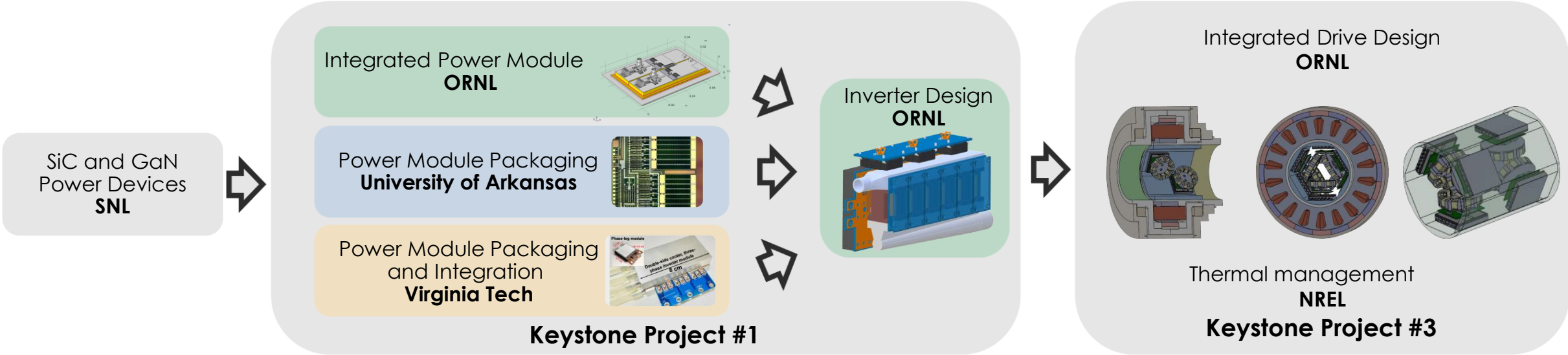
Relevance – Project Objectives

Overall Objective

Develop technologies for next generation advanced integrated power electronic systems enabling high power density and reliability to achieve DOE ELT 2025 technical targets (100kW/L, $2.7/kW, and 300,000 mile lifetime)

FY21 Objectives

- Power Module Design
  - Design and prototype Organic Direct Bonded Copper (ODBC) based power modules with integrated gate driver and cooling
- Automated Design of Power Electronics
  - Validate the performance of compact heat sinks developed with evolutionary based multi-objective optimization tool
- Device Characterization
  - Analyze switching behavior of SiC MOSFETs for different layouts and gate resistance values for inverter loss analysis



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FY21 Milestones and Go/No-Go Decision

Period	Date	Milestones and Go/No-Go Decision	Status
FY21	Q1	Milestone: • Finalize design of gate driver and heat sink integrated substrates for 100kW traction drive system	Completed
	Q2	Milestone: • Experimentally validate the performance of the genetic algorithm optimized heat sink	Completed
	Q3	Milestone: • Complete assembly of integrated substrates for 100kW traction drive systems	On-track
	Q4	Go/No-Go Decision: • If the integrate substrate performs well in dynamic and static characterizations, deliver 6 modules for 100kW traction drive system	On-track
FY22	Q1	Milestone: • Evaluate electrical performance of the power modules in a three-phase inverter	On-track
	Q2	Milestone: • Evaluate thermal performance of the power modules in the three-phase inverter	On-track
	Q3	Go/No-Go Decision: • If electrical and thermal performance evaluation is satisfactory, run the three-phase inverter with a motor emulator	On-track
	Q4	Milestone: • Run the three-phase inverter at the ORNL dynamometer setup with a high speed motor	On-track

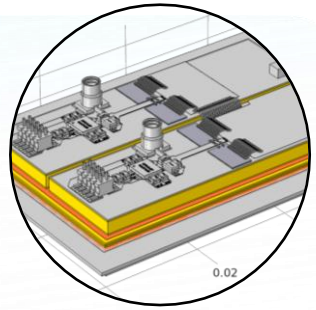
Any proposed future work is subject to change based on funding levels

Approach/Strategy

Increase power density and reliability of power electronics to meet DOE ELT 2025 targets by focusing on power electronic module research

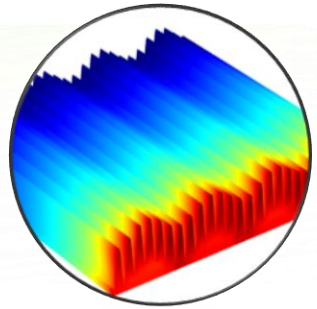
Power Module Design
Identify state-of-the-art (SOA) substrate and interconnect solutions that allow increased power density and high reliability for WBG device-based power modules via

- Improved heat extraction
- Enhanced thermal and power cycling capability
- Low electrical parasitic inductance
- Integrated gate driver, sensor and protection



Automated Design of Power Electronics
Develop novel cooling solutions for high power density by

- Exploring potential design space for individual components using evolutionary based optimization algorithms
- Generating new analysis methods for computationally efficient optimization of the system



Characterization of SiC Devices for High Power Applications
Characterize high power, high voltage SiC MOSFETs in terms of:

- Switching and conduction performance under wide operating temperature and load conditions
- Integration and thermal management in high power modules for specific device structure

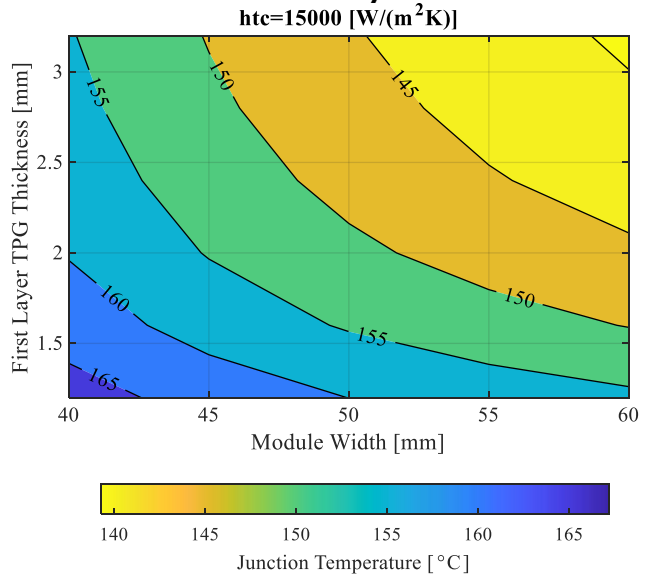


Technical Accomplishments – FY21

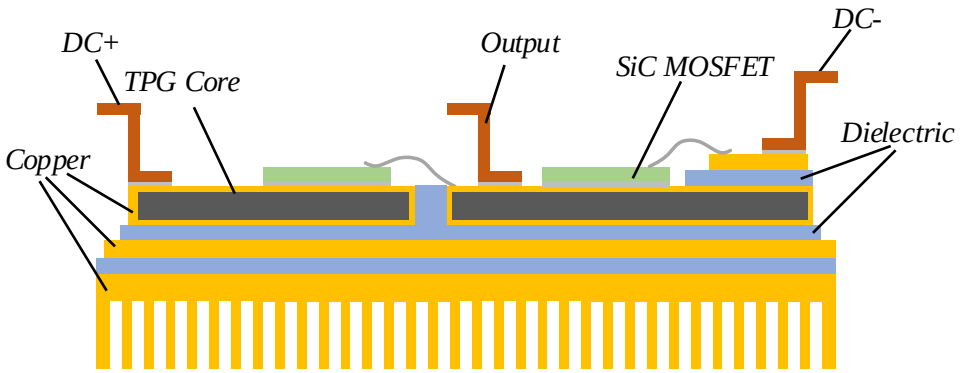
Designed SiC Power Module Based on TPG Embedded ODBC Substrate, Integrated Gate Driver, and Heat Sink

- Organic Direct Bonded Copper (ODBC) provides a multi-layer structure that enables integration of heat sink and gate driver in the power module
  - Middle copper layer provides common-mode shielding
- Thin organic film dielectric (35μm) can operate at high temperature (>175°C) and withstand high voltage (>5kV, dielectric strength=164kV/mm)
- Copper thickness can be optimized, and thermally annealed pyrolytic graphite (TPG) can be embedded for enhanced heat spreading
  - TPG has 1500W/(m×K) thermal conductivity in two axes and 10W/(m×K) in the third axis

Thermal Analysis Results

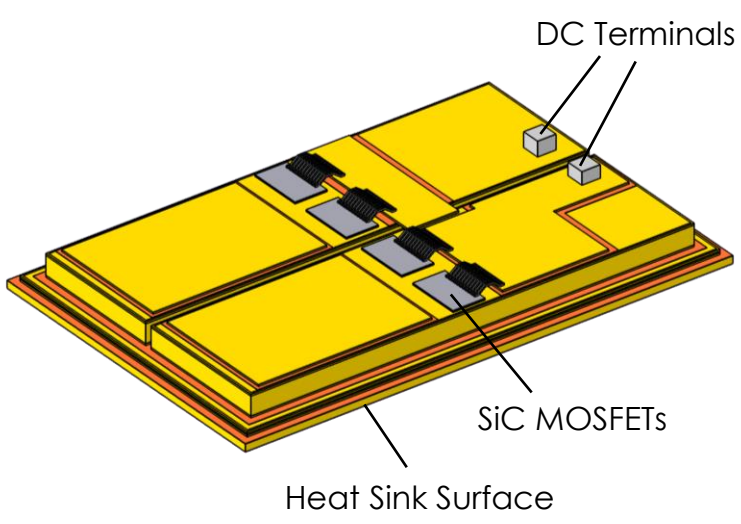


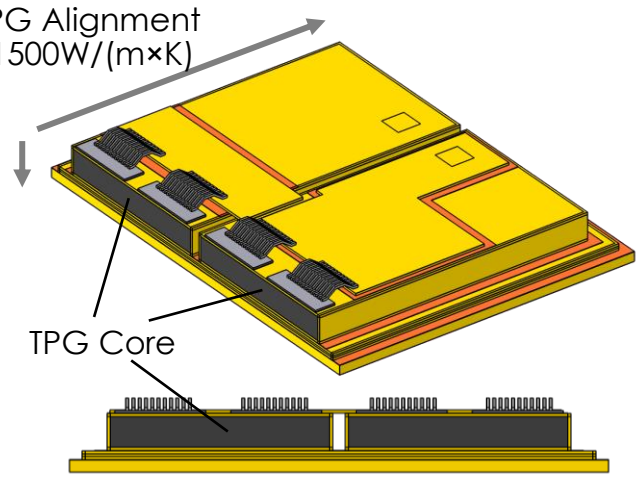
ODBC Based Integrated Power Module Concept



High power density capable substrate layout is achieved by optimizing layer thickness and TPG alignment

Final Module Layout Based on Thermal Analysis

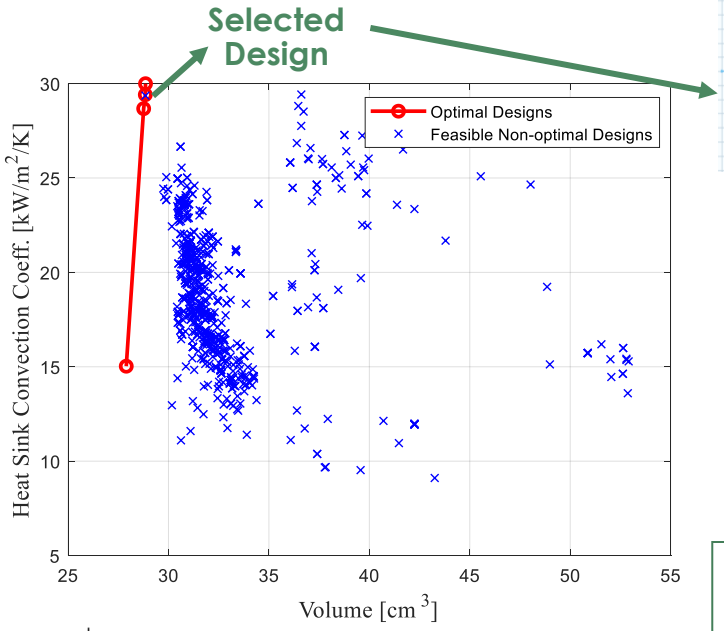


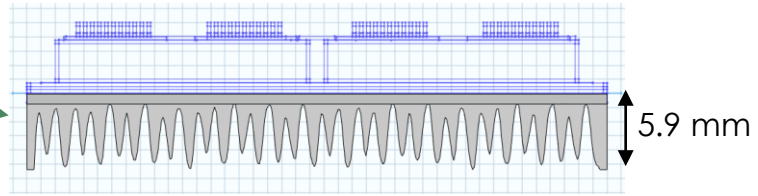


Technical Accomplishments – FY21

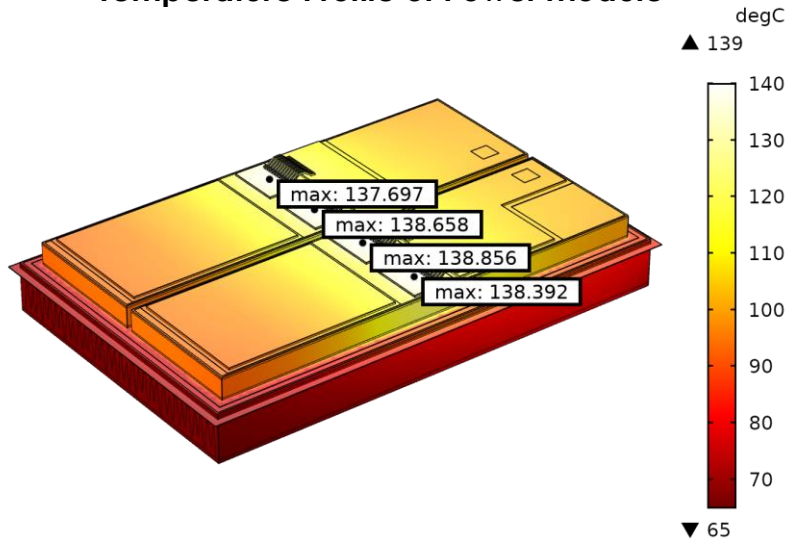
Optimized Heat Sink Geometry and Evaluated Thermal Performance

- Integrated heat sink for the ODBC based power module is designed using the genetic algorithm (GA) based multi-objective optimization tool
  - Heat load: 500W/cm^2 (~160W loss per chip)
  - Design objectives:
    - Minimize volume of the power module
    - Maximize heat sink surface to coolant heat transfer coefficient (htc)
  - Constraints:
    - Maximum junction temperature: 150°C
    - Maximum pressure drop: 2kPa
    - Flow rate: 1.66L/min

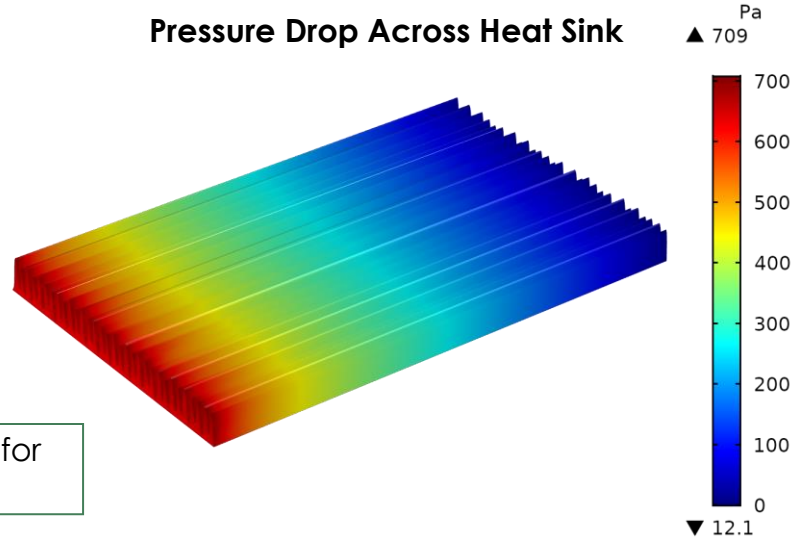




Temperature Profile of Power Module



Pressure Drop Across Heat Sink

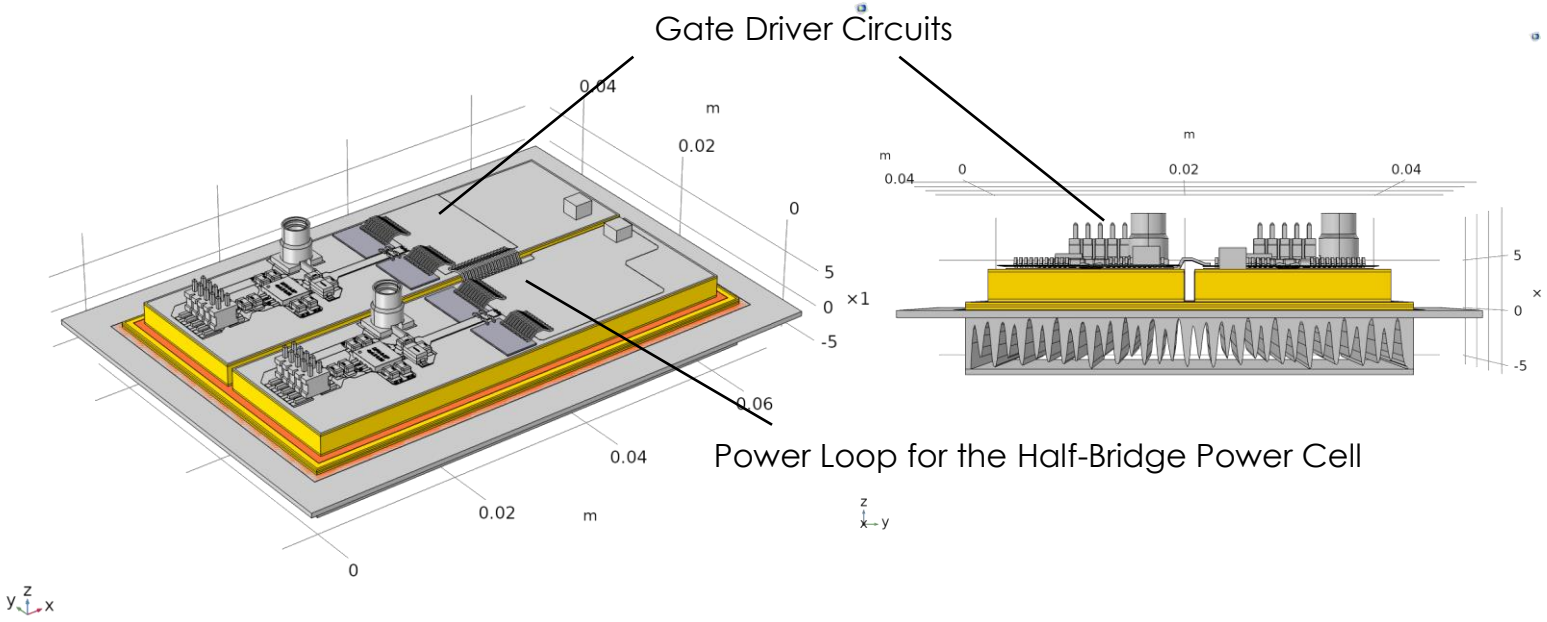


High performance heat sink optimized for the proposed layout is developed.

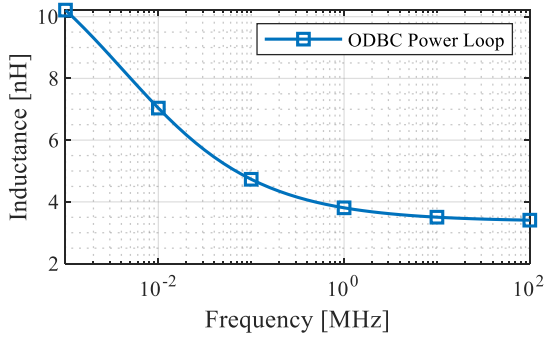
Technical Accomplishments – FY21

Designed Integrated Gate Driver, Power Loop Layout, and Evaluated Electrical Performance

- Integrated gate driver provides enhanced switching performance with:
  - Reduced parasitic inductance
  - High gate current capability (>10A)
  - Short circuit protection (<3µs)
  - Turn-on and turn-off speed adjustment with gate resistors
- Multi-layer power loop provides low parasitic inductance for the half-bridge power cell:
  - Less than 4nH power loop inductance between DC+ and DC- terminals above 1MHz
  - Reduced ringing and voltage overshoot during fast switching transients



Power Loop Inductance



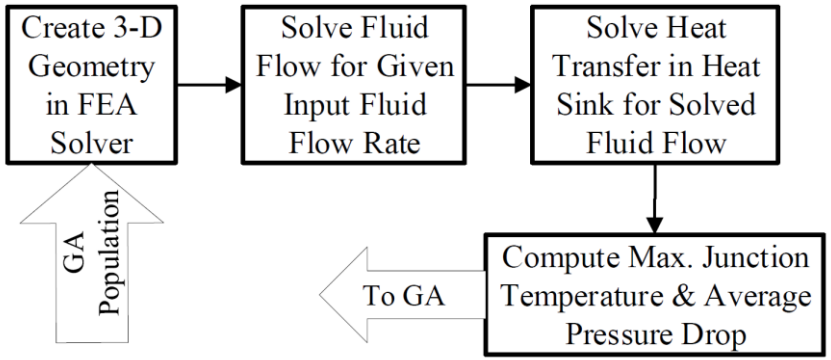
High performance electrical design is achieved via integrated gate drivers and low power loop inductance

Technical Accomplishments – FY20

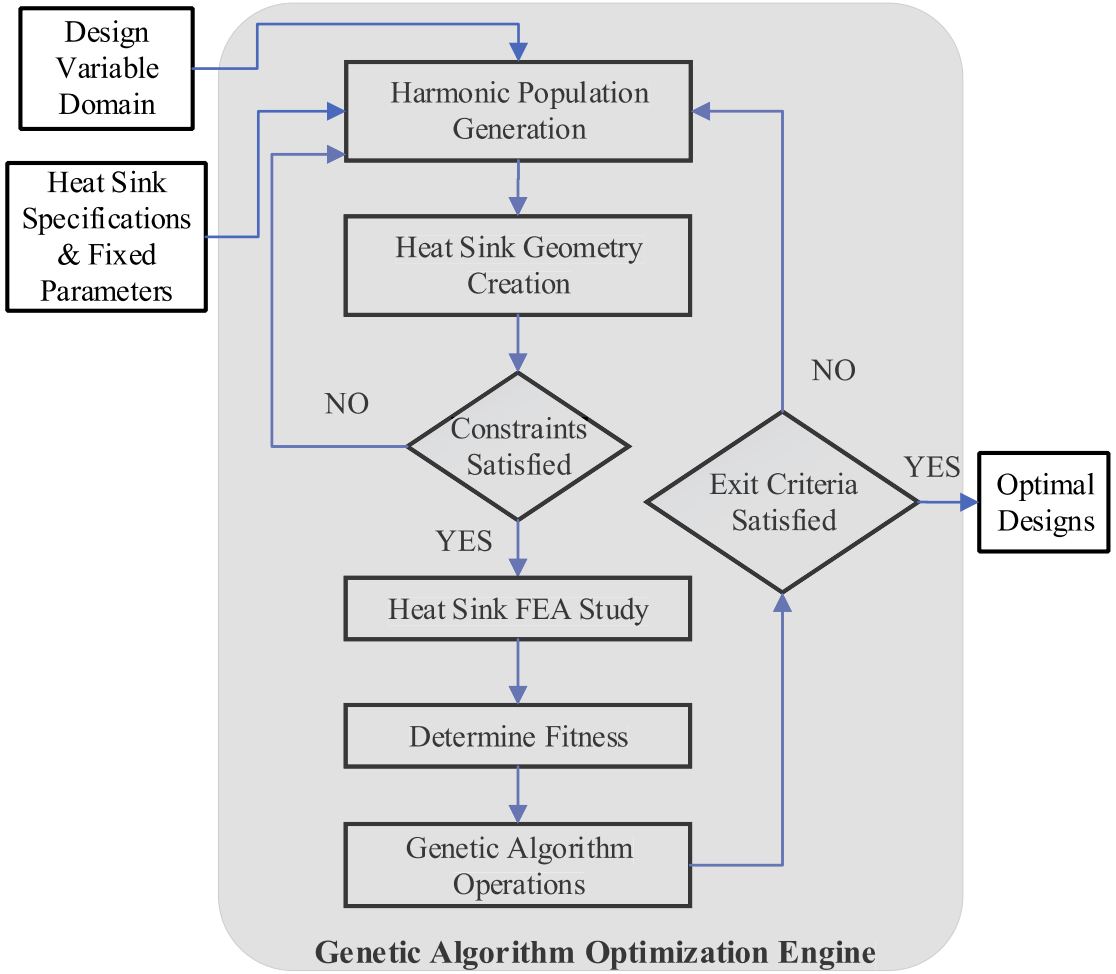
Developed Liquid Cooled Heat Sink Optimization Scheme for Automated Design for Power Electronics

- At-least 10^{60} heat sink candidates in design space: genetic algorithm (GA) utilizes ~1200 computations to find solutions
- Minimize maximum junction temperature and coolant pressure drop while satisfying physical constraints
- Constrained multi-objective optimization problem is formulated and solved using Genetic Algorithm
- Genetic Algorithm (GA) interacts with FEA simulation to evaluate heat sinks and determine best possible designs
- Developed scheme is based on Genetic Optimization System Engineering Tool from Purdue University

FEA Scheme for Design Solution and Optimization



Multi-Objective Design Optimization



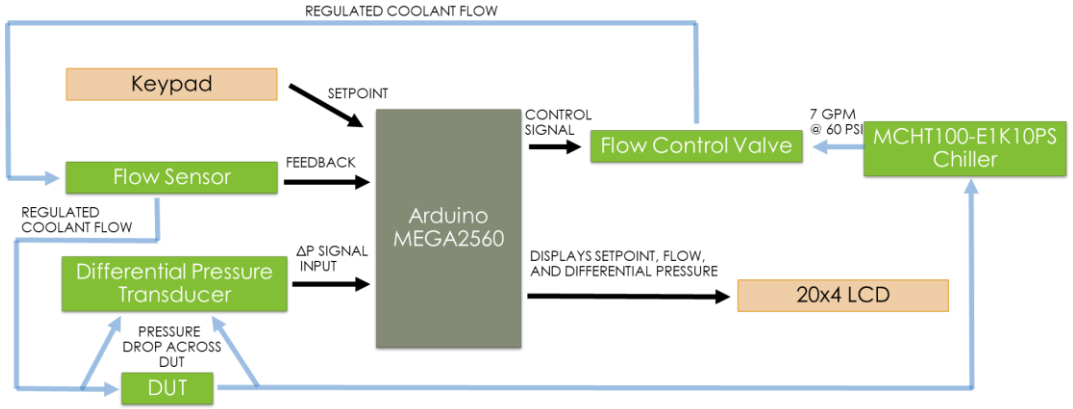
Technical Accomplishments – FY21

Developed Experimental Setup for Heat Sink Characterization

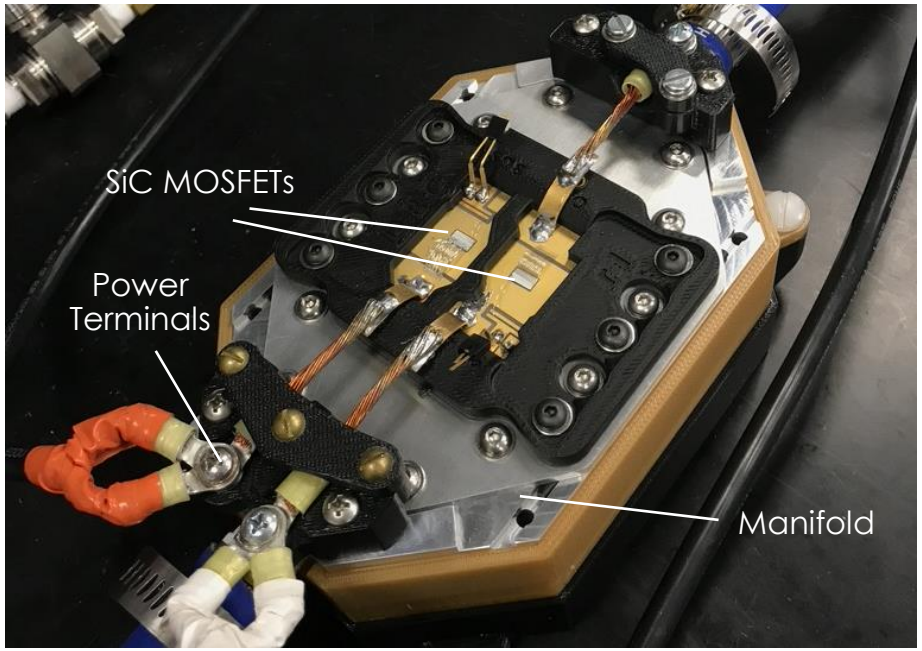
Pin Fin from BMW i3 → **50% Smaller** → **Optimized Heat Sink**



Test Setup for Heat Sink Performance Evaluation



- SiC MOSFETs, mounted on a direct bonded copper (DBC), are used as heating elements to mimic power module operation
- Flow rate, inlet and outlet temperatures, and differential pressure drop are monitored along with IR imaging of the DBC for performance evaluation

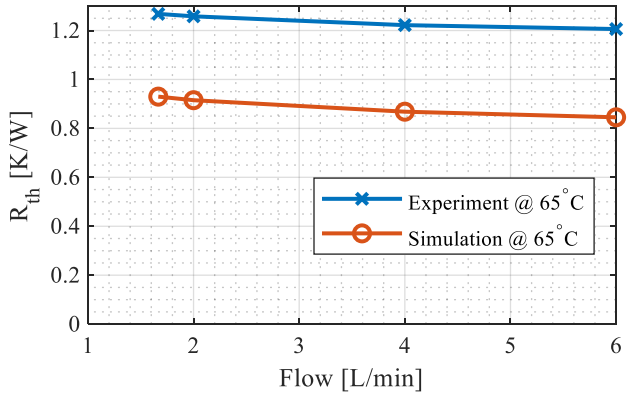


Technical Accomplishments – FY21

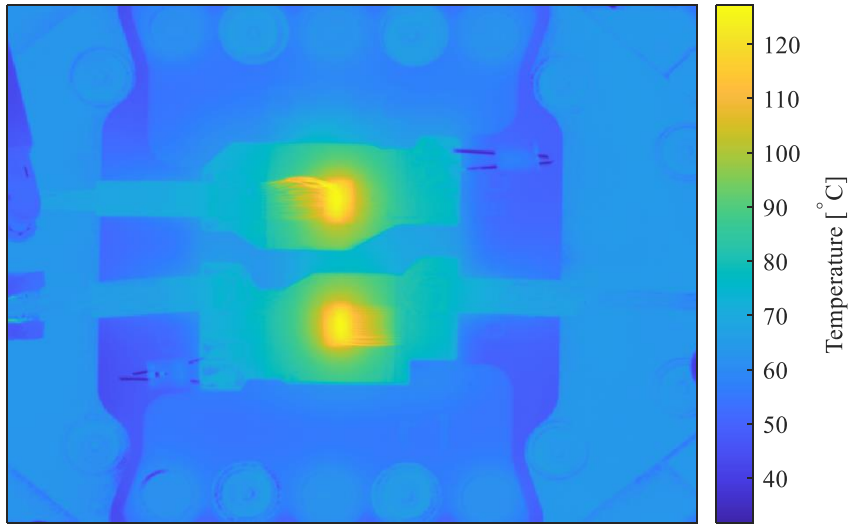
Characterized Developed Heat Sink with SiC MOSFETs and DBC

- Optimized heat sink performance is characterized at different coolant and loading conditions
  - Surface temperature of the DBC is measured with IR camera
  - Pressure drop across the manifold is measured with differential pressure transducer
- The performance of the heat sink aligns with the simulation results and validates the performance of the manufactured prototype

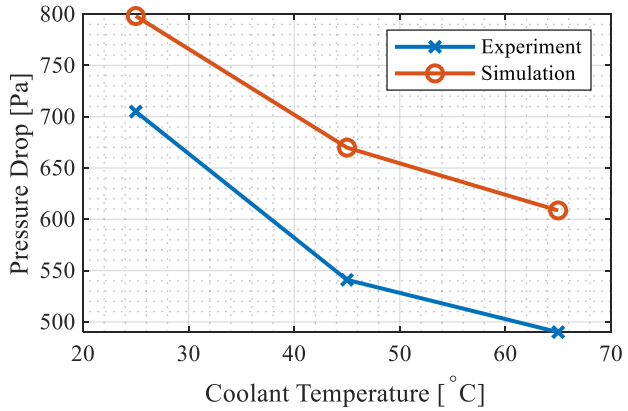
Junction to Coolant Thermal Resistance



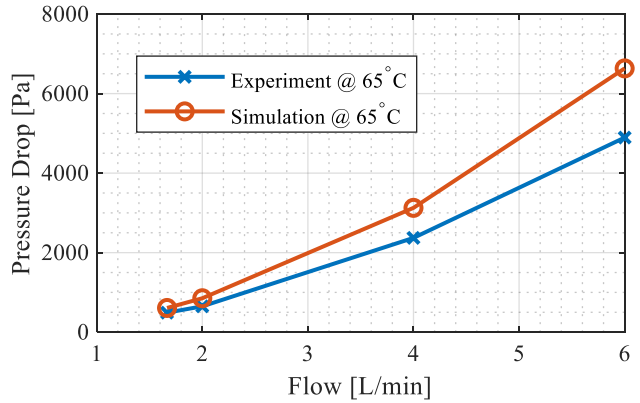
Flow: 1.66 L/min, 65°C Inlet Temperature. Load: 50W per chip



Pressure Drop Across Manifold @ 1.66L/min



Pressure Drop Across Manifold



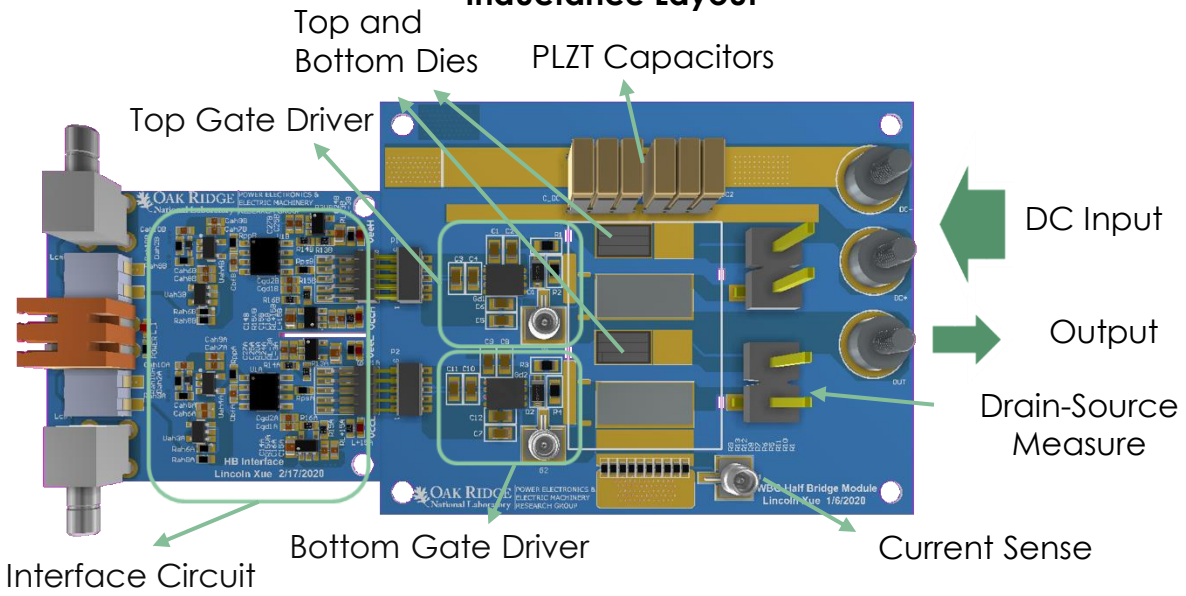
Performance of the GA optimized heat sink is validated.

Technical Accomplishments – FY21

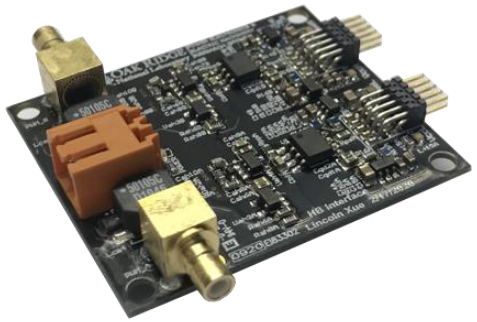
Characterized 1.2kV, 13mΩ SiC MOSFETs with Different Module Layout and Gate Performance

- For characterization of the proposed electrical layout for multi-layer ODBC with SiC MOSFET and GaN HEMT, a flexible test board is developed
  - Gate driver circuit can operate at different voltage levels according to bare die requirements
  - Protection, signal generation, and isolated power supplies are built-in to the interface circuit
- The developed test board provides a setup for switching, conduction, and EMI characterization of SiC MOSFET with different EMI shielding options

Overall System Overview of SiC Device Characterization with Low Inductance Layout



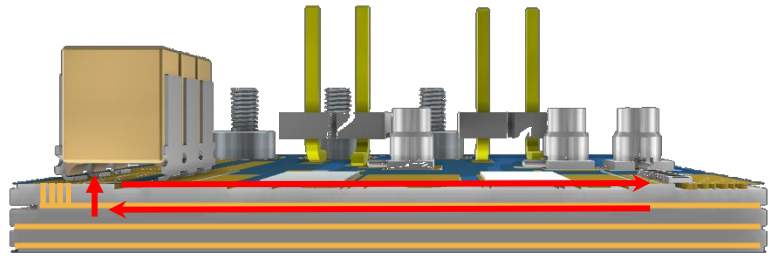
Interface Board



Power PCB with Housing



Vertical Commutation Power Loop for Low Parasitic Inductance

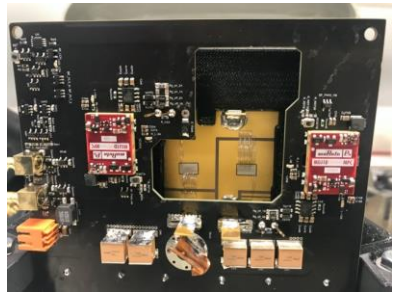


Technical Accomplishments – FY21

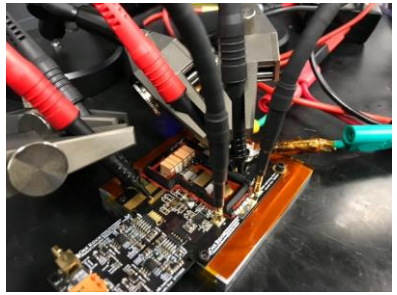
Characterized 1.2kV, 13mΩ SiC MOSFETs with Different Module Layout and Gate Performance

- Characterized the 13mΩ, 1.2kV SiC MOSFET bare dies for switching and conduction estimation in a 100kW inverter with different power loop layouts:
  - Low inductance layout, realized in a PCB for this experiment, provides cleaner switching
  - 68% reduction in voltage overshoot is achieved during switching transients

Direct Bonded Copper (DBC)

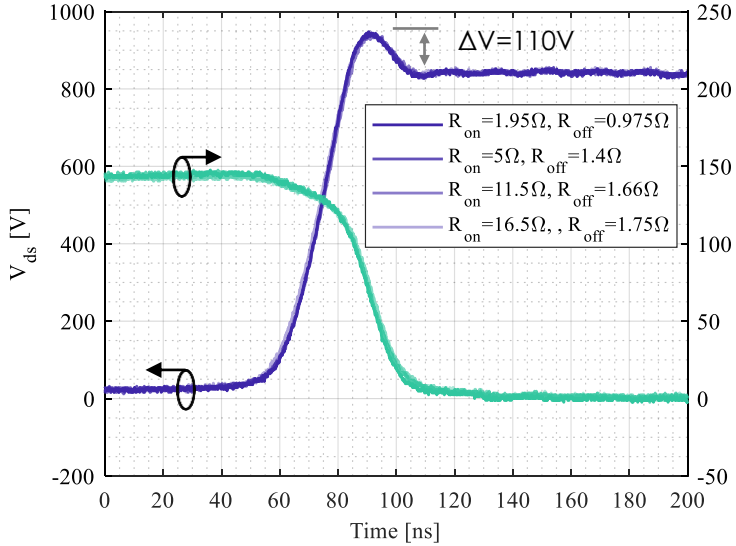


Printed Circuit Board (PCB)

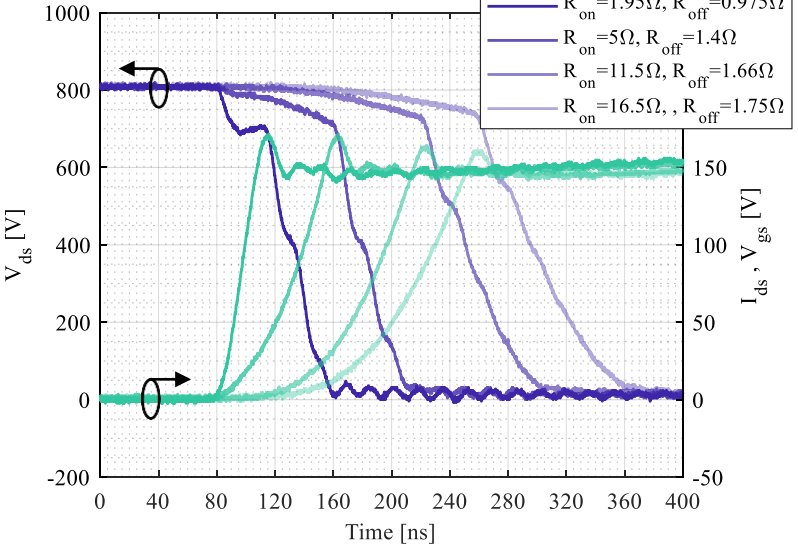


DBC

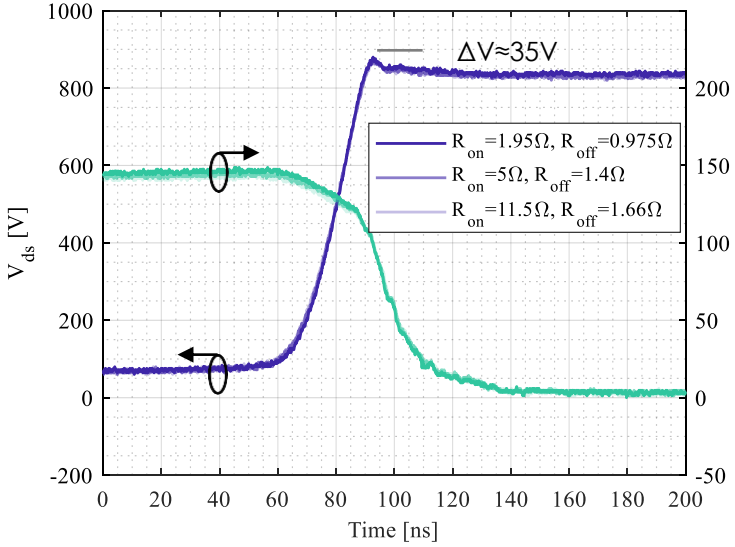
Turn-off

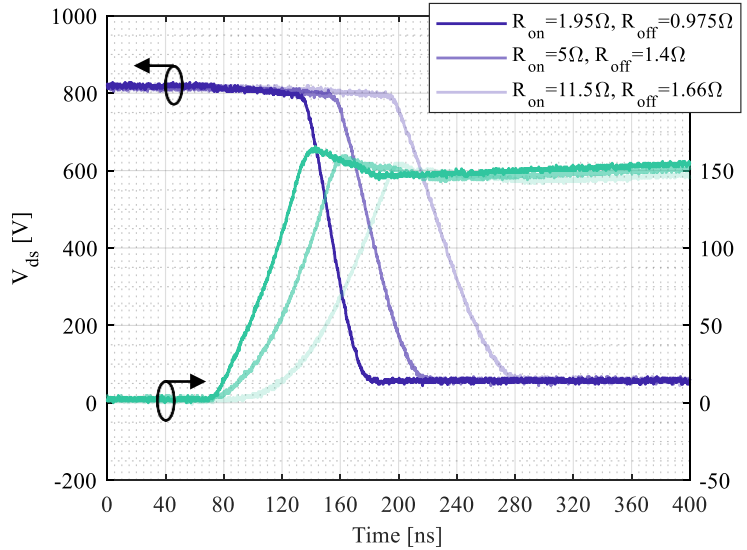


Turn-on



PCB





Responses to Previous Year Reviewers' Comments

- **Reviewer:** The hardware prototyping and test plan are good. The reviewer looked forward to hearing about the prototype test results. It might be beyond the scope of this project, but it would be even better if specific consideration were given to extending the concept in this project to the double-sided cooling.

Response: We will focus on double sided cooled packaging concepts once the single sided cooled prototypes are experimentally validated.

- **Reviewer:** The project documented well the design, simulation, and experimental results. Experimental results are not reflecting steady state temperature similar to simulation results. It would be critical to identify for evaluation the impact on the reliability objective.

Response: We are collaborating with NREL to evaluate the impact of proposed solutions (e.g. ODBC substrates) to system reliability.

- **Reviewer:** It may or may not be under the scope of this project, but the switching transient associated high-frequency oscillations on Slide 11 will sooner or later become a major concern. It might be a good idea to start giving specific thought to how to handle that from the packaging viewpoint (module parasitics and semiconductor capacitance).

Response: We are looking into low inductance structures and have shown that low inductance layout enabled by ODBC can reduce the high frequency oscillations and voltage overshoot significantly.

Collaboration and Coordination with Other Institutions

Organization	Role
NREL NATIONAL RENEWABLE ENERGY LABORATORY	Thermal Analysis of Substrates
Sandia National Laboratories	WBG Device Models and Samples
VIRGINIA TECH	Double Sided Packaging and Sintering
UNIVERSITY OF ARKANSAS	High Temperature Gate Driver IC
IIC Indiana Integrated Circuits	Quilt Packaging Interconnect Design and Manufacturing
MOMENTIVE	TPG Embedded Substrate
DUPONT	Organic DBC Material

Remaining Challenges and Barriers for FY21

- Determining prototyping options for advanced heat sink designs with copper and nickel plating
- Availability of high temperature rated (>200°C) WBG devices with gold metallization on top side for wire bondless packaging concepts
- Implementation of the heat sink optimization algorithm to cloud computing systems for reduced design time

Proposed Future Work

- Remainder of FY21
  - Complete characterization and high-fidelity modelling of heat sink prototype
  - Complete prototyping integrated power module based on multi-layer ODBC
  - Implement optimization algorithm in ORNL Compute and Data Environment for Science (CADES) Cloud computing system



https://cades.ornl.gov/

- FY22
  - Evaluate electrical and thermal performance of the traction drive system based on ODBC power modules
  - Run the ODBC based three-phase inverter with a motor emulator
  - Run the three-phase inverter at the ORNL dynamometer setup with a high-speed motor

Any proposed future work is subject to change based on funding levels

Summary

- **Relevance:** Develop technologies for next generation advanced integrated power electronic systems enabling high power density and reliability to achieve DOE ELT 2025 technical targets (100kW/L, $2.7/kW, and 300,000 mile lifetime)
- **Approach:** Develop substrate, heat sink, and integrated power module technologies to achieve high power density and reliability in next generation advanced integrated power electronic systems
- **Collaborations:** NREL, SNL, Virginia Tech, University of Arkansas, Momentive, Indiana IC, and DuPont
- **Technical Accomplishments:**
  - Developed TPG embedded multilayer ODBC substrate with integrated gate driver and liquid cooled heat sink for SiC MOSFET based traction inverter
  - Prototyped optimized heat sink architecture and experimentally validated the performance
  - Characterized 1.2kV, 13mΩ SiC MOSFET for different power loop and gate resistance configurations
- **Future Work:**
  - Prototype SiC MOSFET ODBC based power modules
  - Complete electrical and thermal characterization of the power modules and build a 100kW inverter
  - Characterize the three-phase inverter with a motor emulator and a high-speed traction motor

Any proposed future work is subject to change based on funding levels