OAK RIDGE National Laboratory

Integrated Electric Drive System (Keystone Project #3)

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Oak Ridge National Laboratory

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U.S. DEPARTMENT OF ENERGY

Overview

Timeline

- Start – FY19
- End – FY24
- 53% complete

Budget

- Total project funding
  - DOE share – 100%
- Funding for FY21: $420K

Barriers

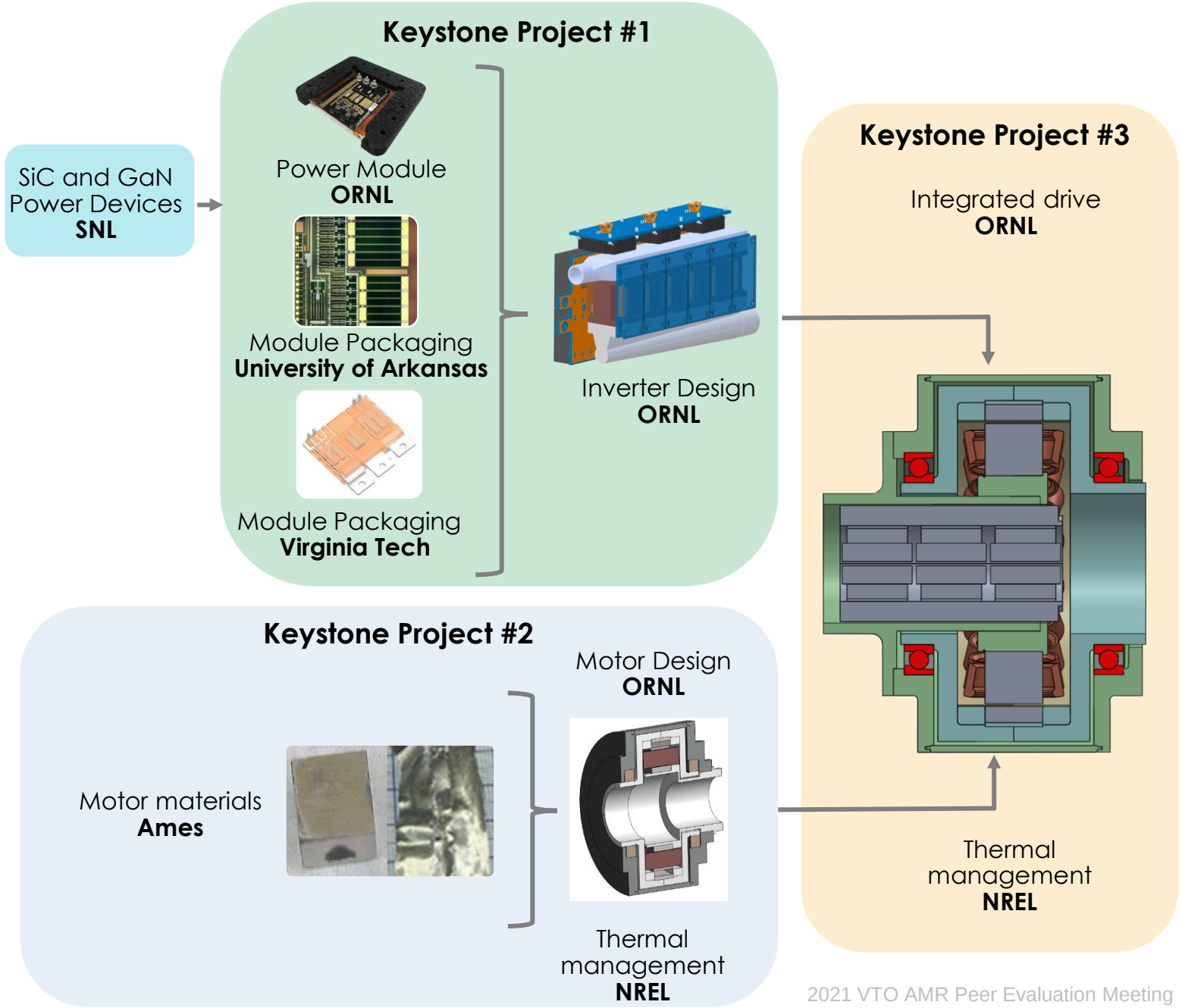
- Integration of inverter and motor to achieve high power density electric drive
- Identification, evaluation, and integration of high energy density capacitor technologies
- Meeting DOE ELT 2025 integrated drive power density target of 33kW/L

Partners

- National Renewable Energy Laboratory (NREL)
- Sandia National Laboratories (SNL)
- Ames Laboratory
- ORNL team members: Shajjad Chowdhury, Emre Gurpinar, Tsarafidy Raminosoa, Gui-Jia Su, Jon Wilkins, and Burak Ozpineci

Project Relevance

- **Overall Objective:**
  - Research technologies that will allow the integration of the inverter with the motor resulting in a high-power density integrated traction drive
  - The project results from Keystone Projects #1 and #2 will be fed into this project for an iterative approach
- **FY21 Objectives:**
  - Assess feasibility of the proposed internal stator mount integration technique
  - Evaluate capacitor packaging techniques to improve electrical performance
  - Optimize power electronic substrate area to fit inside the outer rotor motor



Milestones

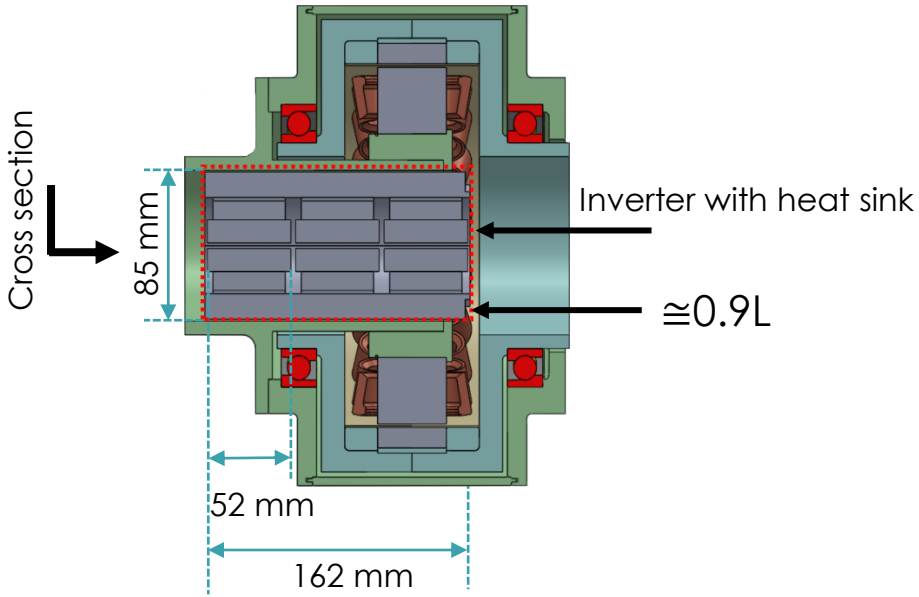
	Date	Milestones and Go/No-Go Decision	Status
FY 2021	Q1	**Milestone:** Experimentally evaluate high voltage PLZT capacitors	**Completed**
	Q2	**Milestone:** Optimize capacitor packaging to complement wide bandgap devices while keeping the electric drive power density within consortium target	**Completed**
	Q3	**Milestone:** Optimize power module area and identify cooling solutions for the inverter to integrate with the outer rotor motor	**On track**
	Q4	**Go/No-Go Decision:** If power module and heatsink fits inside the available volume then start designing other inverter components	**On track**

	Date	Milestones and Go/No-Go Decision	Status
FY 2022	Q1	**Milestone:** Build a test setup to evaluate current sensors and select one to optimize volume	**On track**
	Q2	**Milestone:** Prototype and evaluate optimized substrate	**On track**
	Q3	**Milestone:** Develop a single-phase power module integrating, gate drivers, current and voltage sensors, busbars, and connectors	**On track**
	Q4	**Go/No-Go Decision:** If the developed module fit inside the motor, then start building the six-phase inverter for integration	**On track**

Any proposed future work is subject to change based on funding levels

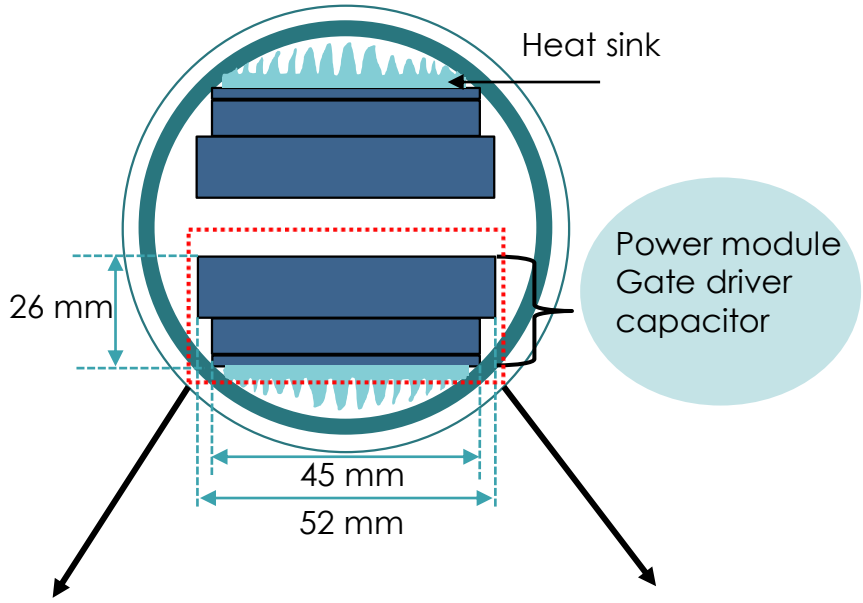
Approach/Strategy

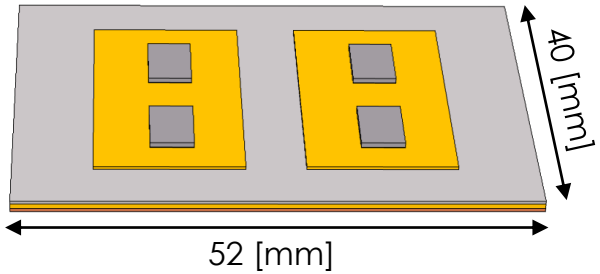
- Assess internal dimensions for outer rotor motor for power electronics integration
- Identify required capacitor parameters and then design and characterize capacitor packages to fit inside the available space while optimized for performance
- Evaluate required cooling performance for the power module and estimate minimum dimensions to keep the device temperature within the manufacturer specified limits



Internal stator mount integration for outer rotor motor

Inverter cross section





Analyze a DBC based power module to calculate the required cooling performance



Select, characterize, and package capacitors

Any proposed future work is subject to change based on funding levels

Technical Accomplishments – FY21

Cooling system design for the proposed integrated drive– ORNL and NREL collaboration

ORNL and NREL are working together to understand the impact of integrating inverter with the motor to achieve high power density target

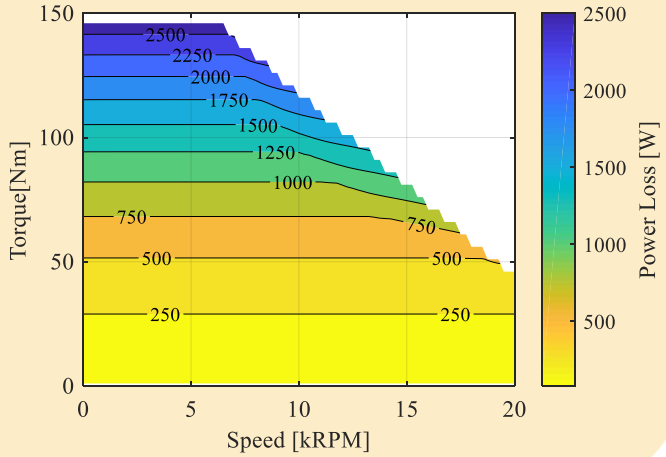
ORNL

- Proposed internal stator mount integration solution to achieve DOE 2025 target
- Identified motor currents, voltages, and phase angles for the full operating range
- Estimated inverter losses based on 1.2kV SiC MOSFETs

Internal stator mount integration

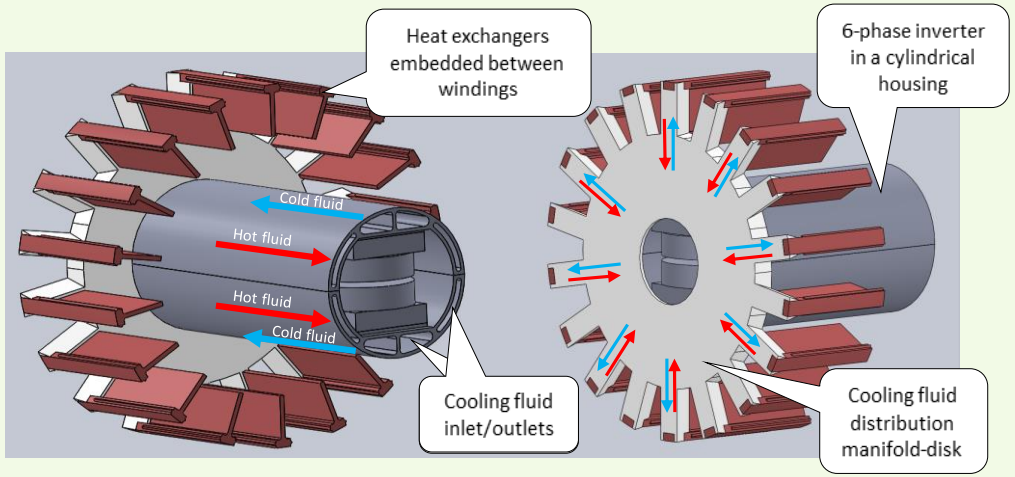


Inverter loss



NREL

Developed cooling concepts for the proposed internal stator mount integration technique



Designed heat exchanger for motor and inverter cooling for internal stator mount integrated drive

Designed heat exchanger for internal stator mount integration **Bidzina Kekelia and Emily Cousineau – NREL**

Technical Accomplishments – FY21

Developed an analytical model of the outer rotor motor

Steady-state surface mount PM-motor model for loss estimation

When $I_d = 0$, Phase current

$$T_e = \frac{3}{2}\frac{P}{2} i_q \Psi_m$$

$$I = i_q = \frac{T_e}{\Psi_m}\frac{2}{3}\frac{2}{P}$$

Phase voltage

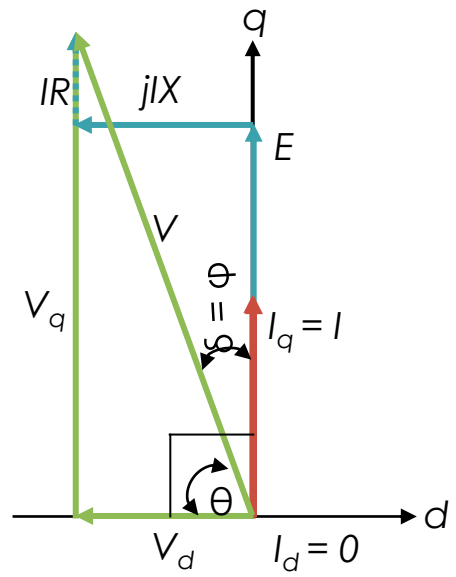
$$V_d = i_d R \times L_d \frac{di_d}{dt} - \omega_e L_q i_q$$

$$V_q = i_q R \times L_q \frac{di_q}{dt} + \omega_e L_d i_d + \omega_e \Psi_m$$

$$V = \sqrt{\left(-\omega_e L_q i_q\right)^2 + \left(i_q R + \omega_e \Psi_m\right)^2}$$

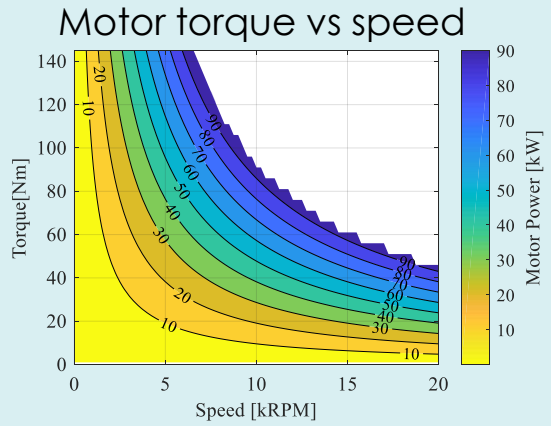
Power factor

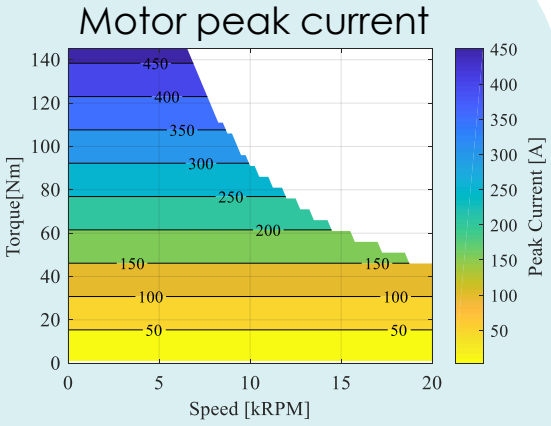
$$\varphi = 90 - cos^{-1}\left(\frac{V_d}{V}\right)$$

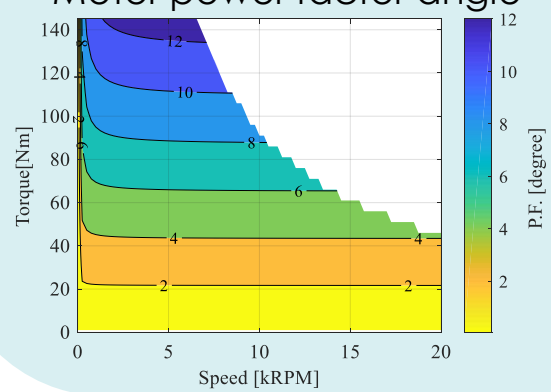


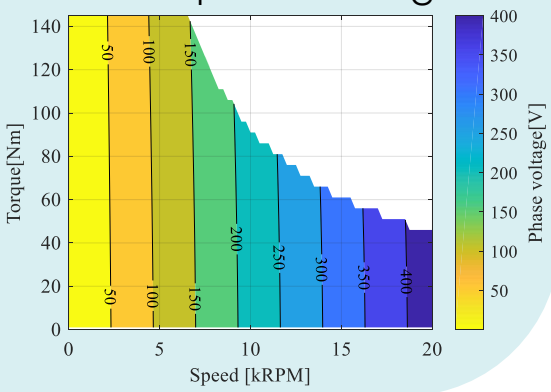
Motor phasor diagram

Results









Maximum current [475A] and maximum phase angle occurs at 6.6kRPM at 100kW power.

Technical Accomplishments – FY21

Calculated inverter loss

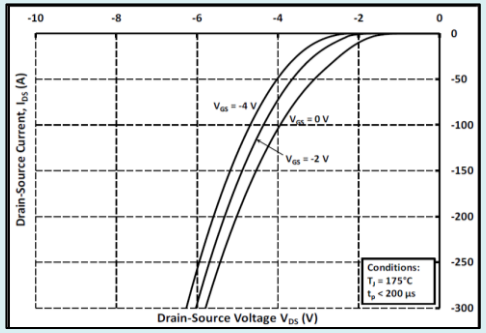
Device selection and loss estimation for segmented inverter

- Selected 1200V, 17mohm SiC MOSFET dies
- Paralleled two devices to handle the required motor current
- Used datasheet conduction losses for loss evaluation
- Calculated switching losses using experimental results

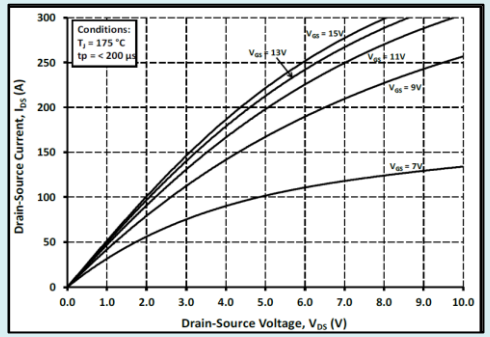
Device parameters

Parameters	Die	Unit
Blocking voltage, V_{DS}	1200	V
R_{DS} @ 150°C	19.5	mΩ
I_{DS} @ 100°C case	102	A
DC bus, V_{dc}	800	V
Switching, f_{sw}	30	kHz
Die temp, T_j	150	°C

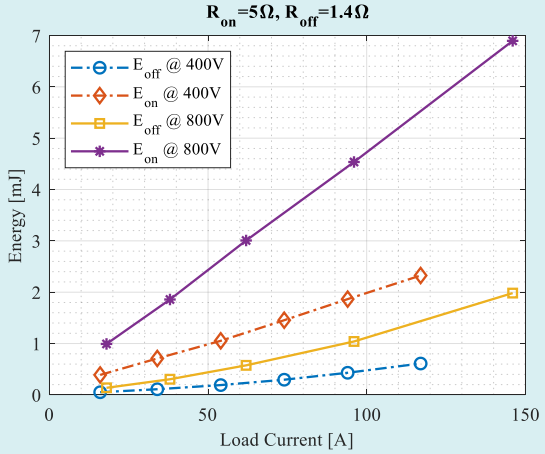
Diode forward characteristics[1]



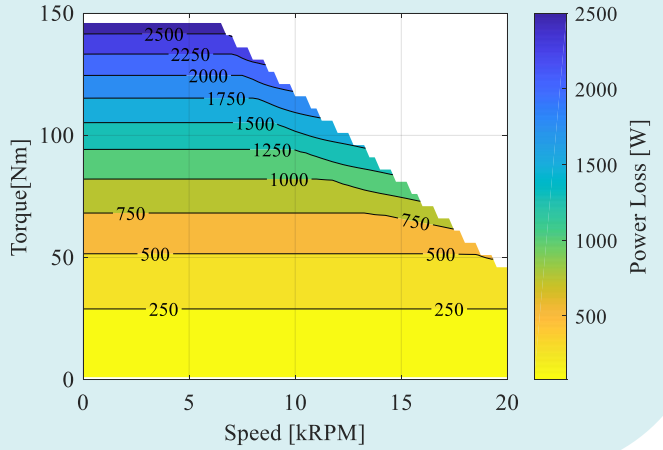
MOSFET forward characteristics[1]



Switching losses



Total inverter loss



Maximum estimated inverter loss is 2500W for a 100kW system. Including a safety margin, 3000W will be considered for cooling system design.

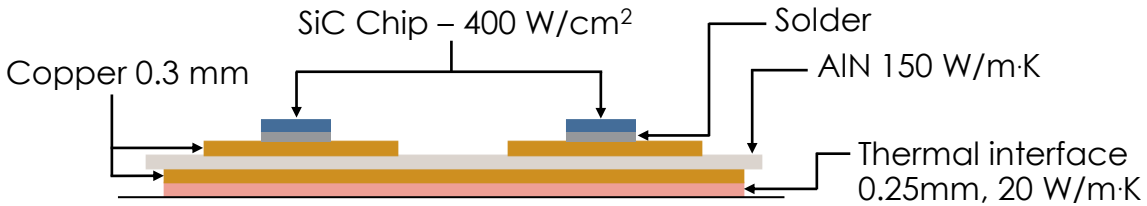
[1]https://www.wolfspeed.com/downloads/dl/file/id/1662/product/659/cpm3_1200_0013a_external_version.pdf

Technical Accomplishments – FY21

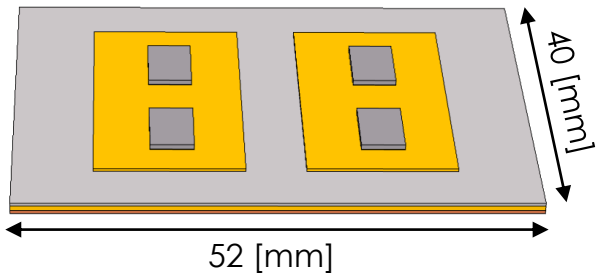
Identified cooling requirements of the power module

Direct bonded copper (DBC) based power module

- Designed a half bridge module considering two dies in parallel
- Utilized an AlN based ceramic insulator to achieve low thermal resistance
- Soldered SiC MOSFETs on the substrate

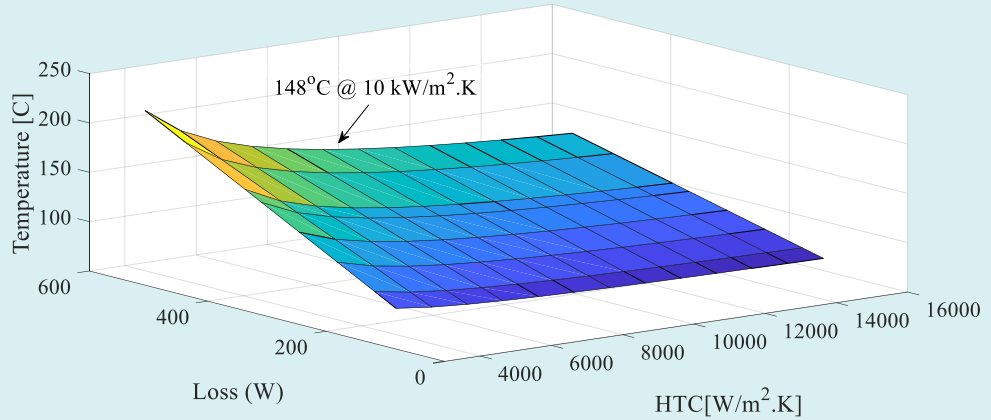


DBC structure considered for FE simulation

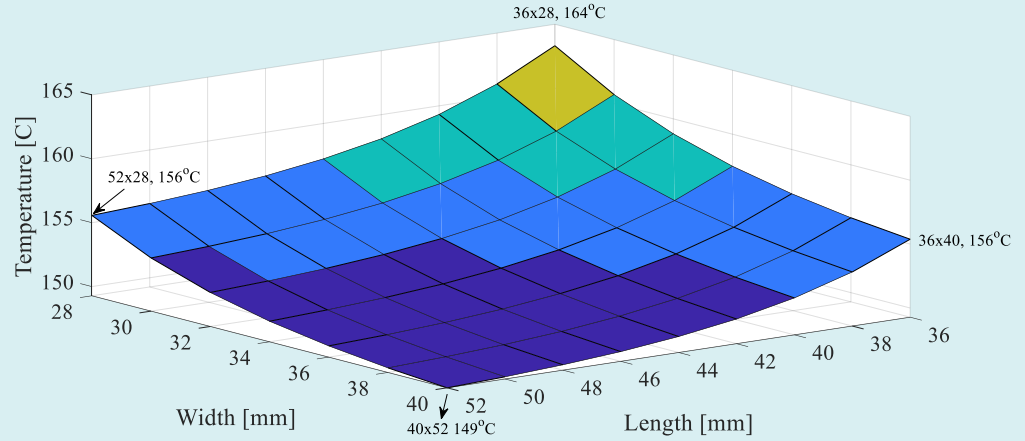


Designed substrate to estimate required heat transfer coefficient (HTC)

Device temperature with HTC



Device area with temperature @ 10kW/m²·K



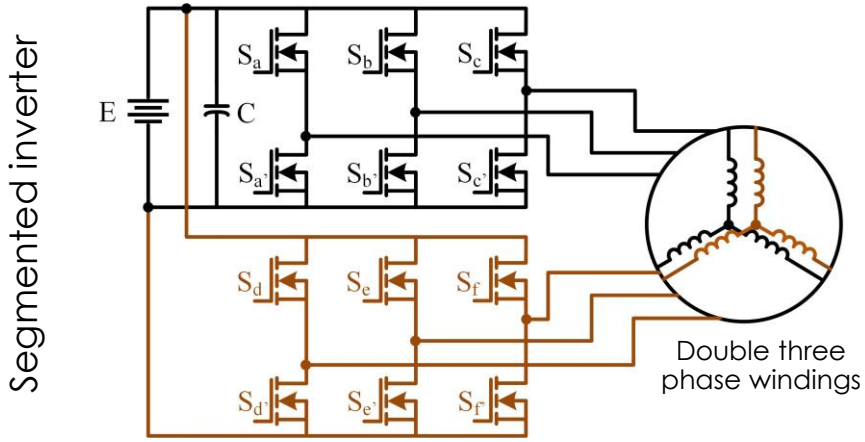
Substrate's length and width are varied without changing device location to understand the thermal impact on MOSFETs

The module requires 10kW/m²·K to keep the device temperature at 150°C.

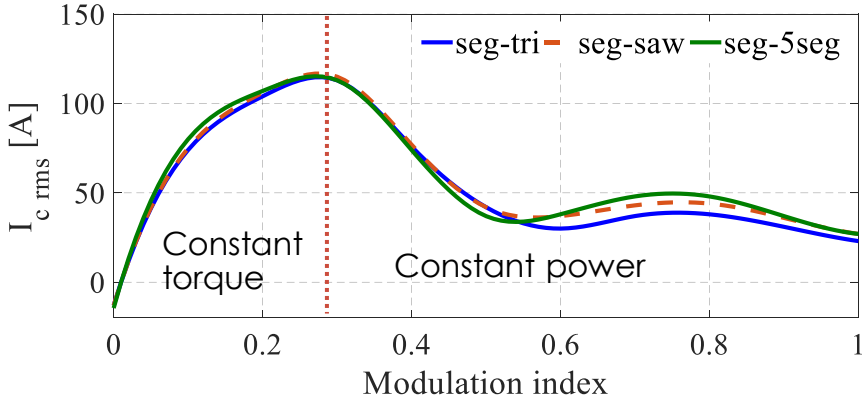
Technical Accomplishments – FY21

Evaluated capacitor current requirements

A segmented inverter reduces capacitor current stress significantly; thus, utilized for this project

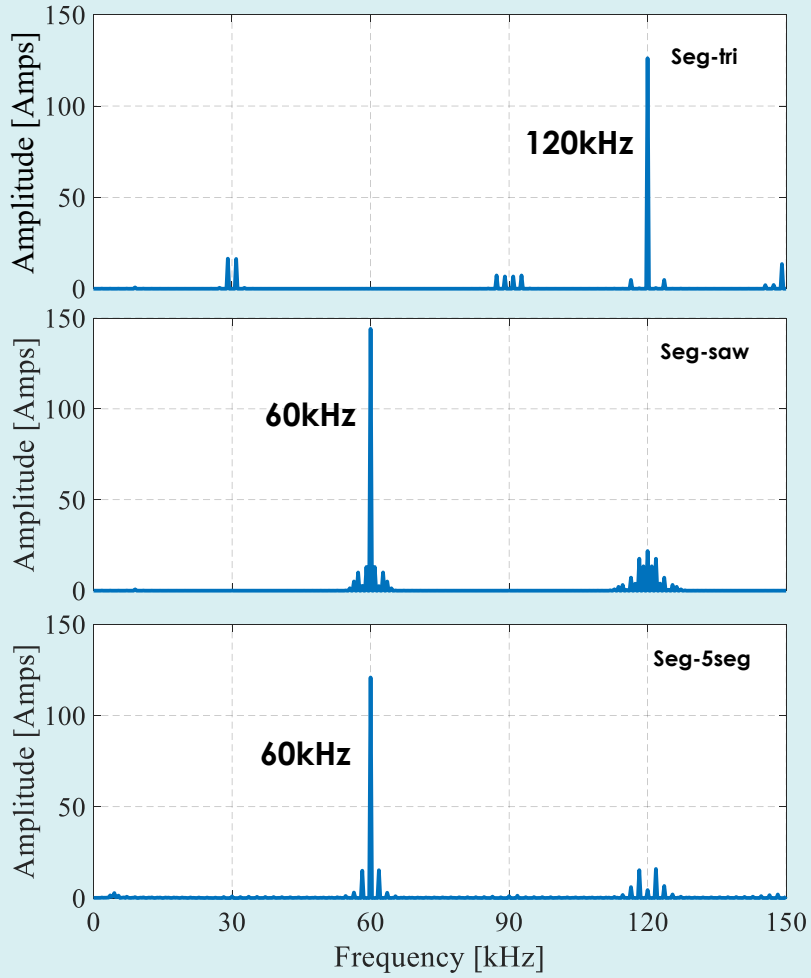


Capacitor current stress



Seg = Segmented inverter
Tri = Triangular modulation
Saw = Sawtooth modulation
5seg= 5segment/ discontinuous/ bus clamped SVPWM

Capacitor current FFT



DC link current components are at 120kHz for triangular modulation; thus, capacitance requirement will be minimum.

Technical Accomplishments – FY21

Estimated capacitance for the segmented inverter

Total capacitor current

$$i_c = C\frac{dV}{dt}$$

$$\int i_c\, dt = CV = Q$$

$$Required\ capacitance, C = \frac{\int i_c\, dt}{V}$$

Where, V is the ripple voltage which is defined by user, $\int i_c$ is constant if load current, power factor, and modulation index are fixed

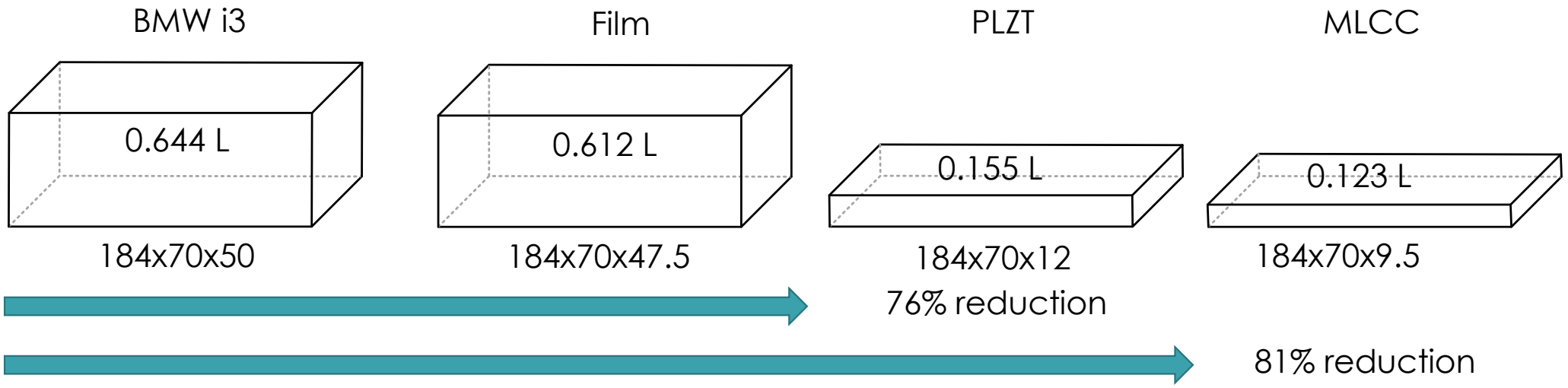
Required DC link capacitance various topologies and modulation techniques

Topology	Modulation	Maximum RMS current for all frequency	Capacitor current frequency	Required Capacitance at 5% voltage ripple
Segmented	Triangular	113 A	120kHz	15 μF
	Sawtooth	115 A	60, 180kHz	25 μF
	Bus clamped SVPWM	113 A	60kHz	21 μF
Three phase	Triangular	198 A	60, 120kHz	38 μF
	Sawtooth	225 A	30, 60, 90kHz	82 μF
	Bus clamped SVPWM	204 A	30,60kHz	73 μF
	Symmetrical SVPWM	198 A	60, 120kHz	35 μF

Segmented inverter with triangular modulation requires a minimum of 15 μF capacitance and will have to handle 113A @ 120kHz frequency. High frequency operation will also ensure minimum capacitor losses.

Technical Accomplishments – FY20

Selected capacitor technology



	Film	PLZT	MLCC – Class II
Dielectric	Metalized Polypropylene	PLZT	$BaTiO_3$
Temperature	105°C	150°C	125°C
Structure		Series Parallel	Parallel
Current handling capability	3 Amps @ 50 kHz, 85°C 0 Amps @ 50 kHz, 105°C	8 Amps @ 50 kHz, 85°C 6.5 Amps @ 50 kHz, 105°C	5 Amps @ 50kHz, 85°C 3.5 Amps @ 50kHz, 105°C

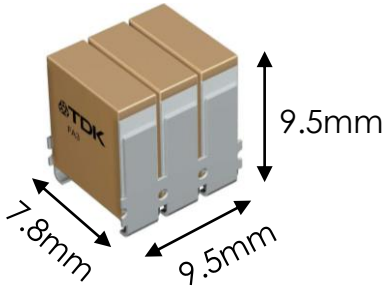
PLZT capacitor has slightly higher volume than the MLCC for a given capacitance but can handle higher current, temperature, and has better reliability.

Technical Accomplishments – FY21

Characterized high voltage PLZT capacitor - experimental setup

Evaluation of PLZT capacitors requires a test rig with

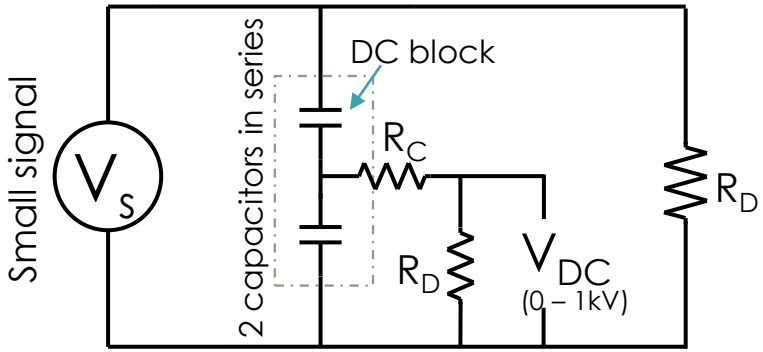
- Two capacitors connected in series
- DC bias range of 0V – 1KV
- Temperature range -25°C – 150°C
- Frequency range 5kHz – 30MHz



PLZT capacitor[1]

High voltage measurement technique

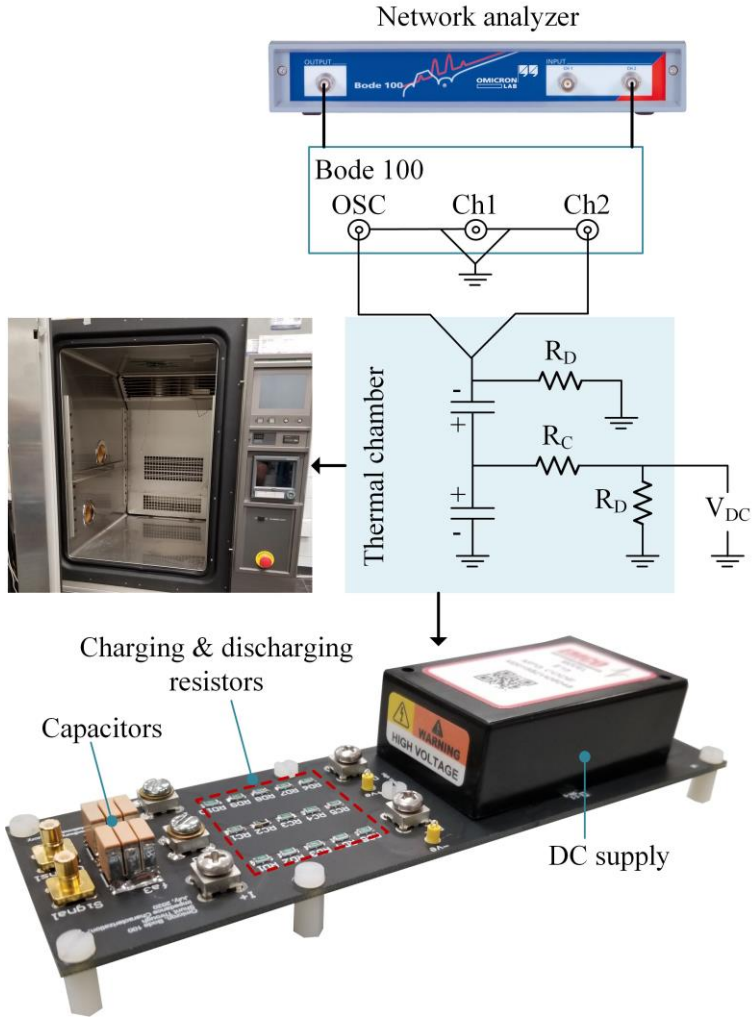
Two port shunt through measurement



R_C = Charging resistor
R_D = Discharging resistor
V_{DC} = DC Bias voltage
Small signal = 1V p-p

Modified two-port-shunt-through method to characterize capacitors with high voltage bias

Experimental setup for capacitor characterization



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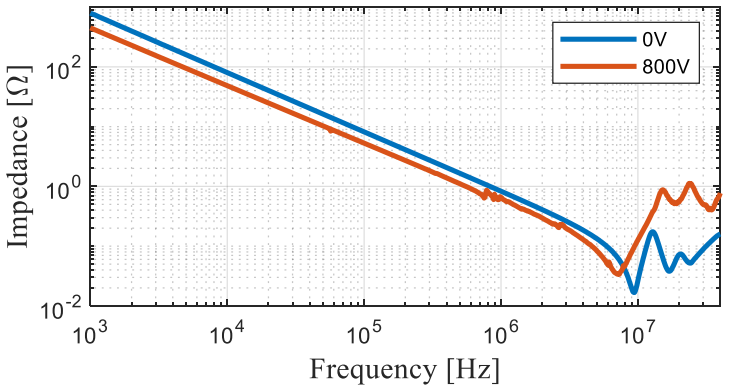
[1] https://www.tdk-electronics.tdk.com/inf/20/10/ds/B58035_FA.pdf

Technical Accomplishments – FY21

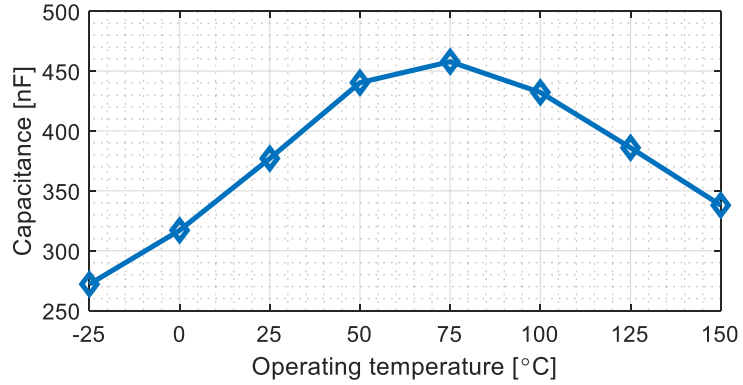
Characterized 800V PLZT capacitor – experimental results

- Impedance curves show the variation of capacitance at different bias voltages
- Maximum capacitance is 0.45 μF which is 40% less than datasheet capacitance value
- Minimum capacitance is 0.25 μF at -25°C and maximum is 0.45 μF at 75°C
- Equivalent series resistance (ESR) increases with DC bias but decreases with temperature; thus, high temperature operation is preferable
- Each capacitor can conduct 11Amps at 85kHz frequency

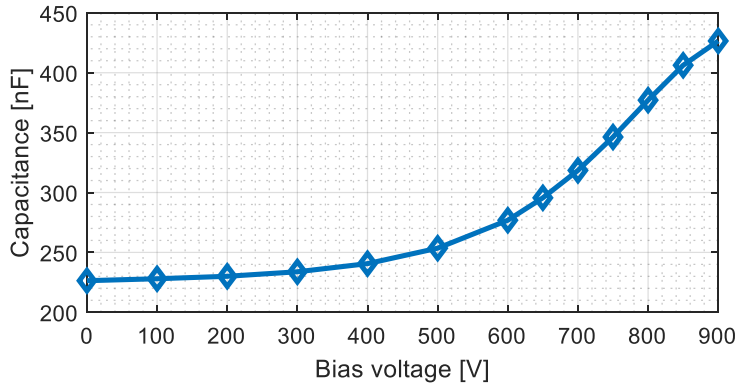
Impedance at 0V and 800V bias voltage



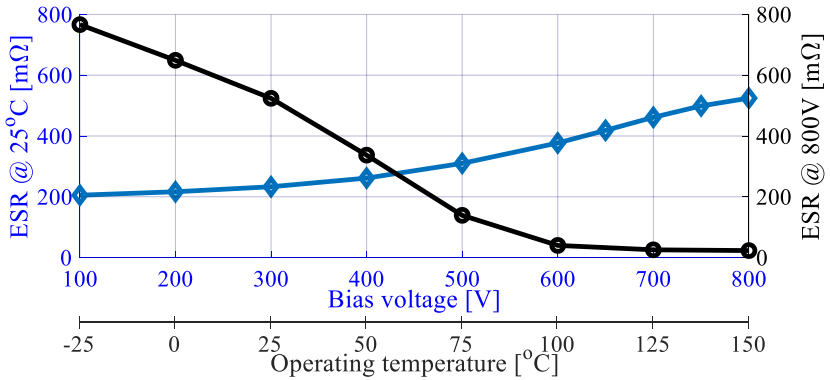
Capacitance with temperature



Capacitance with bias voltage



Change in ESR with voltage and temperature



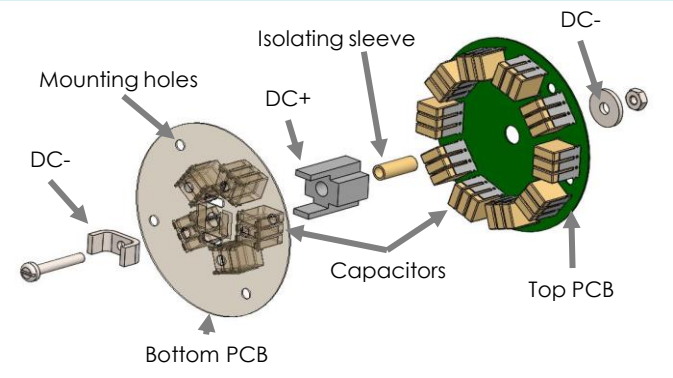
Minimum sixty (60) capacitors are required to achieve the 15 μF capacitance for the segmented inverter with sine triangular modulation scheme

Technical Accomplishments – FY21

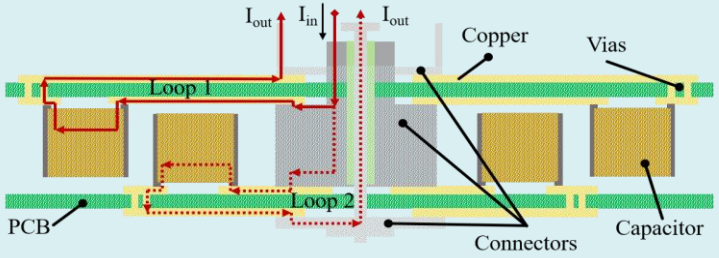
Optimized capacitor packaging – improved fill factor for circular design

- Designed a circular capacitor to fit each power module – six of them will be used in the segmented inverter
- Packaged considering 52mm x 52mm dimensions – circular capacitor

Circular capacitor package

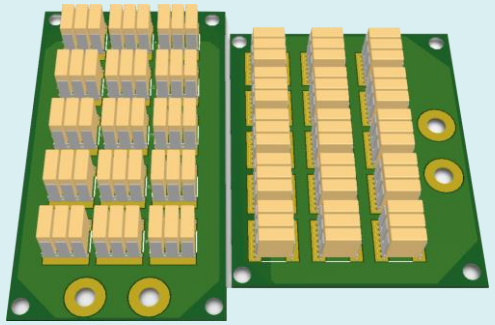


Exploded diagram of the designed circular package

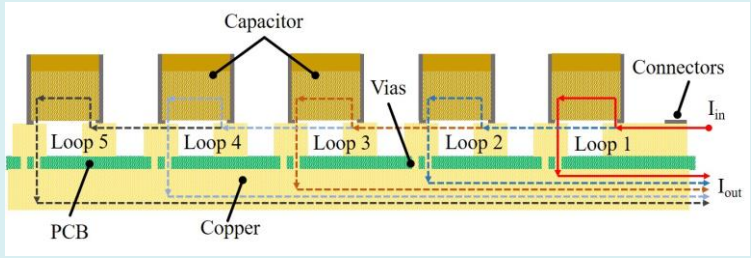


Cross section showing two identical current loops

Traditional flat capacitor package



Flat capacitor boards containing 15 capacitors



Cross section showing several current loops

Circular design has better flux cancellation due to overlapping current path and has improved fill factor than a traditional flat design (fill factor: 35% for circular and 27% for flat design)

Technical Accomplishments – FY21

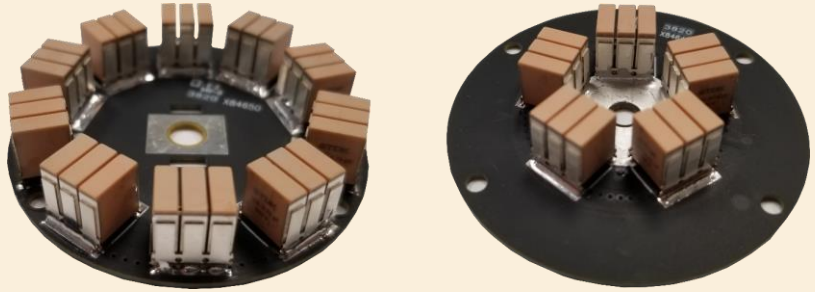
Designed and assembled packaged capacitors

- Designed considering outer rotor motor dimensions
- Built two traditional flat boards for performance evaluation and comparison
- Assembled all three packages with 15 capacitors in parallel

Circular capacitor board components



Connectors and terminals



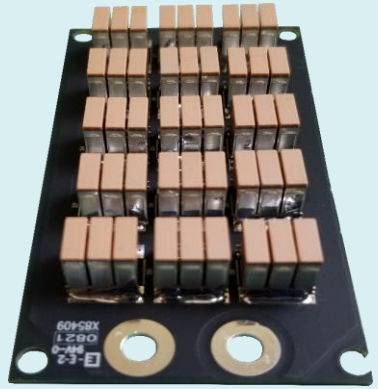
Top board

Bottom board

Assembled flat capacitor boards

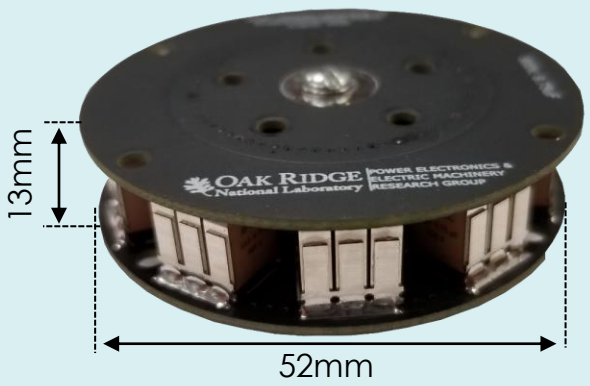


3x5 arrays

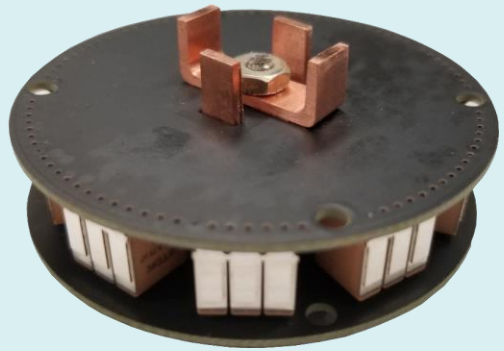


5x3 arrays

Assembled circular capacitor board



Top view



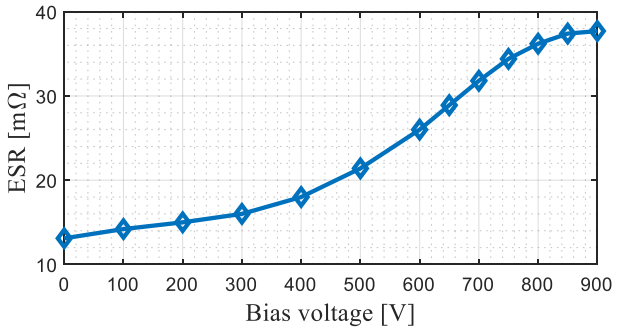
Bottom view

Technical Accomplishments – FY21

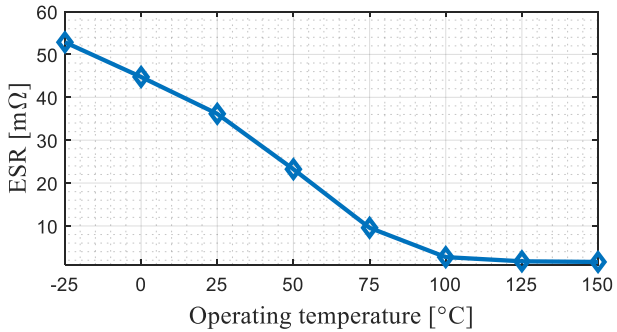
Characterized circular capacitor

- Characterized for various operating voltages and temperatures
- Achieved best results at 800V bias and100°C operating temperature

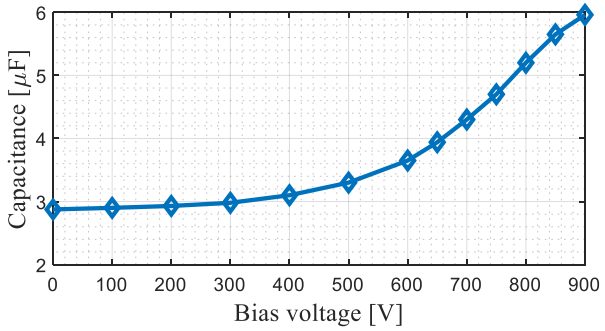
ESR with bias voltage



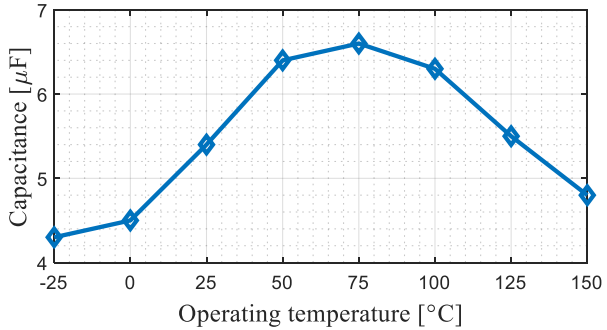
ESR with temperature



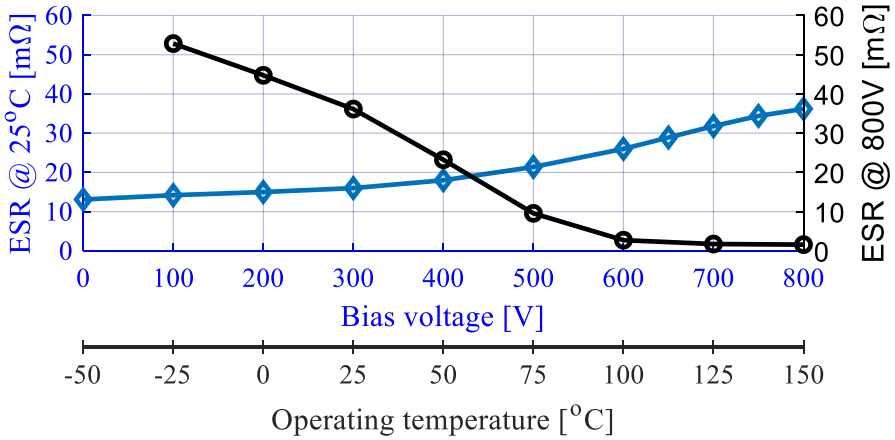
Capacitance with bias voltage



Capacitance with temperature



Change in ESR with bias voltage and temperature



Designed circular capacitor parameters

Parameters	Values	Comments
Volume	0.028*L*	Total 0.168L
Capacitance	$4.2\mu F - 6\mu F$	50*kHz*, 100°C
Theoretical current	More than 100 A	85*kHz*, 25°C [from datasheet]
Required current	20 A	Segmented inverter
Equivalent series resistance (ESR)	2.73$m\Omega$	50*kHz*, 100°C
Equivalent series inductance (ESL)	3.78*nH*	10*MHz*

The designed capacitor has minimum capacitance of 25 μF and occupies only 0.17L volume for the segmented inverter.

Response to the Reviewer's Comments

- **There is good collaboration. Would industry or university partners help the cause?**
  - Thank you for your comment. We are currently collaborating with several national labs and universities within the consortium. We are also discussing with companies to start collaborations.

- **Assessing the impact of stator heat on the inverter components will be a critical step toward successfully executing this concept architecture. Capacitor packaging will also be a key next step. So future plans as stated are sound.**
  - Thank you for your comment. We are currently collaborating with NREL to assess the impact of stator heat flux on the inverter and presented some results showing the positive effect of higher temperature on capacitor parameters.

- **The reviewer stated that this is a review of existing know-how and reports, followed by simulation and prototyping to obtain power-dense drivetrain system—it looks like an appropriate approach for this project.**
  - Thank you for your comment. We are looking into component level volume minimization and tight integration techniques to minimize the overall traction drive volume. One of the major outcomes is the minimization of the DC link capacitor to 0.17L compared to 0.6 liter for 2016 BMW-i3's traction drive capacitor.

Collaboration

Organization	Type of Collaboration
NREL NATIONAL RENEWABLE ENERGY LABORATORY	Working on thermal analysis of the integrated electric drive systems
Sandia National Laboratories	Will provide wide bandgap device models and samples when they are available
AMES LABORATORY Creating Materials & Energy Solutions U.S. DEPARTMENT OF ENERGY	Providing properties of newly developed magnetic materials for the traction motor drive.

Remaining Challenges

- Identify the optimum substrate area for the estimated inverter operating conditions
- Assess the feasibility of the proposed internal stator mount integration
- Identify a suitable place to integrate output current sensors, input voltage sensors, busbars, and identify low profile connectors for terminations

Proposed future work

- **Remainder of FY21**
  - Evaluate substrates to identify minimum substrate area for the estimated losses
  - Characterize the flat capacitor boards and identify current conduction capability of the designed capacitor packages

- **Future work – FY22**
  - Build a DBC based substrate to fit within the identified space inside the outer rotor motor
  - Characterize different current sensors, select one, and integrate with the inverter
  - Build and characterize a single phase leg power module

Any proposed future work is subject to change based on funding levels

Summary

- **Relevance:** The core function of this project is to research technologies that will allow the integration of inverter with the motor to meet DOE ELT 2025 power density target of 33kW/L for a 100kW integrated electric drive.
- **Approach:**
  - Identify ways to fit the inverter components inside the designed outer rotor motor to achieve tight integration
  - Characterize and package capacitors to identify promising capacitor technology for volume along with electrical performance optimization
  - Optimize substrate dimensions for the estimated inverter loss
- **Collaborations:**
  - **NREL:** Designing cooling structures for internal stator mount integration technique
  - Interactions are ongoing with Sandia and AMES
- **Technical Accomplishments:**
  - Identified available dimensions for inverter integration with outer rotor motor
  - Designed circular capacitor package with emerging PLZT based capacitor to optimize volume and performance
  - Estimated inverter losses for the designed outer rotor motor
  - Evaluated a DBC based substrate for the proposed integration method
- **Future Work:**
  - Complete the DBC based substrate analysis to evaluate minimum substrate area for the estimated inverter losses
  - Evaluate flat capacitor boards and identify current conduction capability of the designed packages

Any proposed future work is subject to change based on funding levels