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2021 DOE Vehicle Technology Office Annual Merit Review

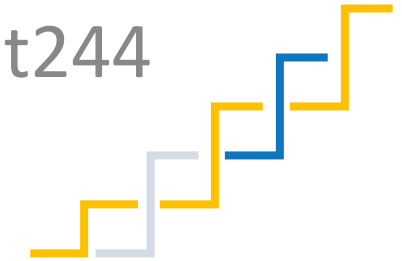
Next-Generation, High-Temperature, High-Frequency, High-Efficiency, High-Power Density Traction System

PI: Robert Pilawa-Podgurski

University of California, Berkeley

June 21-25, 2021

Project ID: elt244



This presentation does not contain any proprietary, confidential, or otherwise restricted information.

Overview

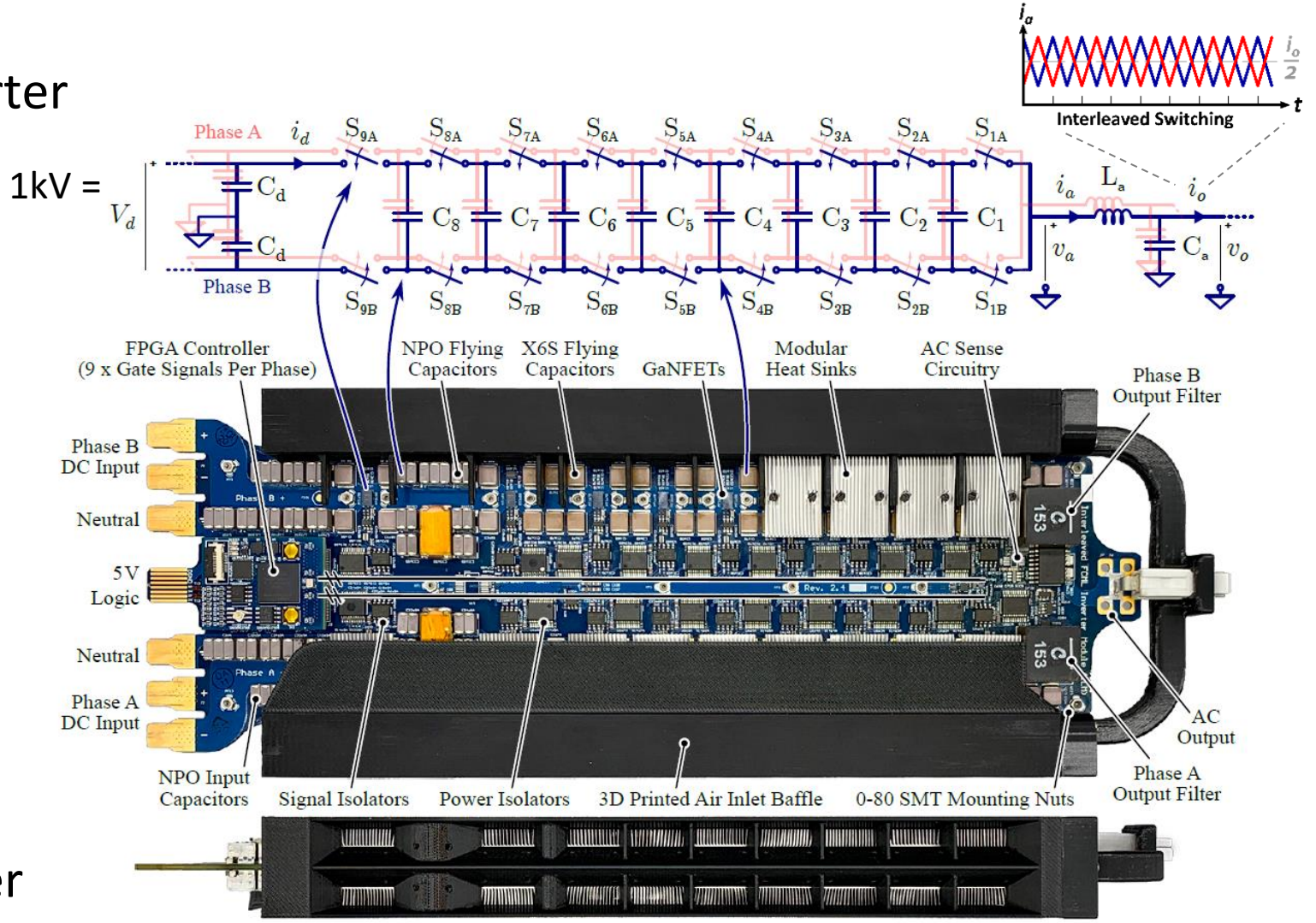
- Timeline: 6/1/2019 – 6/1/2024
- Budget/Spend Plan
  - Total Cost: $1.5M
  - FY 2019: $300k
- Milestones
  - Preliminary design validated
  - Thermal and PCB co-design completed
  - Low-level control tested
  - Inverter cost ≤ $2.7/kW
  - Inverter power density ≥ 100 kW/L
  - Demo hardware at 100 kW peak
- Barriers (EETT 2025 Roadmap)
  1. *WBG device power and voltage levels and availability*
  2. *WBG multi-physics integration designs to enable optimal use*
  3. *Component optimization for miniaturization and cost reduction.*
  4. *Low inductance requirements for WBG multi-physics integration*
- Partners
  - National laboratories and university partners

Approach – Novel Topology

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Flying Capacitor Multilevel Converter

- Energy dense capacitors are used in power processing
- Multilevel operation, high effective frequency reduces required filter for a given THD
- Wide-bandgap devices facilitate fast switching, low losses and compact design
- High switching frequency reduces the size of the power processing capacitors
- Dual-interleaved design further reduces filter requirements



Y1 15 kW-scale Hardware Prototype

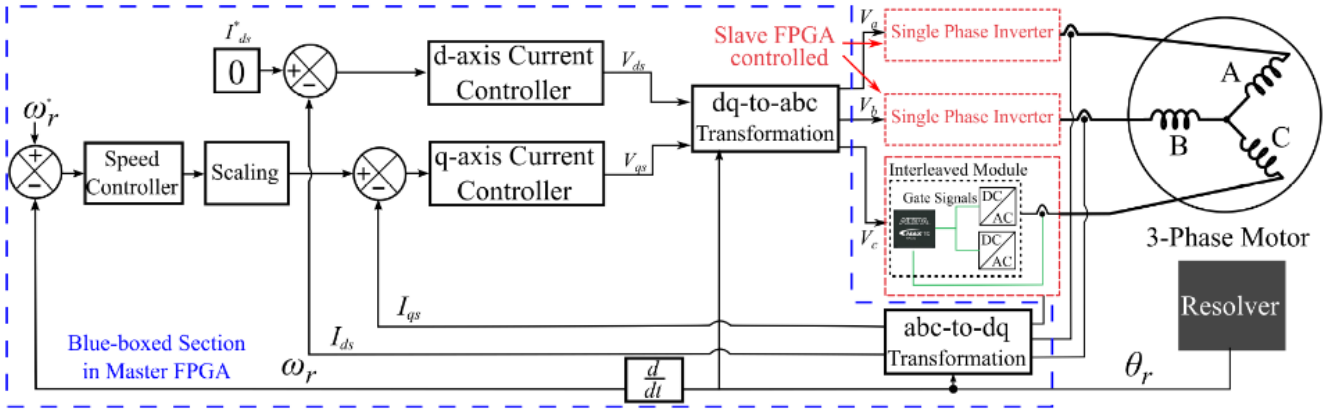
Approach – Scalability & Redundancy

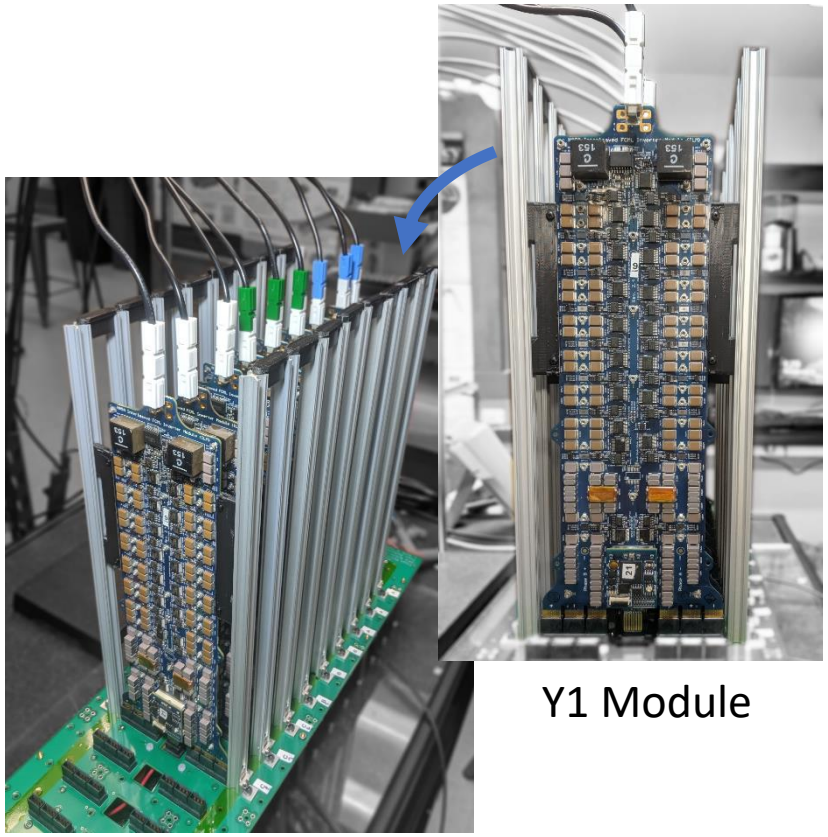
Individual modules rated to a fraction of the total power

- Simplifies design, manufacturing and test scope, with individual modules optimized based on loss-model and volume cost functions (*barrier 2*)
- Modules can be paralleled for more phases or current
- Potential reliability boost through redundant hardware

Hierarchical control coordinates drive behavior

- Local controllers run PWM, balance interleaved currents
- Master controller delegates torque commands
- Shedding modules may improve light-load efficiency





Y1 Module

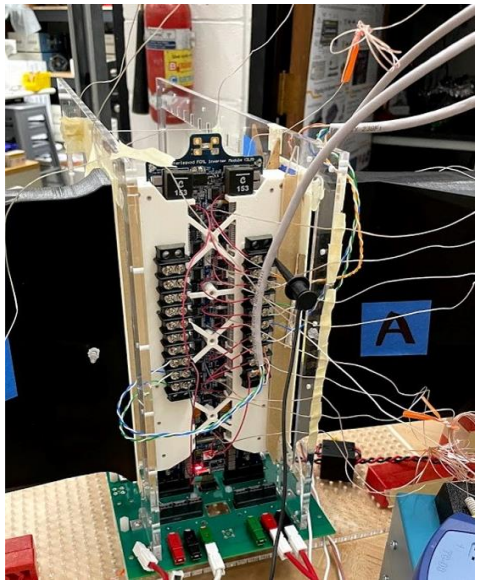
Y1 Array

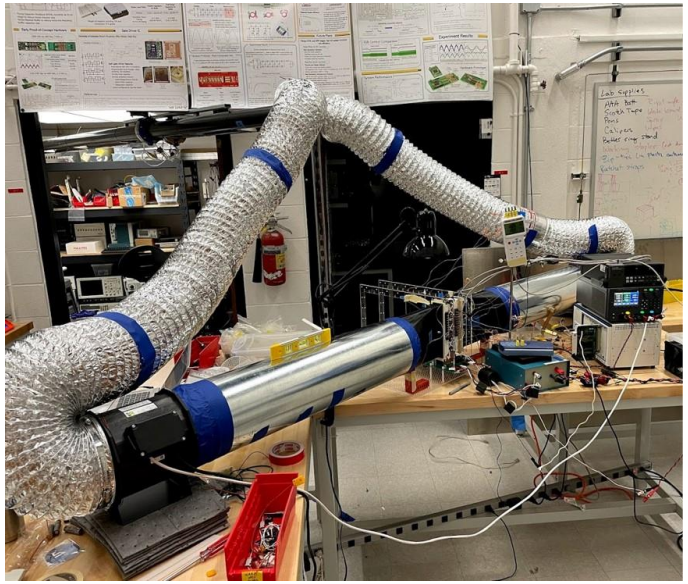
Accomplishments – Thermals

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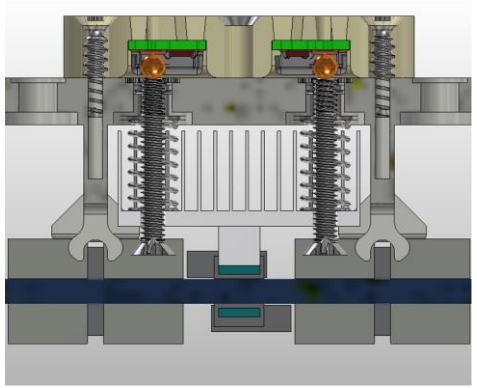
- New snap-fit features designed into manifold to greatly reduce assembly complexity
- Heatsink mounting system designed for measuring contact pressure and temperature of devices
- A thermal test rig was tested and performance of the thermal management strategy was recorded for an entire phase (x 18) active devices. At maximum mass flow, **4.2-5.3°C/W was realized**.

Experimental Setup

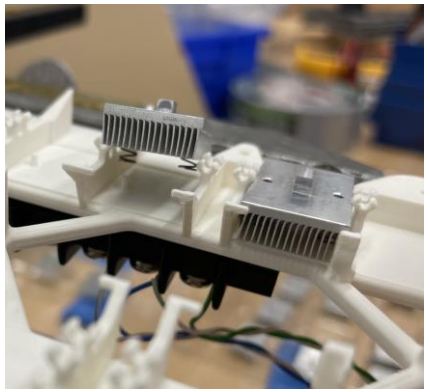




Snap-Fit Features

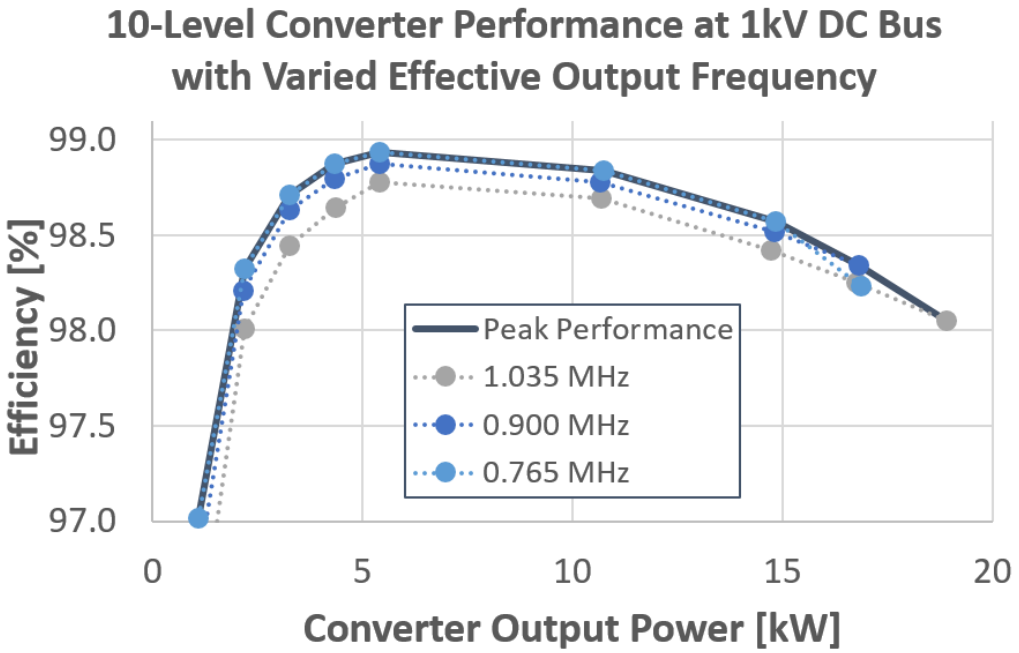






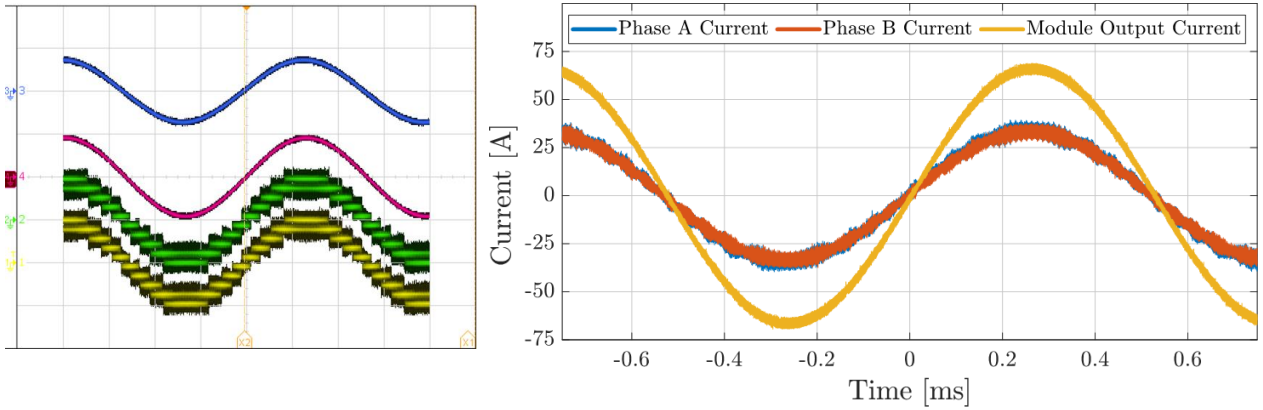
Acc. – Performance Testing

- High-power test setup designed to assess performance of newest module design
- Phase currents of dual-interleaved module shown to match well
- Interleaving effectively reduces output current ripple, thus improving THD
- Capacitor balancing is excellent
- Efficiency measurements taken at different frequencies and loads



Experimental performance includes gate drive and controller losses

Experimental Waveforms

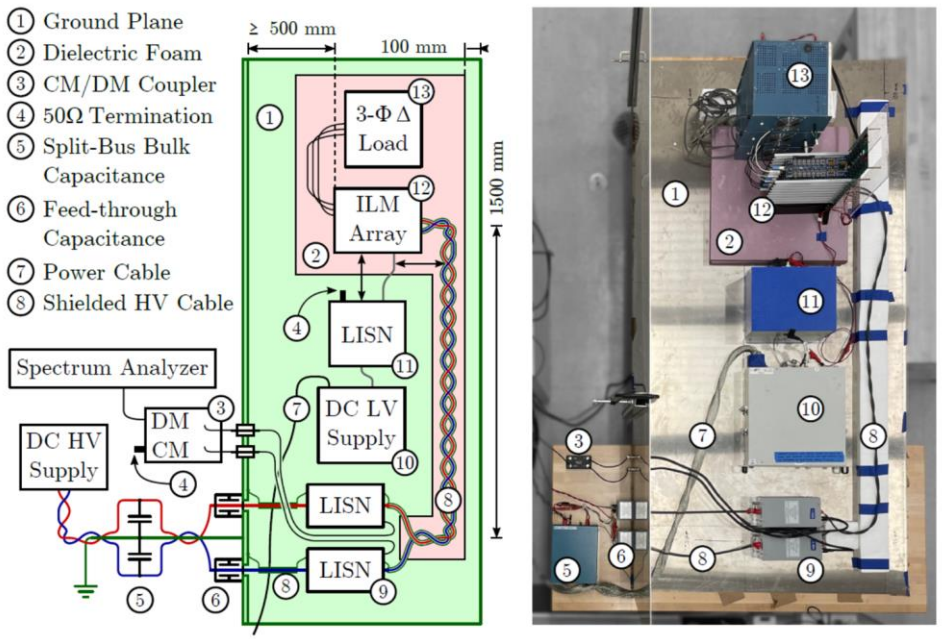


Peak Efficiency	Peak Power	Power Density
98.95%	18.9 kW	**38.4 kW/kg**

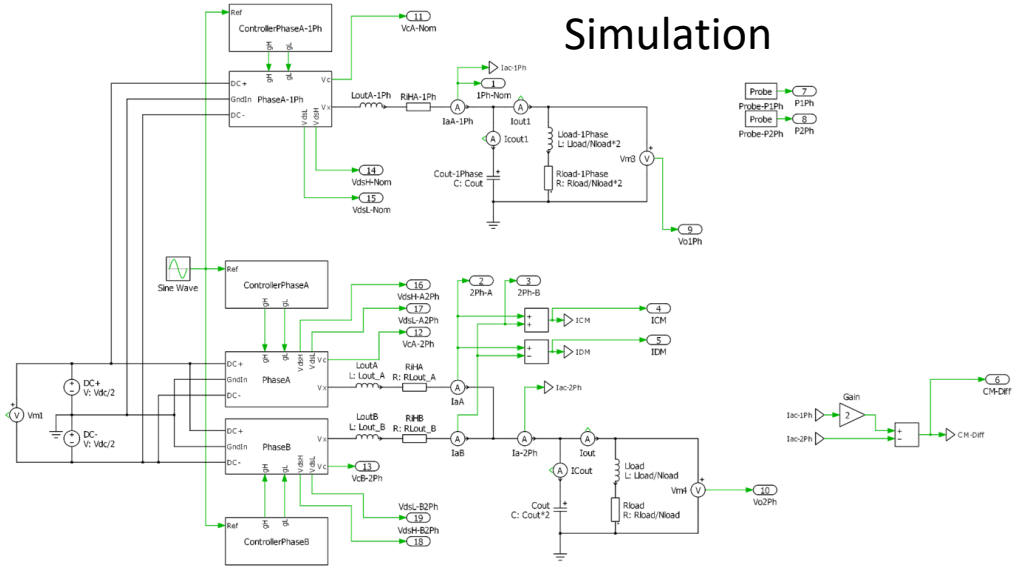
Acc. – EMI Analysis & Testing

- Double Fourier technique used to estimate conducted waveforms
- Simulations performed to analyze output currents based on converter operating parameters
- Full CISPR-25 EMC testbench designed
- EMI testing performed for both individual and interleaved modules

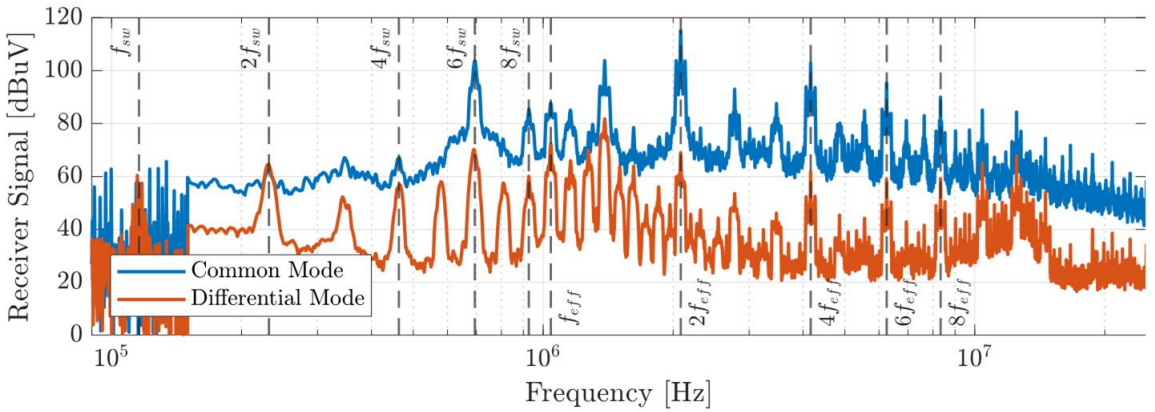
EMI Testing Setup



Simulation

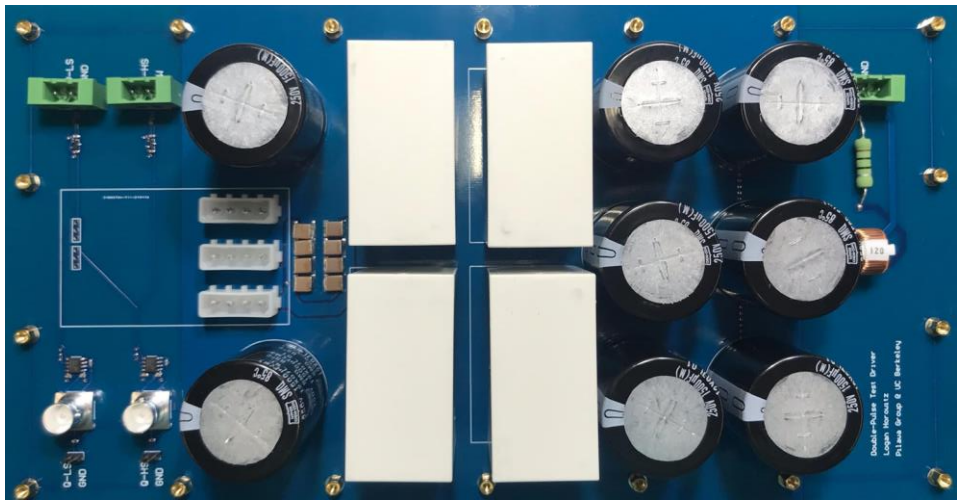


Experimental EMI Results



Acc. – Converter Design

- Parasitic inductances arising from layout severely hinder performance
- Software developed to estimate these inductances and experimental measurements done to validate it
- New switching cell and 4-level converter designed to test improved layout and compare devices
- Double-pulse-test board fabricated to analyze voltage overshoots in converter and optimize component selection for new design

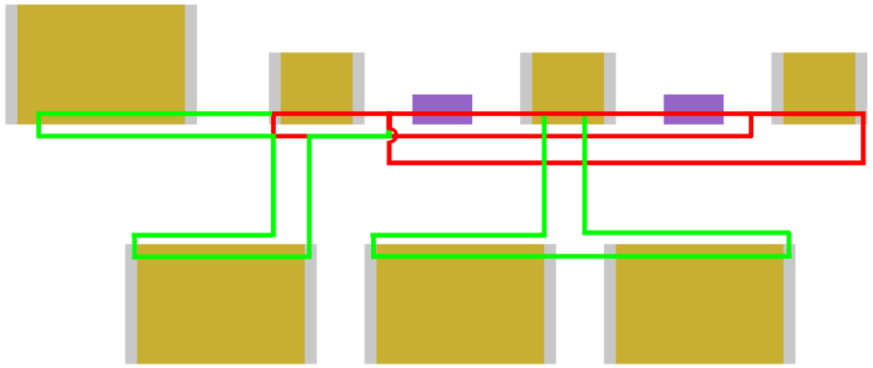


Double-Pulse-Test Circuit Board



< 1 nH Inductance!

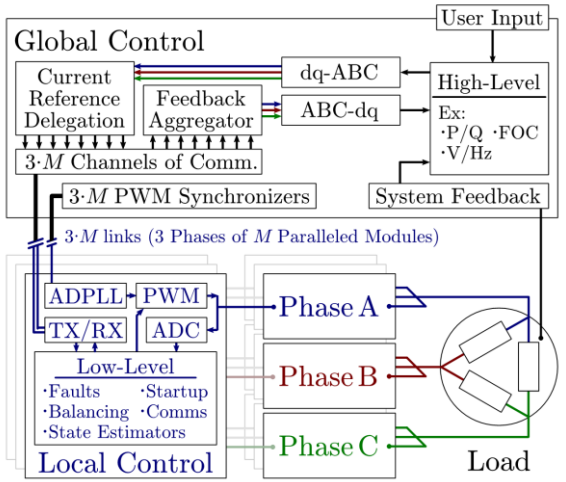
New Switching Cell Design



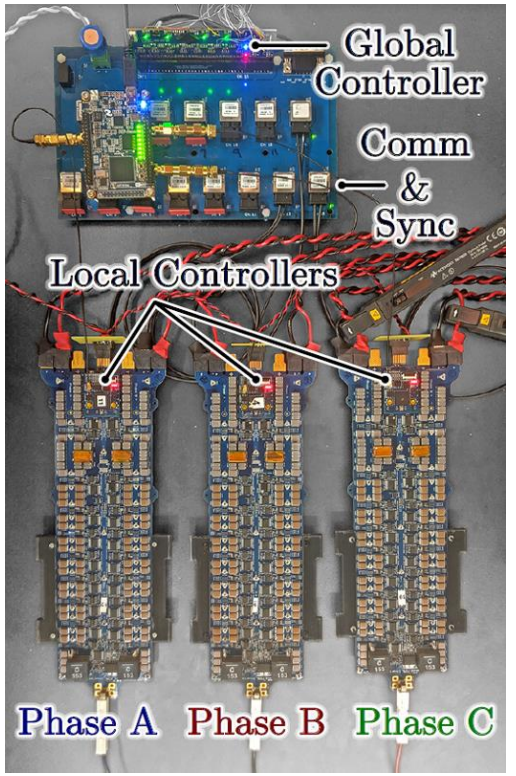
Acc. – Control

- Switching-frequency synchronization and interleaving achieved through phase-locked-loop design
- New global controller fabricated and testing has begun to develop a robust electrical communication protocol allowing deletion of complex, expensive optical link currently in use
- Migrating global control to C2000 co-processor for high performance motor control algorithms

Overall Control Diagram



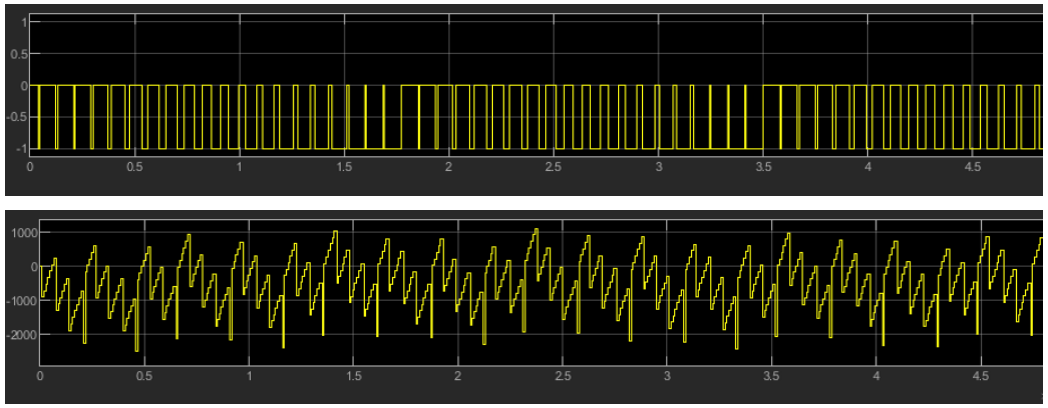
Synchronization Testing



New Global Controller



PLL Waveforms



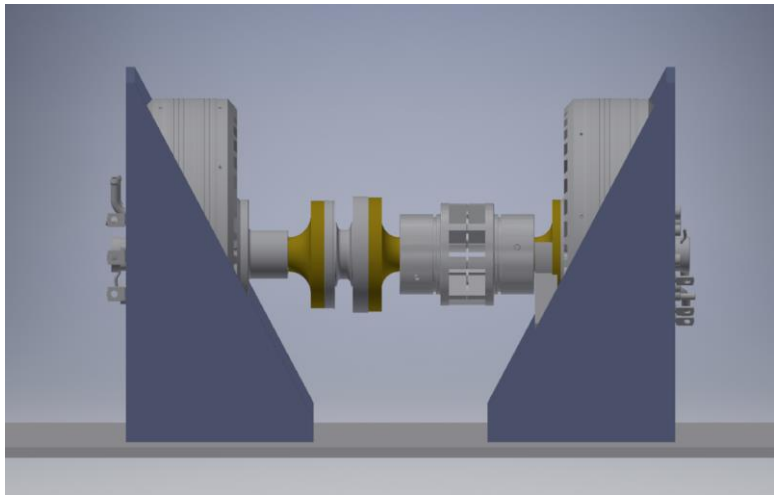
Proposed Future Research

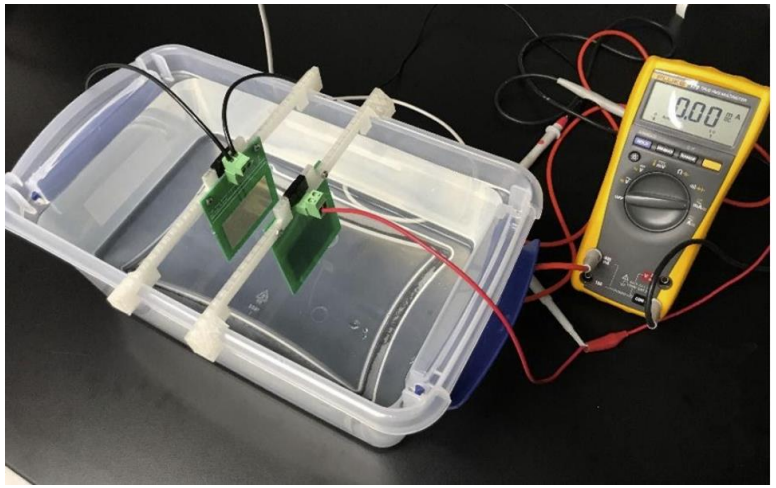
- High-Power Dynamometer

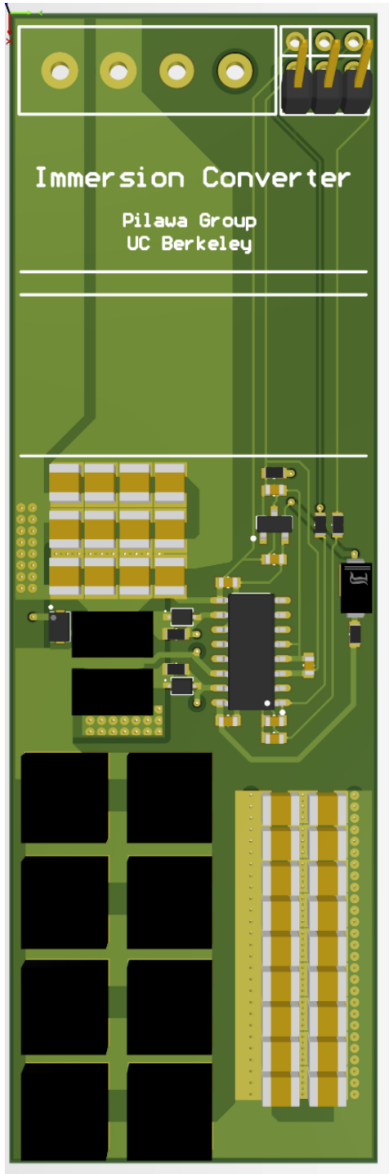
  The design phase of a custom high power dyno design has finished and manufacturing has begun. The dyno incorporates two low-inductance Emrax 348 motors (peak power 380 kW) allowing the validation of the novel inverter system driving high power motors.

- Development of novel immersion cooling dielectrics

  Parylene and SiO2 coating recipes for potential liquid-immersion cooling have been manufactured in-house and tested on sample devices and circuit boards.







Any proposed future work is subject to change based on funding levels.

Summary

- Enable dramatic cost and size reduction in EV traction inverters through new circuit topologies, which can exploit low-voltage (e.g., GaN) transistors in a high-voltage applications
  - Reduced passive component size
  - Conventional PCB-style hardware
  - Improved cooling through distributed heat generation
- Further the understanding and control of FCML converter dynamics under various motor operating points and transients
- Seek to rapidly demonstrate concepts and performance in hardware
- Execute key DOE research objective of training students

5 grad: Nathan Pallo, Samantha Coday, Logan Horowitz, Joseph Schaadt, Rod Bayliss

1 undergrad: Amanda Jackson

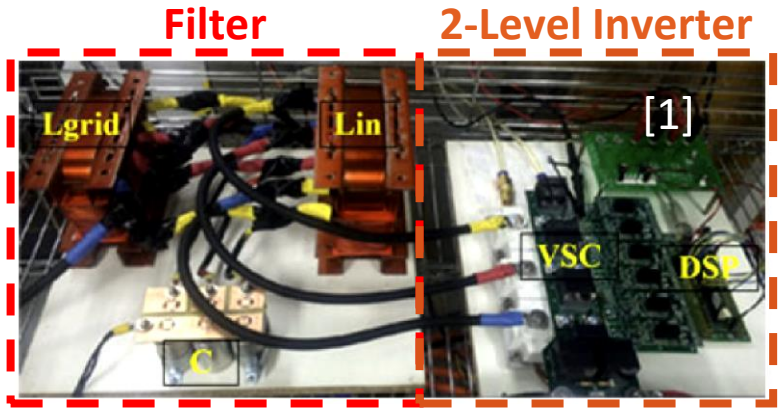
Course module on multilevel converters and electric vehicles in FA2019 power electronics class

Course module on multilevel converters and electric vehicles in SP2020 power systems class

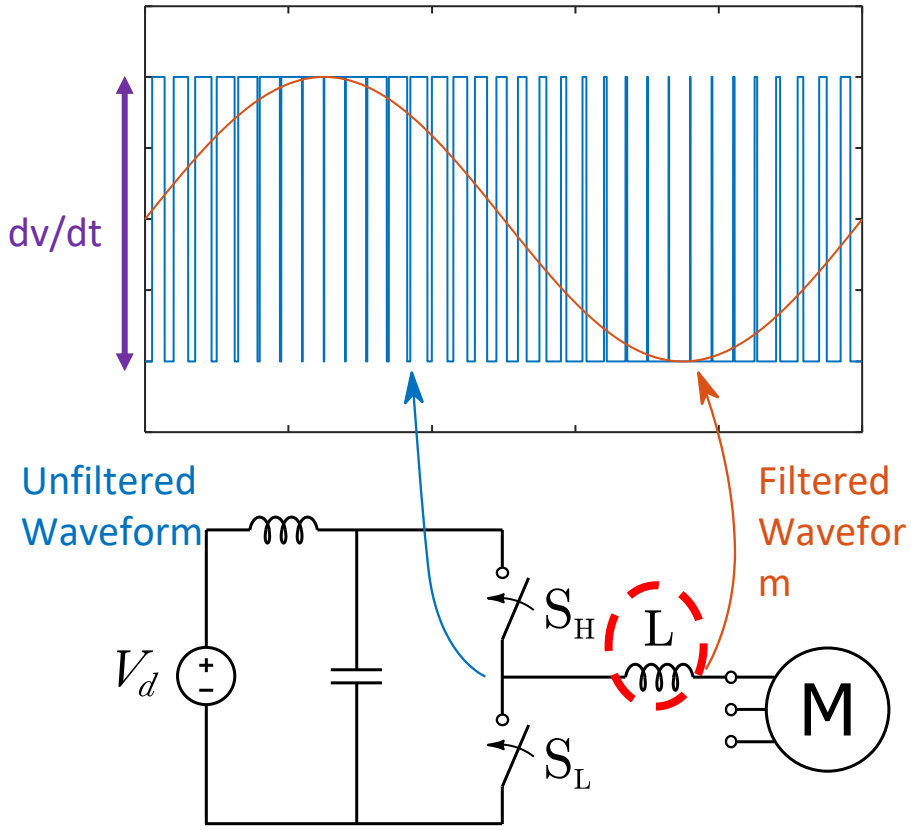
Back-Up Slides Next

Traditional Approach

- 2-level converters have been the standard approach
  - Requires large inductive filters (dv/dt limiter)
  - Increased motor losses due to harmonic
  - Large bus capacitance required



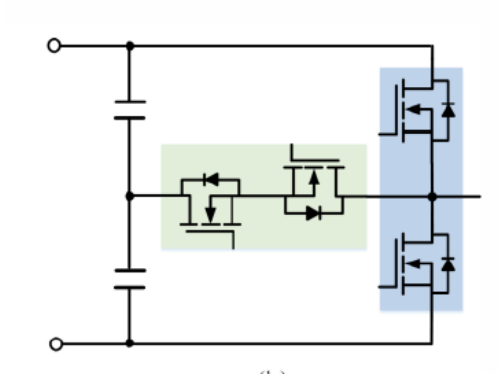
  - Custom power modules and gate drivers
  - Typically low redundancy [2]
  - Cooling can be challenging due to hot-spots



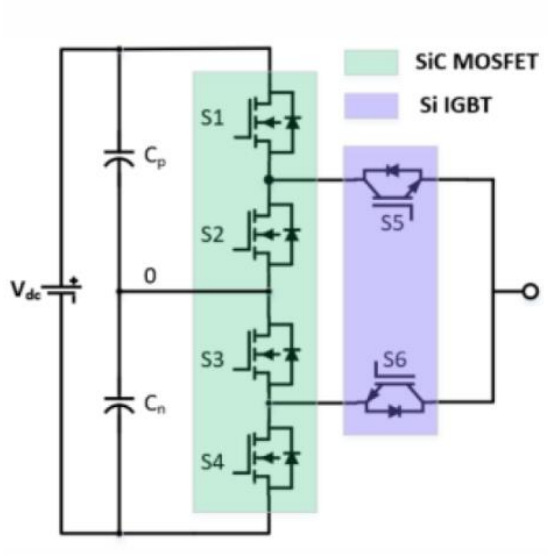
[1] Liu, et al., "LCL Filter Design of a 50-kW 60-kHz SiC Inverter with Size and Thermal Considerations for Aerospace Applications," IEEE TIE, 2017.
[2] E. Gurpinar, et al., "SiC MOSFET-Based Power Module Design and Analysis for EV Traction Systems," IEEE ECCE, 2018.

Traditional Approach

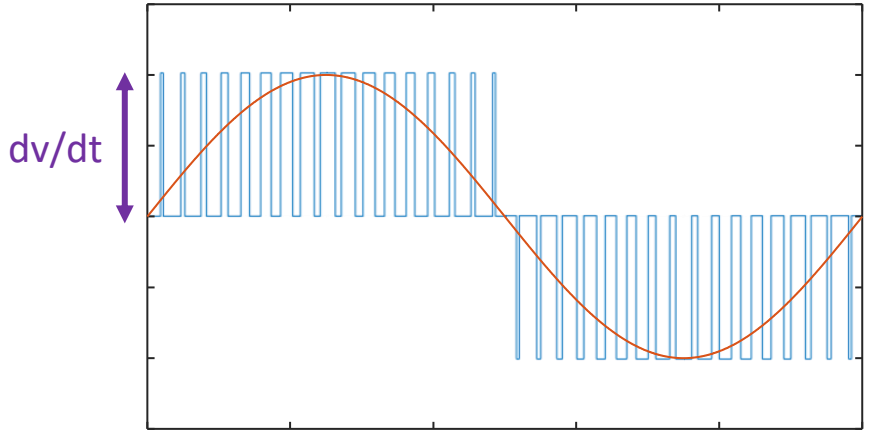
- 3-level neutral-point-clamp (NPC) topologies can reduce dv/dt
  - Similar design strategy as 2-level designs
  - Still require HV devices, high dv/dt



T-type NPC Phase Leg [4]



Active NPC Phase Leg [5]



– Both still require large volume/mass of filter magnetics at the output

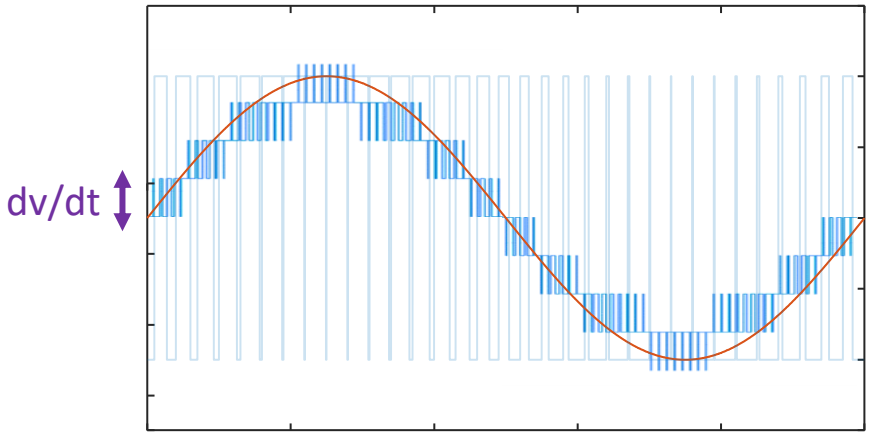
[3] Z. Wang, et. al, "Design and Validation of A 250 kW All Silicon Carbide High-Density Three-Level T-Type Inverter," IEEE JESTPE, 2019
[4] D. Pan, et al., "Control of MW-Scale High-Frequency "SiC+Si" Multilevel ANPC Inverter … for Aircraft … Applications," IEEE JESTPE, 2020

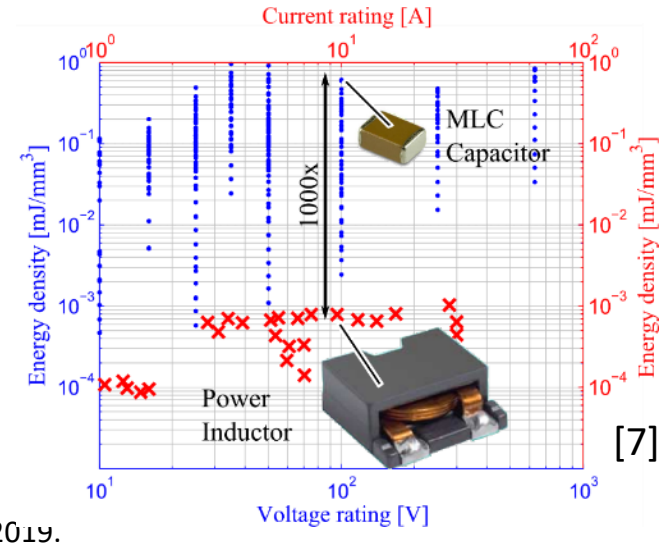
An Unconventional Approach

- Flying Capacitor Multilevel Converter
  - Low dv/dt with high level count
  - High effective switching frequency

Key Benefit [6]	2-Level	FCML
Switch Stress	V	V/(N-1)
V_{sw} Ripple Amplitude	V	V/(N-1)
V_{sw} Ripple Frequency	f	(N-1)f
Output Inductance	L	$L/(N-1)^2$

  - Allows the use of lower-cost, low-voltage WBG devices
  - Energy dense capacitors process most of the converter energy





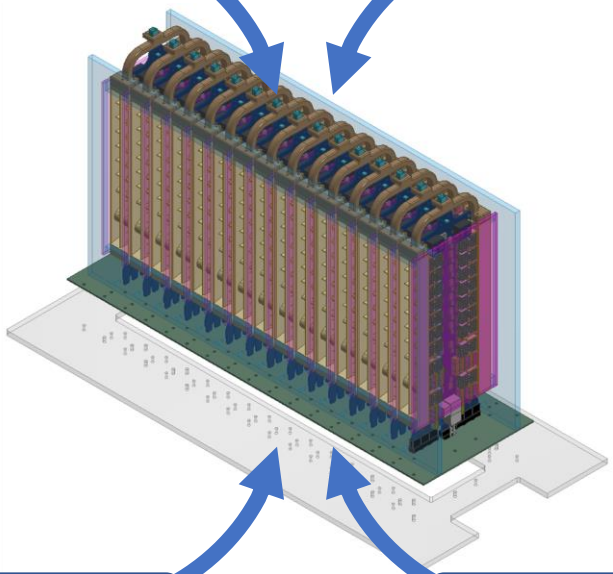
[7]

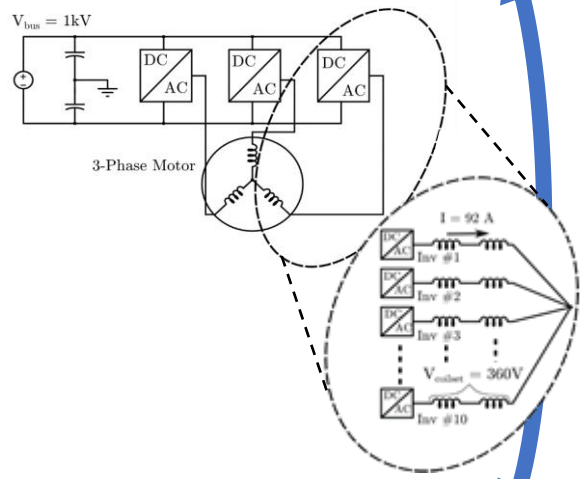
[5] C T. Meynard and H. Foch, "Multilevel conversion: high voltage choppers and voltage-source inverters," IEEE PESC, 1992.
[6] C. B. Barth, et. al, "Experimental Evaluation of Capacitors for Power Buffering in Single-Phase Power Converters," IEEE TPE, 2019.

Overall Approach

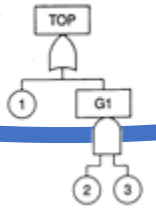
High-Performance Inverter Design and Modeling

Dynamics & Control of FCML Inverter Module





Reliability Assessment and FDI for FCML

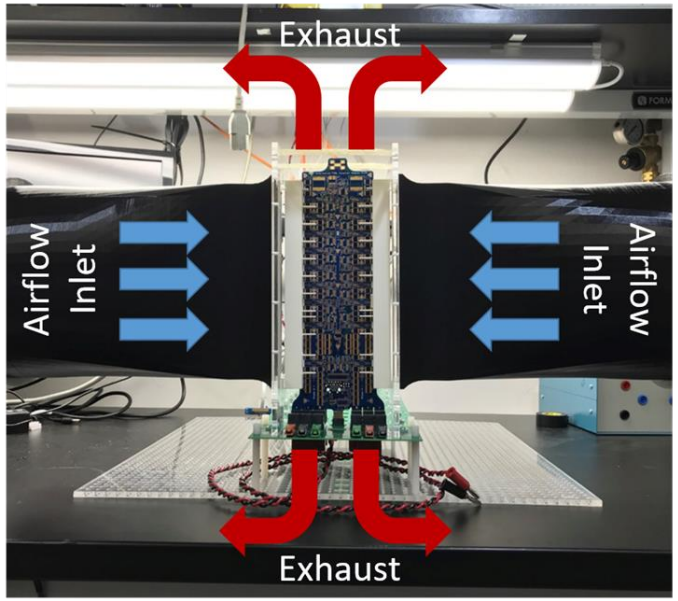


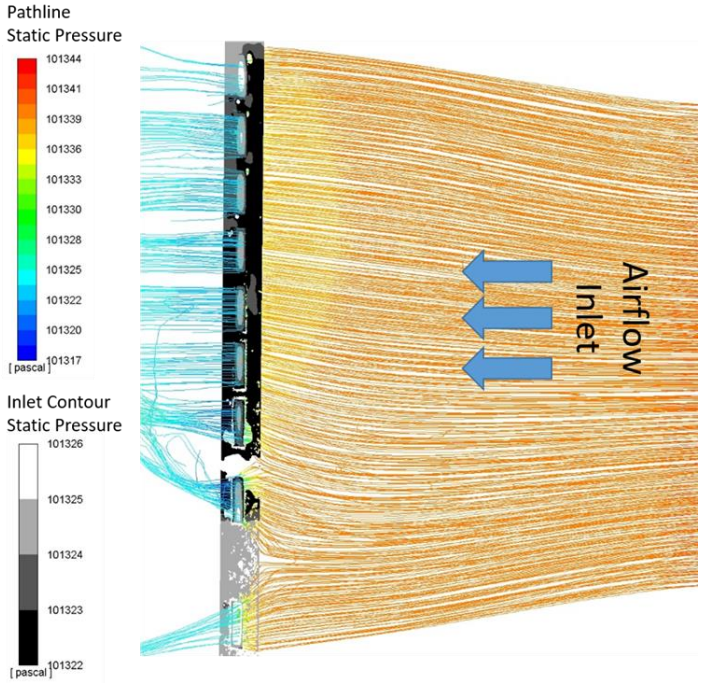
Scalability and Paralleling of Inverter Modules

Approach – Thermal Design

- Design of 3D-printed baffles and inlet ducts to guide flowing air
  - Ensures air is directed through heatsinks
- CFD simulation to ensure uniform pressure front at inlets of converter
  - Allows for optimization of inlet duct design

Current air-cooled test setup with inlet ducts directing air through baffles





CFD indicates negligible pressure or temperature difference across heat sinks